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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C800
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	RAM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	P-DSO-28
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-c868-1sg-ba

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- One 8-bit and one 5 bits general purpose push-pull I/O ports
  – Enhanced sink current of 10 mA on Port 1/3 (total max current of 43 mA @ 100^{o}C)
- Three 16-bit timers/counters
  –Timer 0 / 1 (C501 compatible)
  –Timer 2 (up/down counter feature)
  –Timer 1 or 2 can be used for serial baudrate generator
- Capture/compare unit for PWM signal generation
  –3-channel, 16-bit capture/compare unit
  –1-channel, 16-bit compare unit
- Full duplex serial interface (UART)
- 5 channel 8-bit A/D Converter
  – Start of conversion can be synchronized to capture/compare timer 12/13.
- 13 interrupt vectors with four priority levels
- Programmable 16-bit Watchdog Timer
- Brown out detection
- Power Saving Modes
  –Slow-down mode
  –Idle mode (can be combined with slow-down mode)
  –Power-down mode with wake up capability through $\overline{\text{INT0}}$ or RxD pins.
- Single power supply of 3.3V, internal voltage regulator for core voltage of 2.5V.
- P-DSO-28-1, P-TSSOP-38-1 packages
- Temperature ranges:
  SAF-C868-1RR BA, SAF-C868-1SR BA, SAF-C868-1RG BA, SAF-C868-1SG BA, SAF-C868A-1RR BA, SAF-C868A-1SR BA, SAF-C868A-1RG BA, SAF-C868A-1SG BA, SAF-C868P-1SR BA, SAF-C868P-1SG BA T_A = – 40 to 85 ^{o}C
  SAK-C868-1RR BA, SAK-C868-1SR BA, SAK-C868-1RG BA, SAK-C868-1SG BA, SAK-C868A-1RR BA, SAK-C868A-1SR BA, SAK-C868A-1RG BA, SAK-C868A-1SG BA, SAK-C868P-1SR BA, SAK-C868P-1SG BA T_A = – 40 to 125 ^{o}C

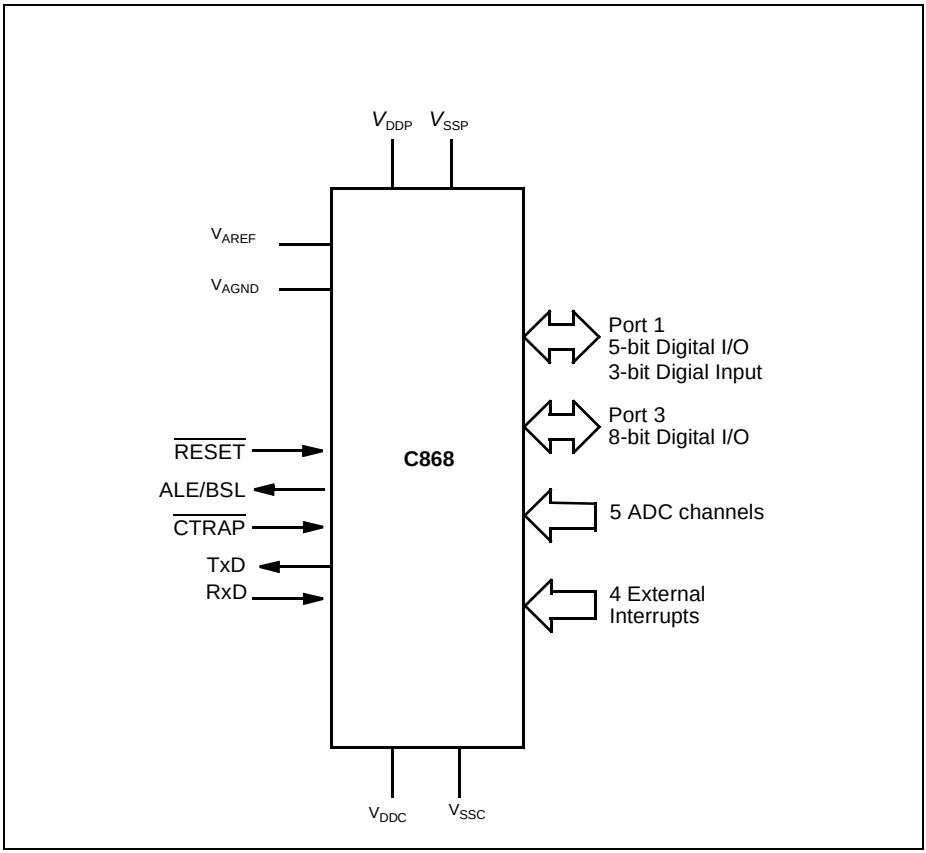

Figure 2 Logic Symbol

CPU

The C868 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 10.67 MHz external crystal (giving a 40MHz CPU clock), 58% of the instructions execute in 300 ns.

PSW

Program Status Word Register **[Reset value: 00_H]**

$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$
CY	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**
rwh	rwh	rw	rw	rw	rwh	rw	rwh

Field	Bits	Typ	Description
P	0	rwh	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.
F1	1	rw	**General Purpose Flag**
OV	2	rwh	**Overflow Flag** Used by arithmetic instructions.
RS0 **RS1**	3 4	rw	**Register Bank select control bits** These bits are used to select one of the four register banks. **Table 2 :** **RS1** / **RS0** / **Function** 0 / 0 / Bank 0 selected, data address 00_H-07_H 0 / 1 / Bank 1 selected, data address 08_H-$0F_H$ 1 / 0 / Bank 2 selected, data address 10_H-17_H 1 / 1 / Bank 3 selected, data address 18_H-$1F_H$
F0	5	rw	**General Purpose Flag**
AC	6	rwh	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
CY	7	rwh	**Carry Flag** Used by arithmetic instructions.

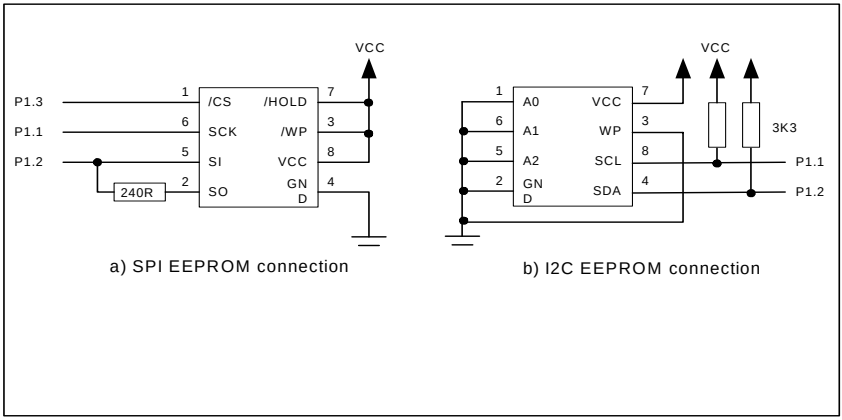

Figure 9 EEPROM connections for a) SPI and b) I2C

The PLL output frequency is determined by:

$$f_{PLL} = f_{VCO} / K = \frac{15}{K} \times f_{OSC} \quad [1]$$

The range for the VCO frequency is given by:

$$100\ MHz \leq f_{VCO} \leq 160\ MHz \quad [2]$$

The relationship between the input frequency and VCO frequency is given by:

$$f_{VCO} = 15 \times f_{OSC} \quad [3]$$

This gives the range for the input frequency which is given by:

$$6.67\ MHz \leq f_{OSC} \leq 10.67\ MHz \quad [4]$$

Table 5 Output Frequencies f_{PLL} Derived from Various Output Factors

K-Factor		f_{PLL}		Duty Cycle [%]	Jitter
Selected Factor	**KDIV**	**f_{VCO} = 100 MHz**	**f_{VCO} = 160 MHz**		
2	000_B	50	80	50	linear depending on f_{VCO} at f_{VCO} =100MHz: +/-300ps at f_{VCO} =160MHz: +/-250ps additional jitter for odd Kdiv factors tbd.
4	010_B	25	40	50	
5[1)]	011_B	20	32	40	
6	100_B	16.67	26.67	50	
8	101_B	12.5	20	50	
9[1)]	110_B	11.11	17.78	44	
10	111_B	10	16	50	
16	001_B	6.25	10	50	

1) These odd factors should not be used (not tested because off the unsymmetrical duty cycle).

2) Shaded combinations should not be used because they are above the maximum CPU frequency of 40MHz.

Figure 12 shows the recommended oscillator circuitries for crystal and external clock operation.

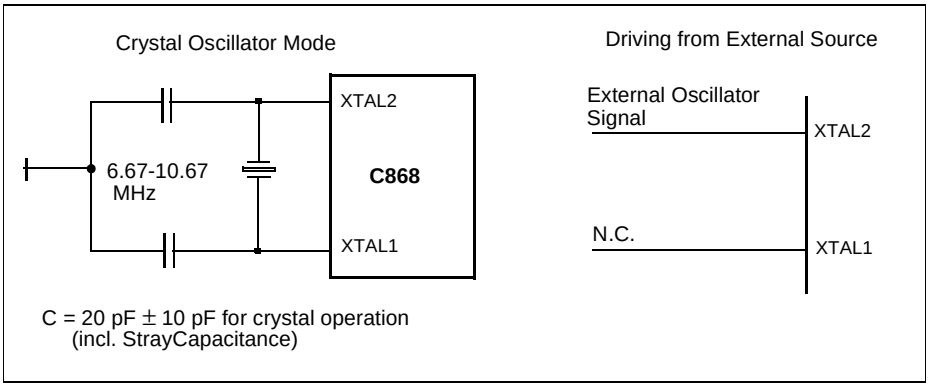

Figure 12 Recommended Oscillator Circuit

In this application the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **Figure 13**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit tbd pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally have different values depending on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.

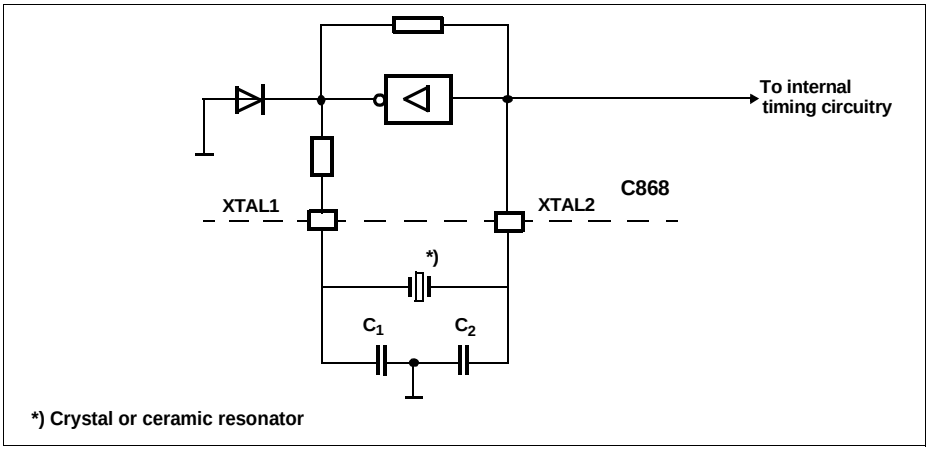

Figure 13 On-Chip Oscillator Circuitry

To drive the C868 with an external clock source, the external clock signal has to be applied to XTAL2, as shown in **Figure 14**. XTAL1 has to be left unconnected. A pullup resistor is suggested (to increase the noise margin), but is optional if V_{OH} of the driving gate corresponds to the V_{IH2} specification of XTAL2.

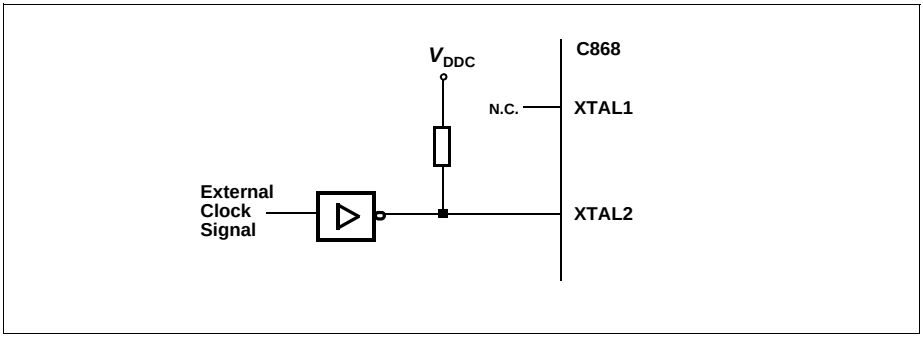

Figure 14 External Clock Source

Table 6 Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
C800 core	ACC	Accumulator	**$E0_H$**[1]	**00_H**
	B	B-Register	**$F0_H$**[1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	84_H	00_H
	PSW	Program Status Word Register	**$D0_H$**[1]	**00_H**
	SP	Stack Pointer	81_H	07_H
	SCON	Serial Channel Control Register	**98_H**[1]	**00_H**
	SBUF	Serial Data Buffer	99_H	00_H
	IEN0	Interrupt Enable Register 0	**$A8_H$**[1]	**$0X000000_B$**[2]
	IEN1	Interrupt Enable Register 1	$A9_H$	$XXXXX000_B$[2]
	IEN2	Interrupt Enable Register 2	AA_H	$XX0000XX_B$[2]
	IP0	Interrupt Priority Register 0	**$B8_H$**[1]	**$XX000000_B$**[2]
	IP1	interrupt Priority Register 1	AC_H	$XX000000_B$[2]
	TCON	Timer 0/1 Control Register	**88_H**[1]	**00_H**
	TMOD	Timer Mode Register	89_H	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	PCON	Power Control Register	87_H	$0XXX0000_B$[2]
System	PMCON0	Wake-up Control Register	$8E_H$	$XXX00000_B$[2]
	CMCON	Clock Control Register	$8F_H$	10011111_B
	EXICON	External Interrupt Control Register	91_H	$XXXXXX00_B$[2]
	IRCON0	External Interrupt Request Register	92_H	$XXXXXX00_B$[2]
	IRCON1	Peripheral Interrupt Request Register	93_H	$XX0000X0_B$[2]
	PMCON1	Peripheral Management Ctrl Register	**$E8_H$**[1]	**$XXXXX000_B$**[2]
	PMCON2	Peripheral Management Status Register	**$F8_H$**[1]	**$XXXXX000_B$**[2]
	SCUWDT	SCU/Watchdog Control Register	**$C0_H$**[1]	**$X0X00000_B$**[2]
	VERSION	ROM Version Register	$F9_H$	00_H
	SYSCON0	System Control Register 0	AD_H	$XX10XXX1_B$[2]
	SYSCON1	System Control Register 1	AF_H	$00XXX0X0_B$[2]

1) Bit-addressable special function registers
2) “X“ means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Add-ress	Contents after Reset
Cap-ture/ Com-pare Unit	ISSL[3]	Cap/Com Int Status Set Reg, Low Byte	BC_H	00_H
	ISSH[3]	Cap/Com Int Status Set Reg, High Byte	BD_H	00_H
	ISRL[4]	Cap/Com Int Status Reset Reg, Low Byte	BC_H	00_H
	ISRH[4]	Cap/Com Int Status Reset Reg,High Byte	BD_H	00_H
	INPL[3]	Cap/Com Int Node Ptr Reg, Low Byte	BE_H	40_H
	INPH[3]	Cap/Com Int Node Ptr Reg, High Byte	BF_H	39_H
	IENL[4]	Cap/Com Interrupt Register, Low Byte	BE_H	00_H
	IENH[4]	Cap/Com Interrupt Register, High Byte	BF_H	00_H
	CC60SRL	Cap/Com Channel 0 Shadow, Low Byte	FA_H	00_H
	CC60SRH	Cap/Com Channel 0 Shadow, High Byte	FB_H	00_H
	CC61SRL	Cap/Com Channel 1 Shadow, Low Byte	FC_H	00_H
	CC61SRH	Cap/Com Channel 1 Shadow, High Byte	FD_H	00_H
	CC62SRL	Cap/Com Channel 2 Shadow, Low Byte	FE_H	00_H
	CC62SRH	Cap/Com Channel 2 Shadow, High Byte	FF_H	00_H
	CC63SRL	T13 Compare Shadow Reg, Low Byte	$B6_H$	00_H
	CC63SRH	T13 Compare Shadow Reg, High Byte	$B7_H$	00_H
	MODCTRL[3]	Modulation Control Register, Low Byte	$D6_H$	00_H
	MODCTRH[3]	Modulation Control Register, High Byte	$D7_H$	00_H
	TRPCTRL	Trap Control Register, Low Byte	CE_H	00_H
	TRPCTRH	Trap Control Register, High Byte	CF_H	00_H
	PSLRL	Passive State Level Register, Low Byte	$A6_H$	00_H
	MCMOUTL[3]	MCM Output Register, Low Byte	DC_H	00_H
	MCMOUTH[3]	MCM Output Register, High Byte	DD_H	00_H
	MCMOUTSL[4]	MCM Output Shadow Register, Low Byte	DC_H	00_H
	MCMOUTSH[4]	MCM Output Shadow Register,High Byte	DD_H	00_H
	MCMCTRLL[4]	MCM Control Register, Low Byte	$D6_H$	00_H
	T12MSELL	T12 Cap/Com Mode Sel Reg, Low Byte	$F6_H$	00_H
	T12MSELH	T12 Cap/Com Mode Sel Reg, High Byte	$F7_H$	00_H

1) Bit-addressable special function registers
2) "X" means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B8_H$	IP0	$XX00\ 0000_B$	–	–	.5	.4	.3	.2	.1	.0
BB_H	PISELH	00_H	–	–	ISPOS2.1	ISPOS2.0	ISPOS1.1	ISPOS1.0	ISPOS0.1	ISPOS0.0
BC_H[3]	ISSL	00_H	ST12PM	ST12OM	SCC62F	SCC62R	SCC61F	SCC61R	SCC60F	SCC60R
BC_H[2]	ISRL	00_H	RT12PM	RT12OM	RCC62F	RCC62R	RCC61F	RCC61R	RCC60F	RCC60R
BD_H[3]	ISSH	00_H	–	SIDLE	SWHE	SCHE	–	STRPF	ST13PM	ST13CM
BD_H[2]	ISRH	00_H	–	RIDLE	RWHE	RCHE	–	RTRPF	RT13PM	RT13CM
BE_H[2]	IENL	00_H	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
BE_H[3]	INPL	00_H	INPCHE.1	INPCHE.0	INPCC62.1	INPCC62.0	INPCC61.1	INPCC61.0	INPCC60.1	INPCC60.0
BF_H[2]	IENH	00_H	–	ENIDLE	ENWHE	ENCHE	–	ENTRPF	ENT13PM	ENT13CM
BF_H[3]	INPH	00_H	–	–	INPT13.1	INPT13.0	INPT12.1	INPT12.0	INPERR.1	INPERR.0
$C0_H$	SCUWDT	00_H	–	PLLR	–	WDTR	WDTEOI	WDTDIS	WDTRS	WDTRE
$C2_H$	CC60RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CC60RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CC61RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CC61RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Timer/Counter 2 with Compare/Capture/Capture

Timer 2 is a 16-bit timer/counter with an up/down count feature. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator

Table 9 Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	T2EX	Remarks	System Clock	
	RCLK or TCLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN			Inte-rnal	T2
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{SYS} /12	max f_{SYS} /24
	0	0	X	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	down counting		
	0	0	1	1	X	1	up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	f_{SYS} /12	max f_{SYS} /24
	0	1	1	X	1	↓	capture T2H,T2L-> RC2H,RC2L		
Baudrate Generator	1	X	1	X	0	X	no overflow interrupt request(TF2)	f_{SYS} /2	-
	1	X	1	X	1	↓	extra external interrupt (“Timer 2“)		
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note: denotes a falling edge

Switching Examples

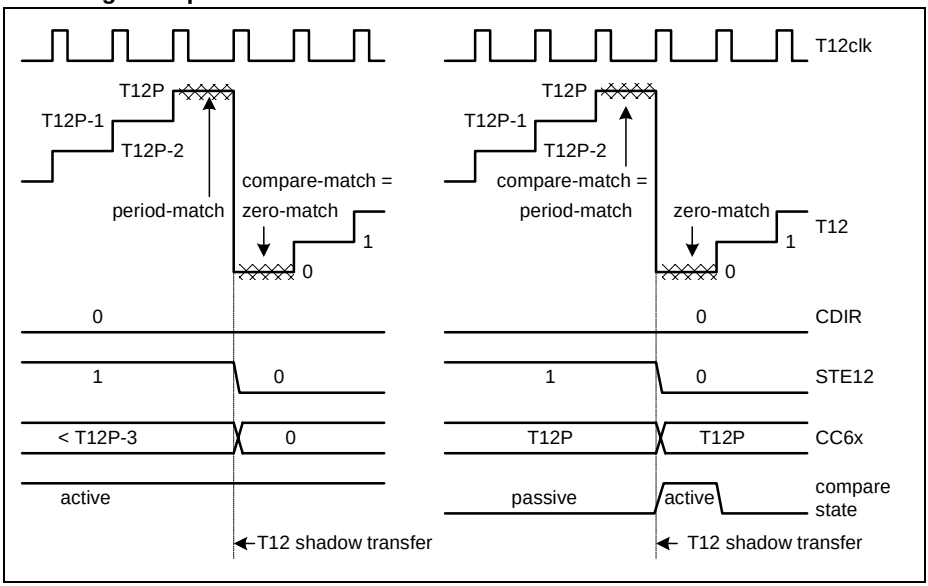

Figure 16 Edge-aligned mode with duty cycles near 100% and near 0%. Applicable to T13 as well.

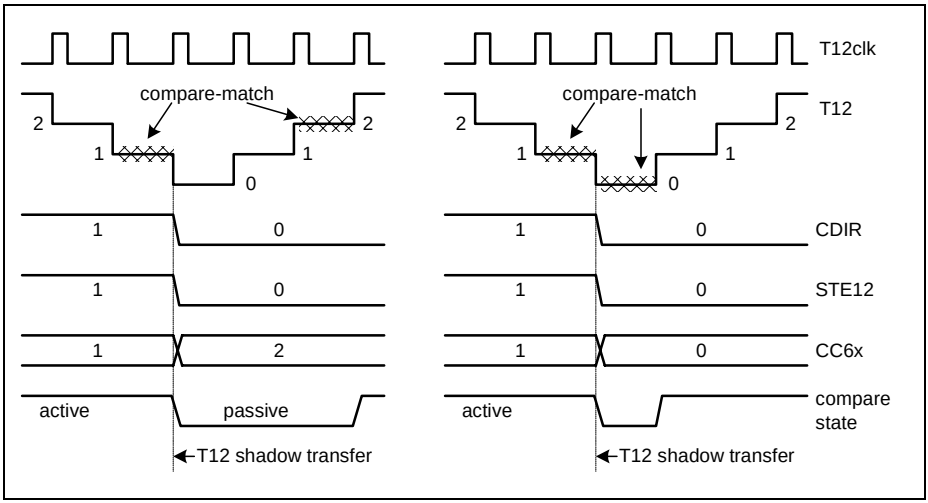

Figure 17 Centre-aligned mode with duty cycles near 100% and near 0%.

Hall Sensor Mode

In **Brushless-DC motors** the next multi-channel state values depend on the pattern of the Hall inputs. There is a strong correlation between the **Hall pattern** (CURH) and the **modulation pattern** (MCMP). Because of different machine types the modulation pattern for driving the motor can be different. Therefore it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding modulation pattern. The CCU6 offers this by having a register which contains the actual Hall pattern (CURHS), the next expected Hall pattern (EXPHS) and its output pattern (MCMPS). At every correct Hall event (CHE, see figure *Hall Event Actions*) a new Hall pattern with its corresponding output pattern can be loaded (from a predefined table) by software into the register MCMOUTS. Loading this shadow register can also be done by a write action on MCMOUTS with bit STRHP = '1'

The **sampling** of the Hall pattern (on CCPOSx) is done with the T12 clock. By using the dead-time counter DTC0 (mode MSEL6x= '1000') a hardware **noise filter** can be implemented to suppress spikes on the Hall inputs due to high di/dt in rugged inverter environment. In case of a Hall event the DTC0 is reloaded and starts counting. When the counter value of one is reached, the CCPOSx inputs are sampled (without noise and spikes) and are compared to the current Hall pattern (CURH) and to the expected Hall pattern (EXPH). If the sampled pattern equals to the current pattern the edge on CCPOSx was due to a noise spike and no action will be triggered (implicit noise filter). If the sampled pattern equals to the next expected pattern the edge on CCPOSx was a correct Hall event, the bit CHE is set which causes an interrupt and the resets T12 (for speed measurement, see description mode '1000' below).

This correct Hall event can be used as a transfer request event for register MCMOUTS. The transfer from MCMOUTS to MCMOUT transfers the new CURH-pattern as well as the next EXPH-pattern. In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive). To restart from IDLE the transfer request of MCMOUTS have to be initiated by software (bit STRHP and bitfields SWSEL/SWSYN).

Below is a table listing output (MCMP) for a BLDC motor.

Block Commutation Control Table

Mode	CCPOS0-CCPOS2 Inputs			CC60 - CC62 Outputs			COUT60 - COUT62 Outputs		
	CCPOS0	CCPOS1	CCPOS2	CC60	CC61	CC62	COUT60	COUT61	COUT62
Rotate left, 0° phase shift	1	0	1	inactive	inactive	active	inactive	active	inactive
	1	0	0	inactive	inactive	active	active	inactive	inactive
	1	1	0	inactive	active	inactive	active	inactive	inactive
	0	1	0	inactive	active	inactive	inactive	inactive	active
	0	1	1	active	inactive	inactive	inactive	inactive	active
	0	0	1	active	inactive	inactive	inactive	active	inactive
Rotate right	1	1	0	active	inactive	inactive	inactive	active	inactive
	1	0	0	active	inactive	inactive	inactive	inactive	active
	1	0	1	inactive	active	inactive	inactive	inactive	active
	0	0	1	inactive	active	inactive	active	inactive	inactive
	0	1	1	inactive	inactive	active	active	inactive	inactive
	0	1	0	inactive	inactive	active	inactive	active	inactive
Slow down	X	X	X	inactive	inactive	inactive	active	active	active
Idle[1)]	X	X	X	inactive	inactive	inactive	inactive	inactive	inactive

[1)] In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive).

Interrupt System

The C868 provides 13 interrupt vectors with four priority levels. Nine interrupt requests are generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial channel, A/D converter, and the capture/compare unit with 4 interrupts) and four interrupts may be triggered externally.

The wake-up from power-down mode interrupt has a special functionality which allows the software power-down mode to be terminated by a short negative pulse at pins CCPOS0/T2/INT0/AN0 or P1.4/RxD.

The 13 interrupt sources are divided into six groups. Each group can be programmed to one of the four interrupt priority levels. Additionally, 4 of these interrupt sources are channeled from 7 Capture/Compare (CCU6) interrupt sources.

Figure 23 to **Figure 28** give a general overview of the interrupt sources and illustrate the request and control flags.

Table 12 Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address(core connections)	Interrupt Request Flags
External Interrupt 0	0003_H(EX0)	IE0
Timer 0 Overflow	$000B_H$(ET0)	TF0
External Interrupt 1	0013_H(EX1)	IE1
Timer 1 Overflow	$001B_H$(ET1)	TF1
Serial Channel	0023_H(ES)	RI / TI
Timer 2 Overflow	$002B_H$(EX5)	TF2
A/D Converter	0033_H(EX6)	IADC
External Interrupt 2	$003B_H$(EX7)	IEX2
External Interrupt 3	0043_H(EX8)	IEX3
	$004B_H$(EX9)	
	0053_H(EX10)	
	$005B_H$(EX11)	
	0063_H(EX12)	
	$006B_H$(EX13)	
CAPCOM interrupt node 0	0083_H(EX14)	INP0[1)]
CAPCOM interrupt node 1	$008B_H$(EX15)	INP1[1)]
CAPCOM interrupt node 2	0093_H(EX16)	INP2[1)]
CAPCOM interrupt node3	$009B_H$(EX17)	INP3[1)]
	$00A3_H$(EX18)	
	$00AB_H$(EX19)	
	$00D3_H$(EX20)	
	$00DB_H$(EX21)	
	$00E3_H$(EX22)	
Wake-up from power-down mode	$007B_H$	–

[1)] Capture/compare has 10 interrupt sources channeled to the 4 interrupt nodes INP0..3. The 3 capture/compare ports has 3 pairs of interrupt request flags, ICC60R, ICC60F, ICC61R, ICC61F, ICC62R, ICC62F. The other flags are T12OM, T12PM, T13CM, T13PM, TRPF, WHE, CHE.

Device Specifications

Absolute Maximum Ratings

Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	-40	125	°C	
Storage temperature	T_{STG}	-65	150	°C	-
Voltage on V_{DDP} pins with respect to ground (V_{SSP})	V_{DDP}	-0.3	4.6	V	-
Voltage on any pin except int/ analog and XTAL with respect to ground (V_{SSP})	V_{IN0}	-0.5	4.6	V	-
Voltage on any int/analog pin with respect to ground (V_{SSP})	V_{IN1}	-0.5	4.6	V	-
Voltage on XTAL pins with respect to ground (V_{SSC})	V_{IN2}	-0.5	4.6	V	-
Input current on any pin during overload condition	I_{OV}	-10	10	mA	-[1)]
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	-	43	mA	-
Power dissipation	P_{DISS}	-	tbd	W	-

1) Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL2 etc.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DDP}$ or $V_{IN}<V_{SSP}$, $V_{IN2}>V_{DDC}$ or $V_{IN2}<V_{SSC}$) the voltage on V_{DDP} pin with respect to ground (V_{SSP}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except XTAL2, int/analog int/analog XTAL2	 V_{IL0} V_{IL1} V_{IL2}	 -0.5 -0.5 -0.5	 $0.3V_{DDP}$ $0.3V_{DDC}$ $0.1V_{DDC}$	 V V V	–[1]
Input high voltages all except XTAL2, int/analog int/analog XTAL2	 V_{IH0} V_{IH1} V_{IH2}	 $0.7V_{DDP}$ $0.7V_{DDC}$ $0.7V_{DDC}$	 V_{DDP}+0.5 V_{DDP}+0.5 V_{DDC}+0.5	 V V V	–
Output low voltage	V_{OL}	–	0.45	V	SAF-C868... I_{OL}=10mA
		–	0.55	V	SAK-C868... I_{OL}=10mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH}=10mA
Input leakage current (all except int/analog)	I_{LI0}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$
Input leakage current (int/ analog)	I_{LI1}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$[2]
Input low current (XTAL2)	I_{LI2}	–	±10	uA	$0.4<V_{IN}<V_{DDC}$
Digital supply voltage	V_{DDC}	2.25[3]	2.75	V	–
Blocking capacitor for V_{DDC}		136	470	nF	–[4]
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A= 25°C

Note:

1) Interrupt/analog pins are input only and has CMOS characteristics whereas the other I/O pins have TTL characteristics.

2) The leakage current of interrupt/analog pins depends on the leakage current of the CMOS pad for the digital functions and the analog pad.

3) The V_{DDC} is measured under the following conditions:

Microcontroller in power down mode;$\overline{\text{RESET}}$ = V_{DDP}; XTAL2 = V_{SSC}; XTAL1 = N.C.; V_{AGND}= V_{SSP}; V_{AREF}= V_{DDP}; RxD/INT0 = V_{DDP}; all other pins are set to input and connected to gnd; ALE output disabled and connected to gnd; 20mA current sourced from the V_{DDC} pin.

4) Ceramic type (±20%) max ESR: 25mΩ ,max trace length to capacitor is 10mm.

Power Supply Current

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[1]	max.[2]		
Active mode	C868-1S	40 MHz[3]	I_{DDP}	13.1	15.6	mA	[4]
	C868-1R	40 MHz[3]	I_{DDP}	13.5	15.5	mA	
Idle mode	C868-1S	40 MHz[3]	I_{DDP}	7.8	9.6	mA	[5]
	C868-1R	40 MHz[3]	I_{DDP}	7.9	9.1	mA	
Active mode with slow-down enabled	C868-1S	40 MHz[3]	I_{DDP}	3.5	4.4	mA	[6]
	C868-1R	40 MHz[3]	I_{DDP}	3.6	4.1	mA	
Idle mode with slow-down enabled	C868-1S	40 MHz[3]	I_{DDP}	3.4	4.2	mA	[7]
	C868-1R	40 MHz[3]	I_{DDP}	3.6	4.1	mA	
Power-down mode	C868-1S		I_{PDP}	240	300	uA	SAF-C868...[8]
				240	400	uA	SAK-C868...[8]
	C868-1R		I_{PDP}	240	300	uA	SAF-C868...[8]
				240	400	uA	SAK-C868...[8]

Note:

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C but not 100% tested.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = – 40 °C and V_{DDP} = 3.6 V).

3) System clock, set by using external clock of 10.67MHz and setting KDIV in CMCON to 010 (factor of 4)

4) I_{DDP} (active mode) is measured with:
XTAL2 driven with t_R, t_F = 5 ns, V_{IL1},V_{IL2} = V_{SSP} + 0.5 V, V_{IH1},V_{IH2} = V_{DDP} – 0.5 V; XTAL1 = N.C.; $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected. ?I_{DDP} would be slightly higher if the crystal oscillator is used (approx. 1 mA).