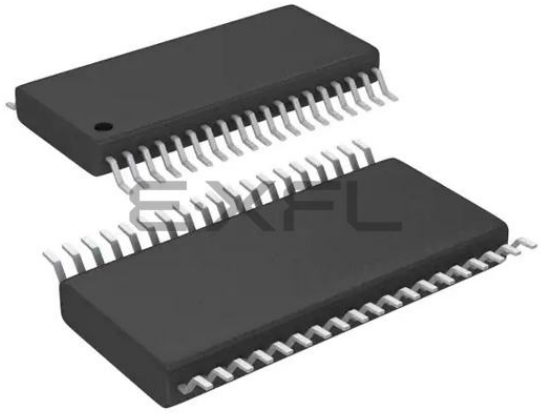

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Details	
Product Status	Obsolete
Core Processor	C800
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	RAM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-c868-1sr-ba

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Previous Version: -

Page	Subjects (major changes since last revision)
	Current data updated
	Description of I2C included

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Table 1 Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-DSO-28	P-TSSOP-38		
P3.0–P3.7	2,3,23, 24,1, 22,5,6	32,33,25, 26,31,24, 36,37	I/O	**Port 3** is an 8-bit push-pull bidirectional I/O port. This port also serves as alternate functions for the CCU6 functions. The functions are assigned to the pins of port 3 as follows :
	2	32		P3.0/COUT63 16 bit compare channel output
	3	33		P3.1/CTRAP CCU trap input
	23	25		P3.2/COUT62 Output of capture/compare ch 2
	24	26		P3.3/CC62 Input/output of capture/compare ch 2
	1	31		P3.4/COUT61 Output of capture/compare ch 1
	22	24		P3.5/CC61 Input/output of capture/compare ch 1
	5	36		P3.6/COUT60 Output of capture/compare ch 0
	6	37		P3.7/CC60 Input/output of capture/compare ch 0
V_{AREF}	19	15	–	**Reference voltage** for the A/D converter.
V_{AGND}	18	14	–	**Reference ground** for the A/D converter.
AN4	21	17	I	**Analog Input Channel 4** is input channel 4 to the ADC unit.
AN3	20	16	I	**Analog Input Channel 3** is input channel 3 to the ADC unit.
$\overline{\text{RESET}}$	7	38	I	**$\overline{\text{RESET}}$** A low level on this pin for two machine cycle while the oscillator is running resets the device.
ALE/BSL	4	34	I/O	**Address Latch Enable/Bootstrap Mode** A low level on this pin during reset allows the device to go into the bootstrap mode. After reset, this pin will output the address latch enable signal. The ALE can be disabled by bit EALE in SFR SYSCON0.
V_{SSP}	14	10	–	**IO Ground** (0V)
V_{DDP}	13	9	–	**IO Power Supply** (+3.3V)

*)I=Input
O=Output

Table 1 Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-DSO-28	**P-TSSOP-38**		
V_{SSC}	25	27	–	**Core Ground** (0V)
V_{DDC}	26	28	O	**Core Internal Reference** (+2.5V) Connect 2*68 - 470nF ceramic capacitor across this pin and core ground.
NC	–	5,7,8,18, 19,20,21, 22,23,35	–	**Not connected**
XTAL1	27	29	I	**XTAL1** Output of the inverting oscillator amplifier.
XTAL2	28	30	O	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generation circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected.

*)I=Input
O=Output

Figure 12 shows the recommended oscillator circuitries for crystal and external clock operation.

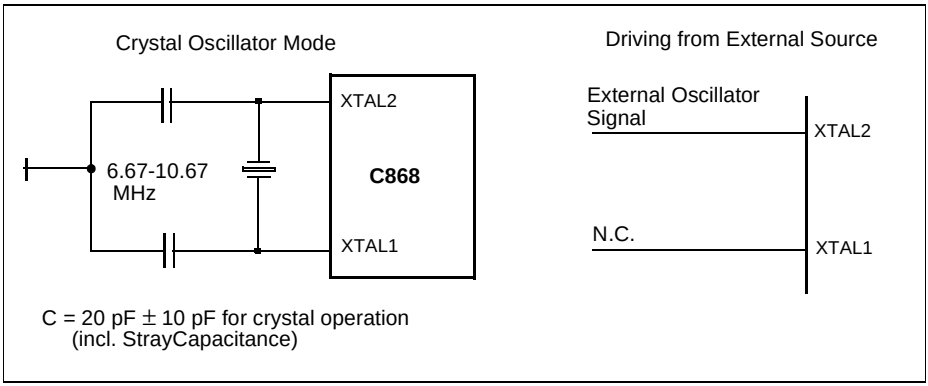


Figure 12 Recommended Oscillator Circuit

In this application the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **Figure 13**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit tbd pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally have different values depending on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.

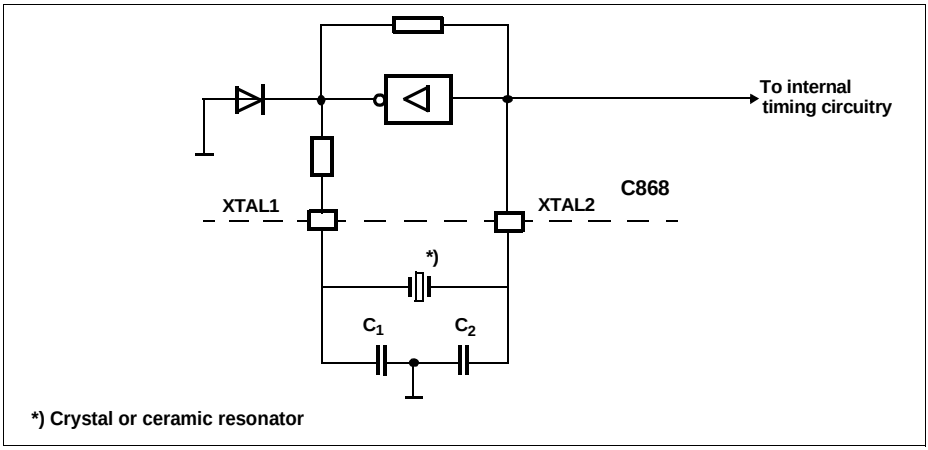


Figure 13 On-Chip Oscillator Circuitry

To drive the C868 with an external clock source, the external clock signal has to be applied to XTAL2, as shown in **Figure 14**. XTAL1 has to be left unconnected. A pullup resistor is suggested (to increase the noise margin), but is optional if V_{OH} of the driving gate corresponds to the V_{IH2} specification of XTAL2.

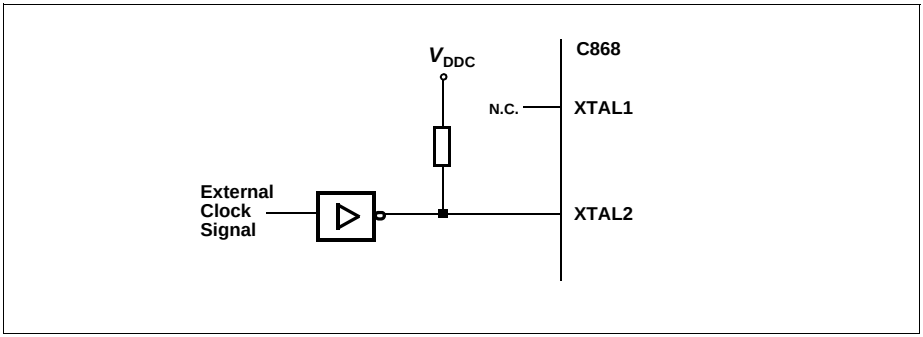


Figure 14 External Clock Source

0.1 Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. For accessing the mapped special function area, bit RMAP in special function register SYSCON0 must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

SYSCON0
System Control Register 0 **[Reset value: XX10XXX1$_B$]**

7	6	5	4	3	2	1	0
-	-	EALE	RMAP	-	-	-	XMAP0
r	r	rw	rw	r	r	r	rw

The functions of the shaded bits are not described here

Field	Bits	Typ	Description
RMAP	4	rw	**Special Function Register Map Control** RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
-	[7:2]	r	**reserved;** returns ’0’ if read; should be written with ’0’;

As long as bit RMAP is set, the mapped special function register area can be accessed. This bit is not cleared automatically by hardware. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

The 109 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All available SFRs whose address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, ..., $F0_H$, $F8_H$) are bit- addressable. Totally there are 128 directly addressable bits within the SFR area.

All SFRs are listed in **Table 6** and **Table 7**.In **Table 6** they are organized in groups which refer to the functional blocks of the C868-1R, C868-1S. **Table 7** illustrates the contents (bits) of the SFRs

Table 6 Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
C800 core	ACC	Accumulator	**$E0_H$**[1]	**00_H**
	B	B-Register	**$F0_H$**[1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	84_H	00_H
	PSW	Program Status Word Register	**$D0_H$**[1]	**00_H**
	SP	Stack Pointer	81_H	07_H
	SCON	Serial Channel Control Register	**98_H**[1]	**00_H**
	SBUF	Serial Data Buffer	99_H	00_H
	IEN0	Interrupt Enable Register 0	**$A8_H$**[1]	**$0X000000_B$**[2]
	IEN1	Interrupt Enable Register 1	$A9_H$	$XXXXX000_B$[2]
	IEN2	Interrupt Enable Register 2	AA_H	$XX0000XX_B$[2]
	IP0	Interrupt Priority Register 0	**$B8_H$**[1]	**$XX000000_B$**[2]
	IP1	interrupt Priority Register 1	AC_H	$XX000000_B$[2]
	TCON	Timer 0/1 Control Register	**88_H**[1]	**00_H**
	TMOD	Timer Mode Register	89_H	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	PCON	Power Control Register	87_H	$0XXX0000_B$[2]
System	PMCON0	Wake-up Control Register	$8E_H$	$XXX00000_B$[2]
	CMCON	Clock Control Register	$8F_H$	10011111_B
	EXICON	External Interrupt Control Register	91_H	$XXXXXX00_B$[2]
	IRCON0	External Interrupt Request Register	92_H	$XXXXXX00_B$[2]
	IRCON1	Peripheral Interrupt Request Register	93_H	$XX0000X0_B$[2]
	PMCON1	Peripheral Management Ctrl Register	**$E8_H$**[1]	**$XXXXX000_B$**[2]
	PMCON2	Peripheral Management Status Register	**$F8_H$**[1]	**$XXXXX000_B$**[2]
	SCUWDT	SCU/Watchdog Control Register	**$C0_H$**[1]	**$X0X00000_B$**[2]
	VERSION	ROM Version Register	$F9_H$	00_H
	SYSCON0	System Control Register 0	AD_H	$XX10XXX1_B$[2]
	SYSCON1	System Control Register 1	AF_H	$00XXX0X0_B$[2]

1) Bit-addressable special function registers
2) “X“ means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

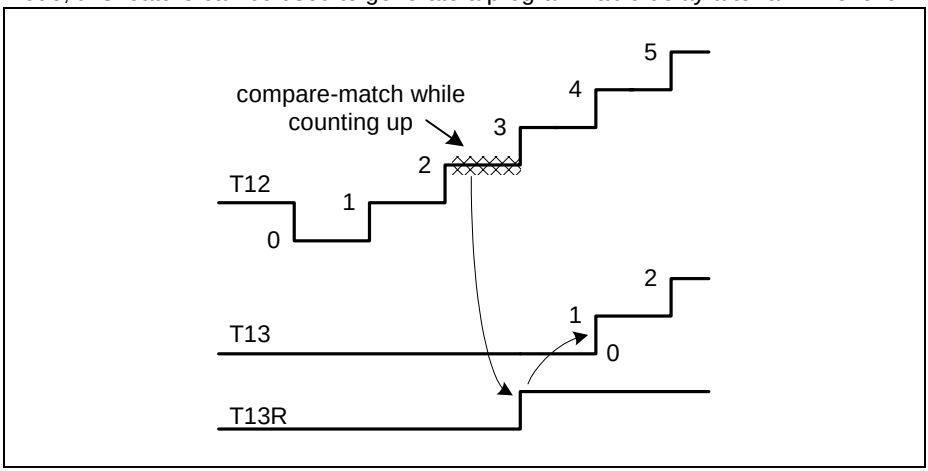
Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$C6_H$	CC62RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CC62RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	XXXXXXX0$_B$	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CE_H	TRPCTRL	00_H	–	–	–	–	–	TRPM2	TRPM1	TRPM0
CF_H	TRPCTRH	00_H	TRPPEN	TRPEN13	TRPEN5	TRPEN4	TRPEN3	TRPEN2	TRPEN1	TRPEN0
$D0_H$	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	T13PRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D3_H$	T13PRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D4_H$	CC63RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CC63RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D6_H$[2)]	MCMCTRLL	00_H	–	–	SWSYN1	SWSYN0	–	SWSEL2	SWSEL1	SWSEL0
$D6_H$[3)]	MODCTRL	00_H	MCMEN	–	T12MODEN5	T12MODEN4	T12MODEN3	T12MODEN2	T12MODEN1	T12MODEN0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Synchronization of T13 to T12

The timer T13 can be synchronized on a T12 event. Combined with the single shot mode, this feature can be used to generate a programmable delay after a T12 event.



Synchronization of T13 to T12

Multi-channel Mode

The multi-channel mode offers a possibility to modulate all six T12-related output signals within one instruction. The bits in bit field MCMP are used to select the outputs that may become active. If the multi-channel mode is enabled (bit MCMEN='1'), only those outputs may become active, which have a '1' at the corresponding bit position in bit field MCMP.

This bit field has its own shadow bit field MCMPS, which can be written by SW. The transfer of the new value in MCMPS to the bit field MCMP can be triggered by and synchronized to T12 or T13 events. This structure permits the SW to write the new value, which is then taken into account by the HW at a well-defined moment and synchronized to a PWM period. This avoids unintended pulses due to unsynchronized modulation sources (T12, T13, SW).

Hall Sensor Mode

In **Brushless-DC motors** the next multi-channel state values depend on the pattern of the Hall inputs. There is a strong correlation between the **Hall pattern** (CURH) and the **modulation pattern** (MCMP). Because of different machine types the modulation pattern for driving the motor can be different. Therefore it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding modulation pattern. The CCU6 offers this by having a register which contains the actual Hall pattern (CURHS), the next expected Hall pattern (EXPHS) and its output pattern (MCMPS). At every correct Hall event (CHE, see figure *Hall Event Actions*) a new Hall pattern with its corresponding output pattern can be loaded (from a predefined table) by software into the register MCMOUTS. Loading this shadow register can also be done by a write action on MCMOUTS with bit STRHP = '1'

The **sampling** of the Hall pattern (on CCPOSx) is done with the T12 clock. By using the dead-time counter DTC0 (mode MSEL6x= '1000') a hardware **noise filter** can be implemented to suppress spikes on the Hall inputs due to high di/dt in rugged inverter environment. In case of a Hall event the DTC0 is reloaded and starts counting. When the counter value of one is reached, the CCPOSx inputs are sampled (without noise and spikes) and are compared to the current Hall pattern (CURH) and to the expected Hall pattern (EXPH). If the sampled pattern equals to the current pattern the edge on CCPOSx was due to a noise spike and no action will be triggered (implicit noise filter). If the sampled pattern equals to the next expected pattern the edge on CCPOSx was a correct Hall event, the bit CHE is set which causes an interrupt and the resets T12 (for speed measurement, see description mode '1000' below).

This correct Hall event can be used as a transfer request event for register MCMOUTS. The transfer from MCMOUTS to MCMOUT transfers the new CURH-pattern as well as the next EXPH-pattern. In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive). To restart from IDLE the transfer request of MCMOUTS have to be initiated by software (bit STRHP and bitfields SWSEL/SWSYN).

For **Brushless-DC** motors there is a special mode (MSEL6x = ’1000b’) which is triggered by a change of the Hall-inputs (CCPOSx). This mode shows the capabilities of the CCU6. Here T12’s channel 0 acts in capture function, channel 1 and 2 in compare function (without output modulation) and the multi-channel-block is used to trigger the output switching together with a possible modulation of T13.
After the detection of a valid Hall edge the T12 count value is captured to channel 0 (representing the actual motor speed) and resets the T12. When the timer reaches the compare value in channel 1, the next multi-channel state is switched by triggering the shadow transfer of bit field MCMP (if enabled in bit field SWEN). This trigger event can be combined with several conditions which are necessary to implement a noise filtering (correct Hall event) and to synchronize the next multi-channel state to the modulation sources (avoiding spikes on the output lines). This compare function of channel 1 can be used as a phase delay for the position input to the output switching which is necessary if a sensorless back-EMF technique is used instead of Hall sensors. The compare value in channel 2 can be used as a time-out trigger (interrupt) indicating that the motors destination speed is far below the desired value which can be caused by a abnormal load change. In this mode the modulation of T12 has to be disabled (T12MODENx = ’0’).

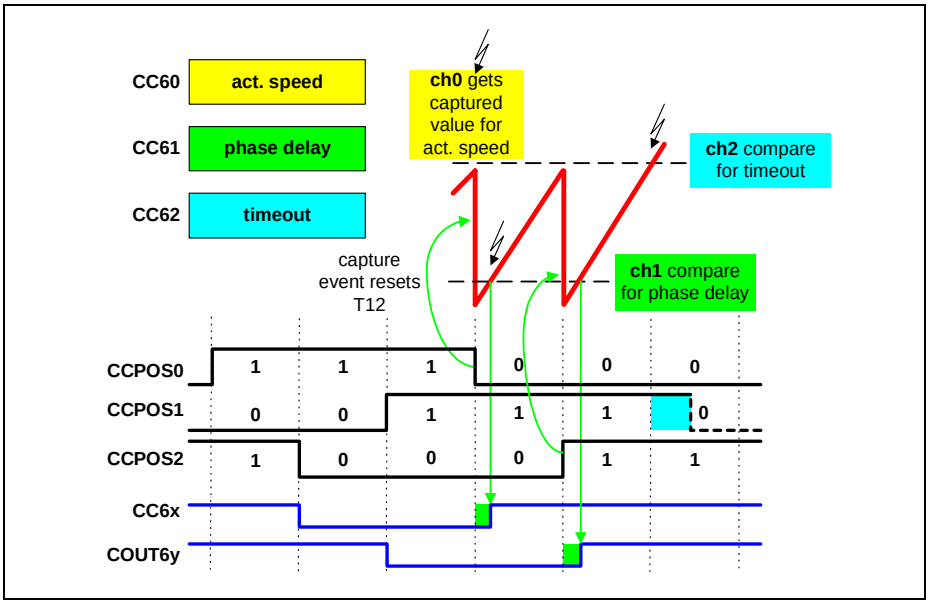


Figure 0-2 Timer T12 Brushless-DC Mode (MSEL6x = 1000)

Interrupt System

The C868 provides 13 interrupt vectors with four priority levels. Nine interrupt requests are generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial channel, A/D converter, and the capture/compare unit with 4 interrupts) and four interrupts may be triggered externally.

The wake-up from power-down mode interrupt has a special functionality which allows the software power-down mode to be terminated by a short negative pulse at pins CCPOS0/T2/INT0/AN0 or P1.4/RxD.

The 13 interrupt sources are divided into six groups. Each group can be programmed to one of the four interrupt priority levels. Additionally, 4 of these interrupt sources are channeled from 7 Capture/Compare (CCU6) interrupt sources.

Figure 23 to **Figure 28** give a general overview of the interrupt sources and illustrate the request and control flags.

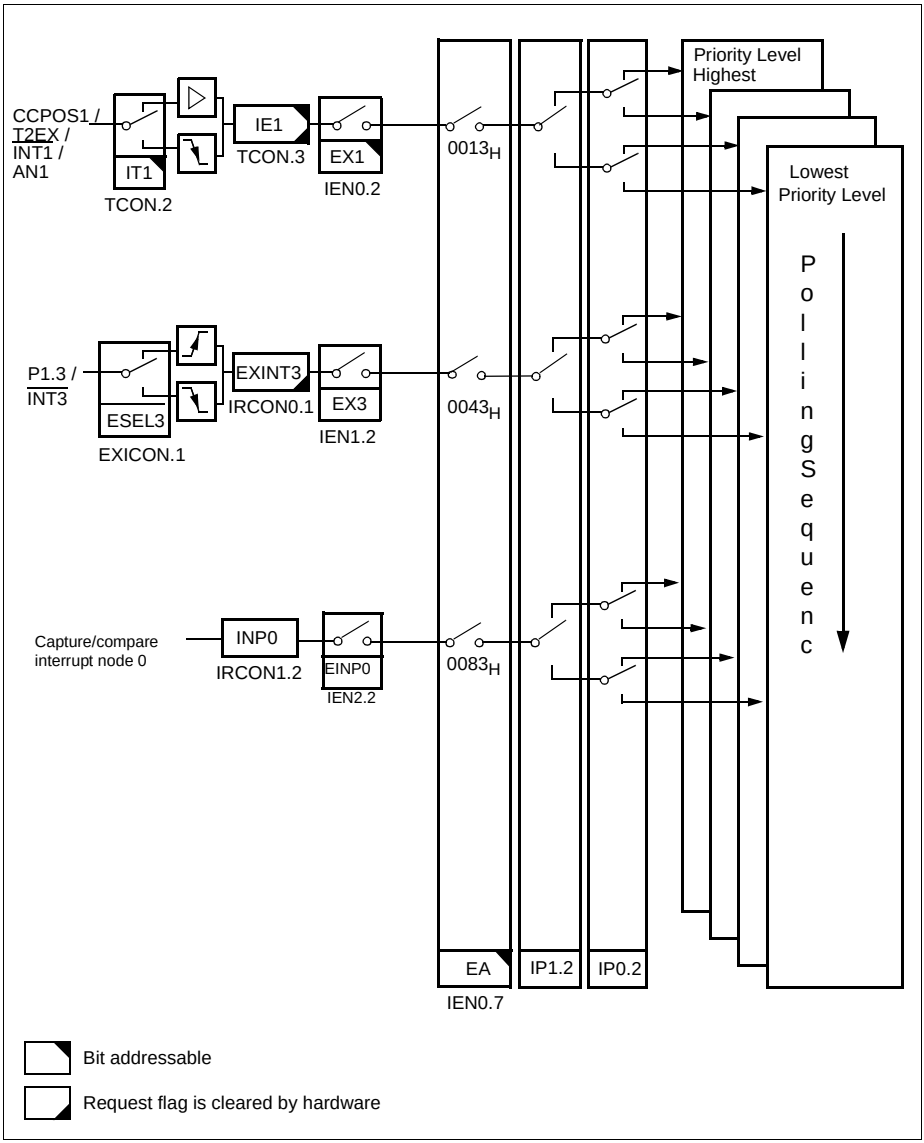


Figure 25 Interrupt Structure, Overview Part 2

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is to be serviced first. Thus, within each priority level there is a second priority structure determined by the polling sequence. This is illustrated in **Table 13**

.

Table 13 Interrupt Source Structure

Interrupt Group	Priority Bits of Interrupt Group	Interrupt Source Priority High Priority → Low Priority				Priority
0	IP0.0	EXINT0	IADC			High
1	IP0.1	TF0	EXINT2			↓
2	IP0.2	EXINT1	EXINT3	INP0[1)]		
3	IP0.3	TF1		INP1[1)]		
4	IP0.4	RI + TI		INP2[1)]		
5	IP0.5	TF2		INP3[1)]		Low

1) Capture/compare has 10 interrupt sources channeled to the 4 interrupt nodes INP0..3. The 3 capture/compare ports has 3 pairs of interrupt request flags, ICC60R, ICC60F, ICC61R, ICC61F, ICC62R, ICC62F. The other flags are T12OM, T12PM, T13CM, T13PM, TRPF, WHE, CHE.

Within a column, the topmost interrupt is serviced first, then the second and the third, when available. The interrupt groups are serviced from left to right of the table. A low-priority interrupt can itself be interrupted by a higher-priority interrupt, but not by another interrupt of the same or a lower priority. An interrupt of the highest priority level cannot be interrupted by another interrupt source.

SFR SCUWDT) consecutively. This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes"). It is not possible to use the idle mode in combination with the watchdog timer function. Therefore, even the watchdog timer cannot reset the device when one of the power saving modes has been entered accidentally.

The time period for an overflow of the Watchdog Timer is programmable in two ways :

- **the input frequency** to the Watchdog Timer can be selected via bit WDTIN in register WDTCON to be either $f_{SYS}/2$ or $f_{SYS}/128$.
- **the reload value** WDTREL for the high byte of WDT can be programmed in register WDTCON.

The period P_{WDT} between servicing the Watchdog Timer and the next overflow can therefore be determined by the following formula:

[0.1]

$$P_{WDT} = \frac{2^{(1 + WDTIN*6)} * (2^{16} - WDTREL * 2^{8})}{f_{SYS}}$$

Table 14 lists the possible ranges for the watchdog time which can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 14 Watchdog Time Ranges

Reload value in WDTREL	Prescaler for f_{SYS}					
	2 (WDTIN = '0')			128 (WDTIN = '1')		
	40 MHz	20 MHz	16 MHz	40 MHz	20 MHz	16 MHz
FF_H	12.8 µs	25.6 µs	32.0 µs	819.2 µs	1.64 ms	2.05 ms
$7F_H$	1.65 ms	3.3 ms	4.13 ms	105.7 ms	211.3 ms	264 ms
00_H	3.28 ms	6.55 ms	8.19 ms	209.7 ms	419.4 ms	524 ms

For safety reasons, the user is advised to rewrite WDTCON each time before the Watchdog Timer is serviced.

Device Specifications

Absolute Maximum Ratings

Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	-40	125	°C	
Storage temperature	T_{STG}	-65	150	°C	-
Voltage on V_{DDP} pins with respect to ground (V_{SSP})	V_{DDP}	-0.3	4.6	V	-
Voltage on any pin except int/ analog and XTAL with respect to ground (V_{SSP})	V_{IN0}	-0.5	4.6	V	-
Voltage on any int/analog pin with respect to ground (V_{SSP})	V_{IN1}	-0.5	4.6	V	-
Voltage on XTAL pins with respect to ground (V_{SSC})	V_{IN2}	-0.5	4.6	V	-
Input current on any pin during overload condition	I_{OV}	-10	10	mA	-[1)]
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	-	43	mA	-
Power dissipation	P_{DISS}	-	tbd	W	-

1) Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL2 etc.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DDP}$ or $V_{IN}<V_{SSP}$, $V_{IN2}>V_{DDC}$ or $V_{IN2}<V_{SSC}$) the voltage on V_{DDP} pin with respect to ground (V_{SSP}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C868. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DDP}	3.0	3.6	V	Active mode, f_{SYSmax} = 40 MHz
		tbd	3.6	V	PowerDown mode[1]
Digital ground voltages	V_{SSC}, V_{SSP}	0		V	-
Ambient temperature	T_A	-40	85	°C	SAF-C868...
		-40	125	°C	SAK-C868...
Analog reference voltage	V_{AREF}	3.0V	V_{DDP} + 0.1	V	-
Analog ground voltage	V_{AGND}	V_{SSP} - 0.1	V_{SSP} + 0.1	V	-
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	-
External Clock	f_{OSC}	6.67	10.67	MHz	-
Input current on any pin during overload condition except int/ analog and XTAL	I_{OV0}	-5	5	mA	-[2)3)]
int/analog pin	I_{OV1}	-2	5	mA	-[3)4)]
XTAL pin	I_{OV2}	-5	5	mA	-[3)5)]
Absolute sum of all input currents during overload condition	ΣI_{OV}	-	|20|	mA	-[3)]

Notes:

1) Oscillator or external clock disabled.

2) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DDP}$ +0.5V or $V_{OV} < V_{SSP}$ -0.5V). The absolute sum of input currents on all port pins may not exceed 20mA. The suply voltages V_{DDP} and V_{SSP} must remain within the specified limits.

3) Not 100% tested, but guaranteed by design characterization.

AC Characteristics

(Operating Condition Apply)

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Ext Clock 6.67 to 10.67 MHz		
		min	max	
Oscillating period	t_{OSC}	93.75	150	ns
High time	t_1	46.875	75	ns
Low time	t_2	46.875	75	ns
Rise time	t_R	-	10	ns
Fall time	t_F	-	10	ns

ALE Characteristics

Parameter	Symbol	Limit Values		Unit
		System freq = 6.25MHz to 40MHz Duty Cycle 0.5		
		min	max	
ALE pulse width	t_{AWD}	50	320	ns
ALE period	t_{ACY}	150	960	ns

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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