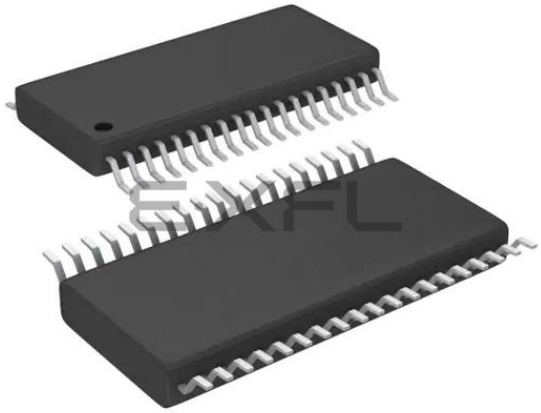

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C800
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	RAM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-c868p-1sr-ba

CPU

The C868 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 10.67 MHz external crystal (giving a 40MHz CPU clock), 58% of the instructions execute in 300 ns.

PSW

Program Status Word Register **[Reset value: 00_H]**

$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$
CY	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**
rwh	rwh	rw	rw	rw	rwh	rw	rwh

Field	Bits	Typ	Description
P	0	rwh	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.
F1	1	rw	**General Purpose Flag**
OV	2	rwh	**Overflow Flag** Used by arithmetic instructions.
RS0 **RS1**	3 4	rw	**Register Bank select control bits** These bits are used to select one of the four register banks. **Table 2 :** **RS1** / **RS0** / **Function** 0 / 0 / Bank 0 selected, data address 00_H-07_H 0 / 1 / Bank 1 selected, data address 08_H-$0F_H$ 1 / 0 / Bank 2 selected, data address 10_H-17_H 1 / 1 / Bank 3 selected, data address 18_H-$1F_H$
F0	5	rw	**General Purpose Flag**
AC	6	rwh	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
CY	7	rwh	**Carry Flag** Used by arithmetic instructions.

The various chip modes supported are shown in **Figure 6**.

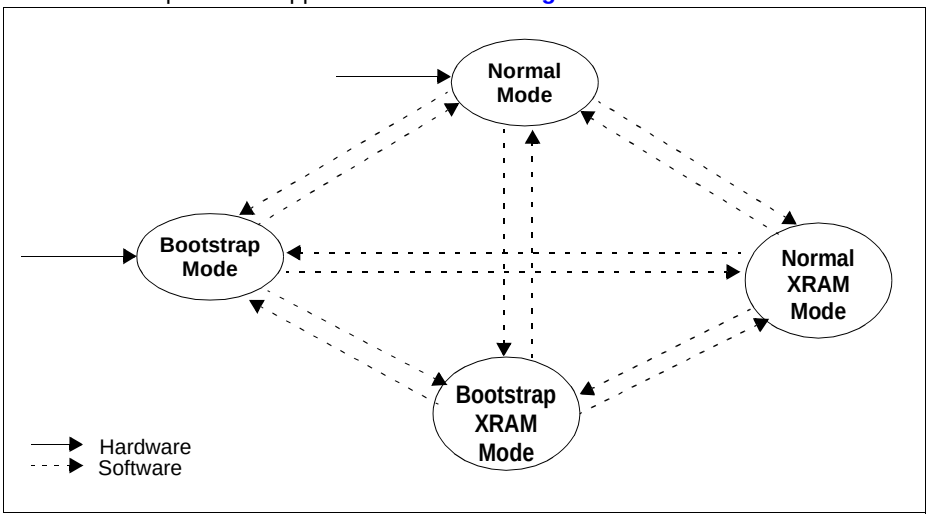


Figure 6 Entry and exit of Chip Modes

A valid hardware reset would, of course, override any of the above entry or exit procedures.

Table 0-1 Hardware and Software Selection of Chipmodes

Operating Mode (Chipmode)	Hardware Selection	Software Selection
Normal Mode	ALE/BSL pin = high RESET rising edge	ALE/BSL = don't care; setting bits BSLEN, SWAP = 0,0; execute unlocking sequence
Normal XRAM Mode	Not possible	setting bits BSLEN,SWAP = 0,1; execute unlocking sequence
Bootstrap XRAM Mode	Not possible	setting bits BSLEN,SWAP = 1,1; execute unlocking sequence
Bootstrap Mode	ALE/BSL pin = low RESET rising edge	ALE/BSL = don't care; setting bits BSLEN, SWAP = 1,0; execute unlocking sequence

Bootstrap loader

The C868, includes a bootstrap mode, which is activated by setting the ALE/BSL pin at logic low with a pulldown and TxD pin at logic high with a pullup at the rising edge of the RESET. Or it can be entered by software, that is by setting BSLEN bit and resetting SWAP bit in SFR SYSCON1 accompany by an unlock sequence.

In the bootstrap mode, software routines of the bootstrap loader located in the boot ROM will be executed. Its purpose is to allow the easy and quick programming of the internal SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ to $FFFF_H$) via serial interface (UART) while the MCU is in-circuit. It also provides a way to program SRAM or XRAM through bootstrapping from an external SPI or I2C EEPROM.

The first action of the bootstrap loader is to detect the presence of EEPROM and its type, SPI or I2C, and check the first byte of the serial EEPROM. If the first byte is $0A5_H$, the MCU would enter Phase A to download from the EEPROM. Otherwise, it will enter Phase B to establish a serial communication with the connected host. Bootstrapping from the serial EEPROM can also be done in phase B if it is invoked by the host.

Phase B consists of two functional parts that represent two phases:

- Phase I: Establish a serial connection and automatically synchronize to the transfer speed (baud rate) of the serial communication partner (host).
- Phase II: Perform the serial communication with the host. The host controls the communication by sending special header information, which select one of the working modes. These modes are:

Table 4 Serial Communication Modes of Phase B

Modes	Description
0	Transfer a customer program from the host to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
1	Execute a customer program in the XRAM at start address $FF00_H$.
2	Execute a customer program in the SRAM at start address 0000_H.
3	Transfer a customer program from the SPI EEPROM to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
4	Transfer a customer program from the I2C EEPROM to the SRAM (0000_H to $1FFF_H$) or XRAM ($FF00_H$ -$FFFF_H$). Then return to the beginning of phase II and wait for the next command from the host.
5-9	reserved

The phases of the bootstrap loader are illustrated in **Figure 7**.

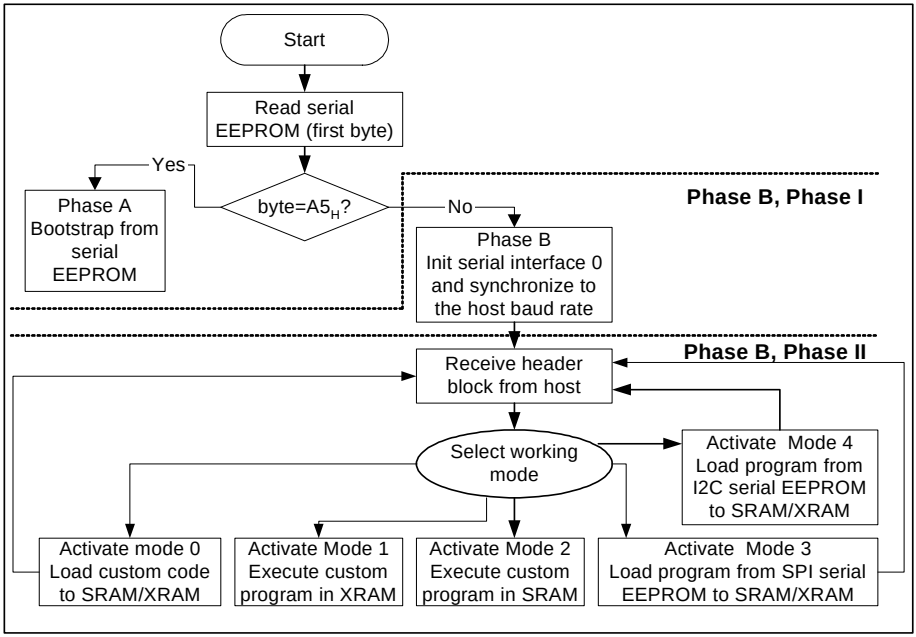


Figure 7 The phases of the Bootstrap Loader

The serial communication is activated in phase B. Using a full duplex serial cable (RS232), the MCU must be connected to the serial port of the host computer as shown in **Figure 8**.

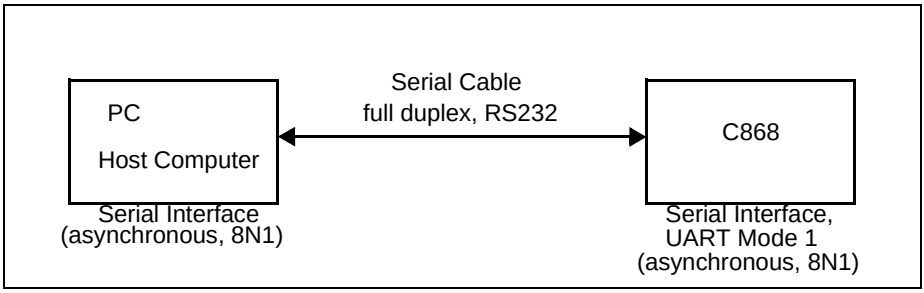


Figure 8 Bootstrap Loader Interface to the PC

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
84_H	DPSEL	00_H	–	–	–	–	–	D2	D1	D0
87_H	PCON	$0XX0\ 0000_B$	SMOD	–	–	SD	GF1	GF0	PDE	IDLE
88_H	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	00_H	GATE 1	C/NT1	M1(1)	M0(1)	GATE 0	C/NT0	M1(0)	M0(0)
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8E_H$	PMCON0	$XXX0\ 0000_B$	–	–	–	EBO	BO	SDSTAT	WS	EPWD
$8F_H$	CMCON	$1001\ 1111_B$	KDIV2	KDIV1	KDIV0	REL4	REL3	REL2	REL1	REL0
90_H[2)]	P1	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[3)]	P1DIR	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
91_H	EXICON	$XXXX\ XX00_B$	–	–	–	–	–	–	ESEL3	ESEL2
92_H	IRCON0	$XXXX\ XX00_B$	–	–	–	–	–	–	EXINT3	EXINT2
93_H	IRCON1	$XX00\ 00X0_B$	–	–	INP3	INP2	INP1	INP0	–	IADC
98_H	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$C6_H$	CC62RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CC62RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	XXXX XXX0_B	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CE_H	TRPCTRL	00_H	–	–	–	–	–	TRPM2	TRPM1	TRPM0
CF_H	TRPCTRH	00_H	TRPPEN	TRPEN13	TRPEN5	TRPEN4	TRPEN3	TRPEN2	TRPEN1	TRPEN0
$D0_H$	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	T13PRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D3_H$	T13PRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D4_H$	CC63RL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CC63RH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D6_H$[2)]	MCMCTRLL	00_H	–	–	SWSYN1	SWSYN0	–	SWSEL2	SWSEL1	SWSEL0
$D6_H$[3)]	MODCTRL	00_H	MCMEN	–	T12MODEN5	T12MODEN4	T12MODEN3	T12MODEN2	T12MODEN1	T12MODEN0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$E6_H$	T12DTCL	00_H		–	DTM5	DTM4	DTM3	DTM2	DTM1	DTM0
$E7_H$	T12DTCH	00_H	–	DTR2	DTR1	DTR0	–	DTE2	DTE1	DTE0
$E8_H$	PMCON1	$XXXX\ X000_B$	–	–	–	–	–	CCUDIS	T2DIS	ADCDIS
EA_H	CMPMODIFL	00_H	–	MCC63S	–	–	–	MCC62S	MCC61S	MCC60S
EB_H	CMPMODIFH	00_H	–	MCC63R	–	–	–	MCC62R	MCC61R	MCC60R
EC_H	T12L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
ED_H	T12H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EE_H	T13L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EF_H	T13H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F2_H$[2)]	TCTR4L	00_H	T12STD	T12STR	–	–	DTRES	T12RES	T12RS	T12RR
$F2_H$[3)]	TCTR2L	00_H	–	T13TED1	T13TED0	T13TEC2	T13TEC1	T13TEC0	T13SSC	T12SSC
$F3_H$[2)]	TCTR4H	00_H	T13STD	T13STR	–	–	–	T13RES	T13RS	T13RR
$F4_H$	CMPSTATL	00_H	–	CC63ST	–	–	–	CC62ST	CC61ST	CC60ST
$F5_H$	CMPSTATH	00_H	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
$F6_H$	T12MSELL	00_H	MSEL613	MSEL612	MSEL611	MSEL610	MSEL603	MSEL602	MSEL601	MSEL600
$F7_H$	T12MSELH	00_H	–	–	–	–	MSEL623	MSEL622	MSEL621	MSEL620

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Timer 0 and 1

Timer 0 and 1 can be used in four operating modes as listed in **Table 8**:

Table 8 Timer 0 and 1 Operating Modes

Mode	Description	TMOD		System Clock
		M1	M0	
0	8-bit timer with a divide-by-32 prescaler	0	0	f_{SYS}/(12*32)
1	16-bit timer	0	1	f_{SYS}/12
2	8-bit timer with 8-bit autoreload	1	0	
3	Timer 0 used as one 8-bit timer and one 8-bit timer timer 1 stops	1	1	

The register is incremented every machine cycle. Since the machine cycle consist of twelve oscillator periods, the count rate is 1/12th of the system frequency. External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate to facilitate pulse width measurements. **Figure 15** illustrates the input clock logic.

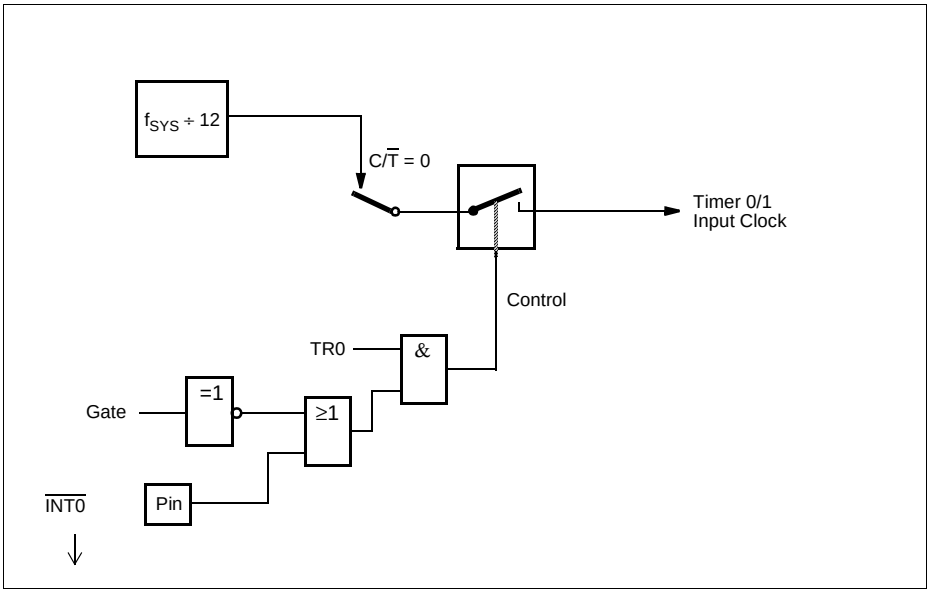


Figure 15 Timer 0 and 1 Input Clock Logic

Timer/Counter 2 with Compare/Capture/Capture

Timer 2 is a 16-bit timer/counter with an up/down count feature. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator

Table 9 Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	T2EX	Remarks	System Clock	
	RCLK or TCLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN			Inte-rnal	T2
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{SYS} /12	max f_{SYS} /24
	0	0	X	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	down counting		
	0	0	1	1	X	1	up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	f_{SYS} /12	max f_{SYS} /24
	0	1	1	X	1	↓	capture T2H,T2L-> RC2H,RC2L		
Baudrate Generator	1	X	1	X	0	X	no overflow interrupt request(TF2)	f_{SYS} /2	-
	1	X	1	X	1	↓	extra external interrupt (“Timer 2“)		
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note: denotes a falling edge

Serial Interface (UART)

The serial port is a full duplex port capable of simultaneous transmit and receive functions. It is also receive-buffered; it can commence reception of a second byte before a previously-received byte has been read from the receive register. The serial port can operate in 3 modes as illustrated in **Table 10**.

Table 10 UART Operating Modes

Mode	SCON		Description
	SM1	SM0	
0	0	0	Reserved
1	0	1	8-bit UART, variable baudrate 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	9-bit UART, fixed baudrate 11 bits are transmitted (through TxD) or received (RxD)
3	1	1	9-bit UART, variable baudrate Similar to mode 2, except for the variable baudrate.

For clarification, some terms regarding the difference between “baudrate clock“ and “baudrate“ should be mentioned.

The serial interface requires a clock rate which is 16 times the baudrate for internal synchronization. Therefore, the baudrate generators must provide a “baudrate clock“ to the serial interface which divides it by 16, thereby resulting in the actual “baudrate“.

The baudrates in Mode 1 and 3 are determined by the timer overflow rate. These baudrates can be determined by Timer 1 or by Timer 2 or both (one for transmit, the other for receive.

Table 11 Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	TCLK/ RCLK	SMOD	
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	x	Controlled by timer 1 overflow: ($2^{SMOD} \times$ Timer 1 overflow rate) / 32
	1	x	Controlled by baud rate generator ($2^{SMOD} \times$ Timer 2[1)] overflow rate) / 32
Mode 2 (9-bit UART)	–	0	f_{SYS} / 64
		1	f_{SYS} / 32

1) Timer 2 functioning as baudrate generator

Switching Examples

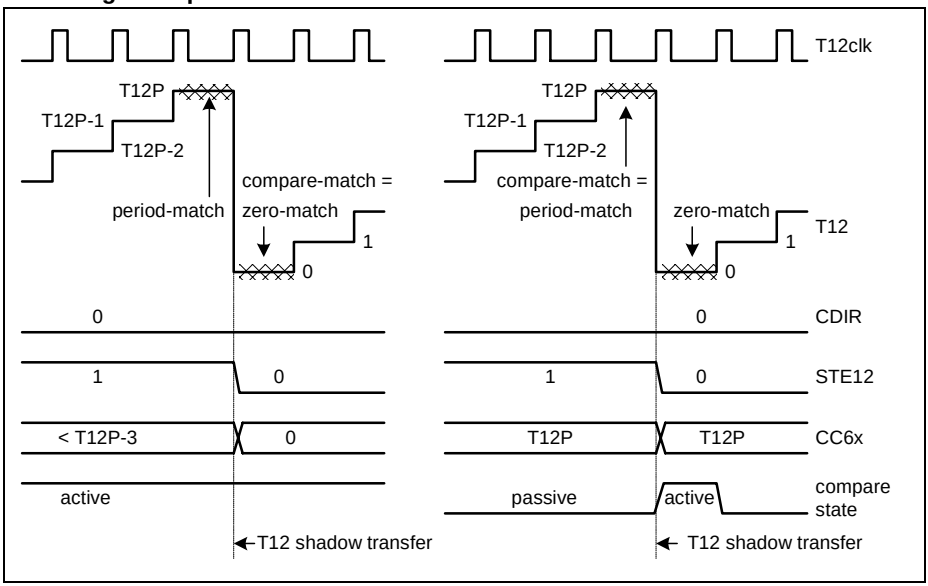


Figure 16 Edge-aligned mode with duty cycles near 100% and near 0%. Applicable to T13 as well.

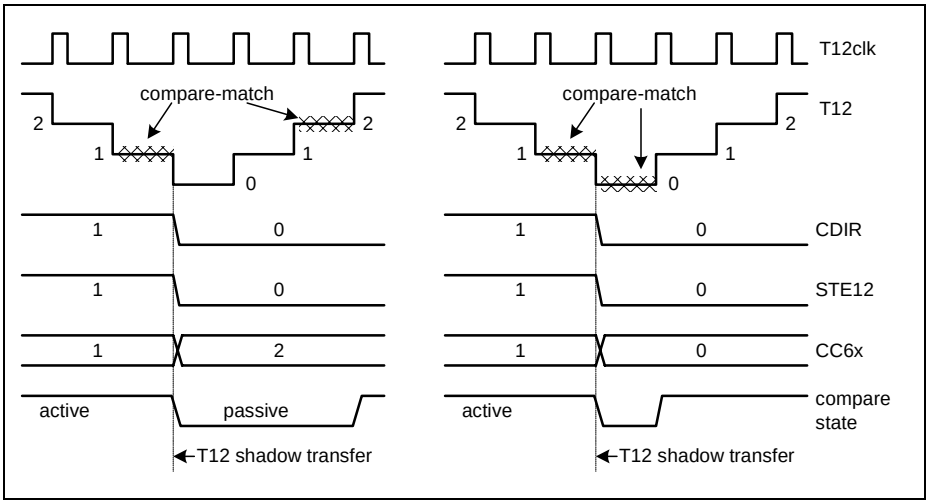
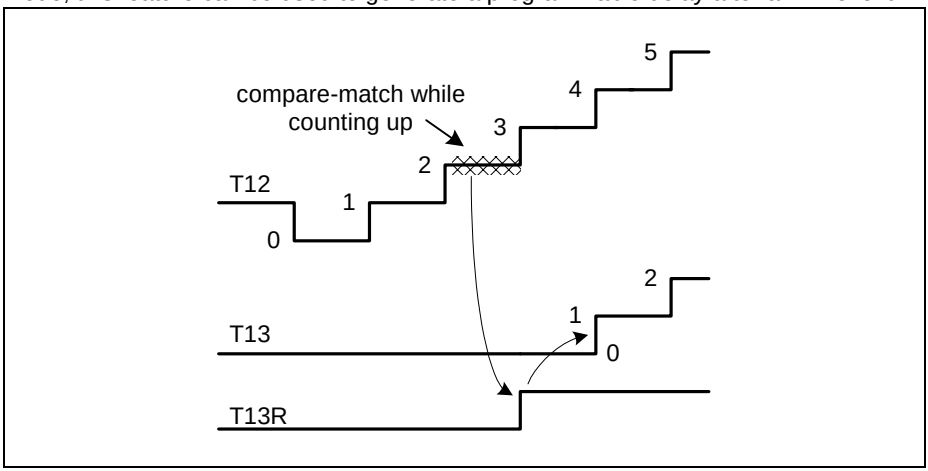


Figure 17 Centre-aligned mode with duty cycles near 100% and near 0%.

Synchronization of T13 to T12

The timer T13 can be synchronized on a T12 event. Combined with the single shot mode, this feature can be used to generate a programmable delay after a T12 event.



Synchronization of T13 to T12

Multi-channel Mode

The multi-channel mode offers a possibility to modulate all six T12-related output signals within one instruction. The bits in bit field MCMP are used to select the outputs that may become active. If the multi-channel mode is enabled (bit MCMEN='1'), only those outputs may become active, which have a '1' at the corresponding bit position in bit field MCMP.

This bit field has its own shadow bit field MCMPS, which can be written by SW. The transfer of the new value in MCMPS to the bit field MCMP can be triggered by and synchronized to T12 or T13 events. This structure permits the SW to write the new value, which is then taken into account by the HW at a well-defined moment and synchronized to a PWM period. This avoids unintended pulses due to unsynchronized modulation sources (T12, T13, SW).

Trap Handling

The trap functionality permits the PWM outputs to react on the state of the input pin CTRAP. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. as emergency stop).

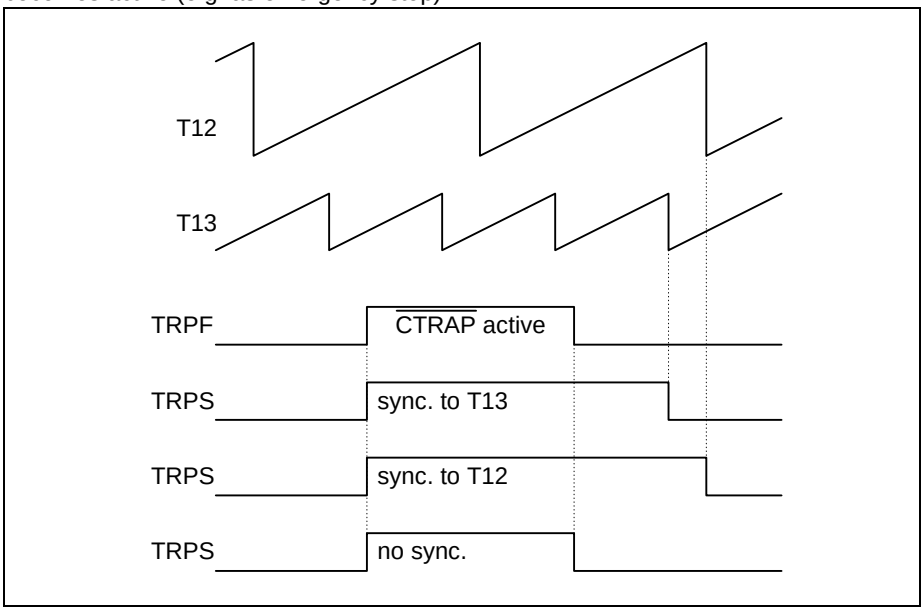


Figure 21 Trap State Synchronization (with TRM2='0')

Modulation control

The modulation control part combines the different modulation sources, six T12-related signals from the three compare channels, the T13-related signal and the multi-channel modulation signals. each modulation source can be individually enabled for each output line. Furthermore, the trap functionality is taken into account to disable the modulation of the corresponding output line during the trap state (if enabled).

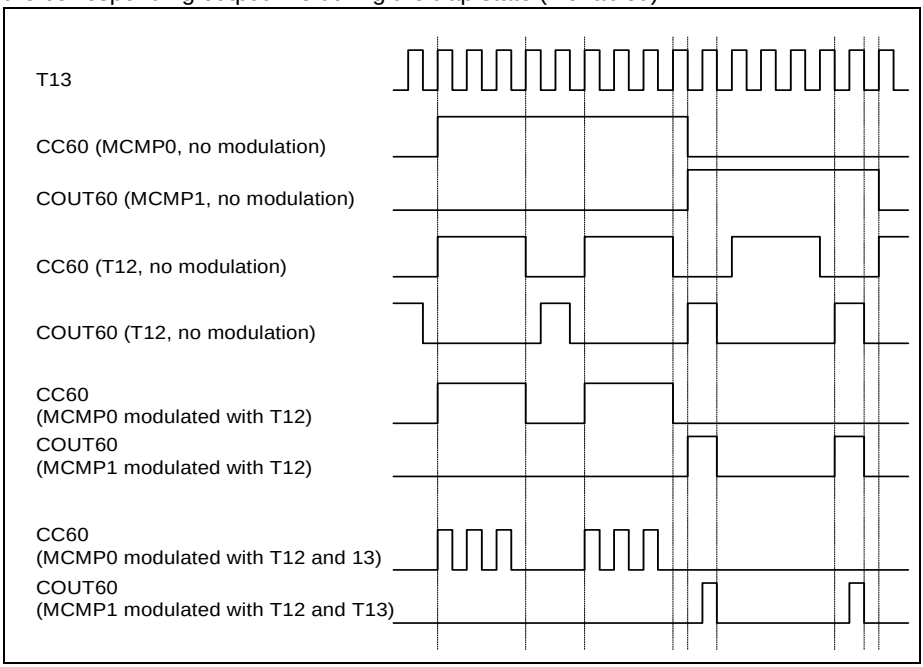


Figure 22 Modulation Control example for CC60 and COUT60.

Interrupt System

The C868 provides 13 interrupt vectors with four priority levels. Nine interrupt requests are generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial channel, A/D converter, and the capture/compare unit with 4 interrupts) and four interrupts may be triggered externally.

The wake-up from power-down mode interrupt has a special functionality which allows the software power-down mode to be terminated by a short negative pulse at pins CCPOS0/T2/INT0/AN0 or P1.4/RxD.

The 13 interrupt sources are divided into six groups. Each group can be programmed to one of the four interrupt priority levels. Additionally, 4 of these interrupt sources are channeled from 7 Capture/Compare (CCU6) interrupt sources.

Figure 23 to **Figure 28** give a general overview of the interrupt sources and illustrate the request and control flags.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is to be serviced first. Thus, within each priority level there is a second priority structure determined by the polling sequence. This is illustrated in **Table 13**

.

Table 13 Interrupt Source Structure

Interrupt Group	Priority Bits of Interrupt Group	Interrupt Source Priority High Priority → Low Priority				Priority
0	IP0.0	EXINT0	IADC			High
1	IP0.1	TF0	EXINT2			↓
2	IP0.2	EXINT1	EXINT3	INP0[1)]		
3	IP0.3	TF1		INP1[1)]		
4	IP0.4	RI + TI		INP2[1)]		
5	IP0.5	TF2		INP3[1)]		Low

1) Capture/compare has 10 interrupt sources channeled to the 4 interrupt nodes INP0..3. The 3 capture/compare ports has 3 pairs of interrupt request flags, ICC60R, ICC60F, ICC61R, ICC61F, ICC62R, ICC62F. The other flags are T12OM, T12PM, T13CM, T13PM, TRPF, WHE, CHE.

Within a column, the topmost interrupt is serviced first, then the second and the third, when available. The interrupt groups are serviced from left to right of the table. A low-priority interrupt can itself be interrupted by a higher-priority interrupt, but not by another interrupt of the same or a lower priority. An interrupt of the highest priority level cannot be interrupted by another interrupt source.

Device Specifications

Absolute Maximum Ratings

Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	-40	125	°C	
Storage temperature	T_{STG}	-65	150	°C	-
Voltage on V_{DDP} pins with respect to ground (V_{SSP})	V_{DDP}	-0.3	4.6	V	-
Voltage on any pin except int/ analog and XTAL with respect to ground (V_{SSP})	V_{IN0}	-0.5	4.6	V	-
Voltage on any int/analog pin with respect to ground (V_{SSP})	V_{IN1}	-0.5	4.6	V	-
Voltage on XTAL pins with respect to ground (V_{SSC})	V_{IN2}	-0.5	4.6	V	-
Input current on any pin during overload condition	I_{OV}	-10	10	mA	-[1)]
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	-	43	mA	-
Power dissipation	P_{DISS}	-	tbd	W	-

1) Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL2 etc.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DDP}$ or $V_{IN}<V_{SSP}$, $V_{IN2}>V_{DDC}$ or $V_{IN2}<V_{SSC}$) the voltage on V_{DDP} pin with respect to ground (V_{SSP}) must not exceed the values defined by the absolute maximum ratings.

Clock calculation table for ADC

TVC[1]	32								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	322	386	450	514	578	642	706	770	t_{SYS}
t_S	64	128	192	256	320	384	448	512	t_{SYS}

TVC[1]	28								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	282	338	394	450	506	562	618	674	t_{SYS}
t_S	56	112	168	224	280	336	392	448	t_{SYS}

TVC[1]	24								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	242	290	338	386	434	482	530	578	t_{SYS}
t_S	48	96	144	192	240	288	336	384	t_{SYS}

TVC[1]	20								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	202	242	282	322	362	402	442	482	t_{SYS}
t_S	40	80	120	160	200	240	280	320	t_{SYS}

TVC[1]	16								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	162	194	226	258	290	322	354	386	t_{SYS}
t_S	32	64	96	128	160	192	224	256	t_{SYS}

TVC[1]	12								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	122	146	170	194	218	242	266	290	t_{SYS}
t_S	24	48	72	96	120	144	168	192	t_{SYS}

TVC[1)]	8								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	82	98	114	130	146	162	178	194	t_{SYS}
t_S	16	32	48	64	80	96	112	128	t_{SYS}

TVC[1)]	4								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	42	50	58	66	74	82	90	98	t_{SYS}
t_S	8	16	24	32	40	48	56	64	t_{SYS}

1) TVC is the clock divider specified by bit fields ADCTC.

2) STC is the sample time control specified by bit fields ADSTC.

3) t_{ADC} is t_{SYS}*TVC