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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	138
Number of Logic Elements/Cells	1100
Total RAM Bits	65536
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCFBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp1k-cm36itr50

General Description

iCE40 Ultra family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 Ultra family includes integrated SPI and I²C blocks to interface with virtually all mobile sensors and application processors. The iCE40 Ultra family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 Ultra family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile sensors. The embedded RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 Ultra provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 500 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the modulation logic that meets his needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. This high current IR driver can also be used as Barcode Emulation, sending barcode information to external Barcode Reader.

The iCE40 Ultra family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 Ultra family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I²C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

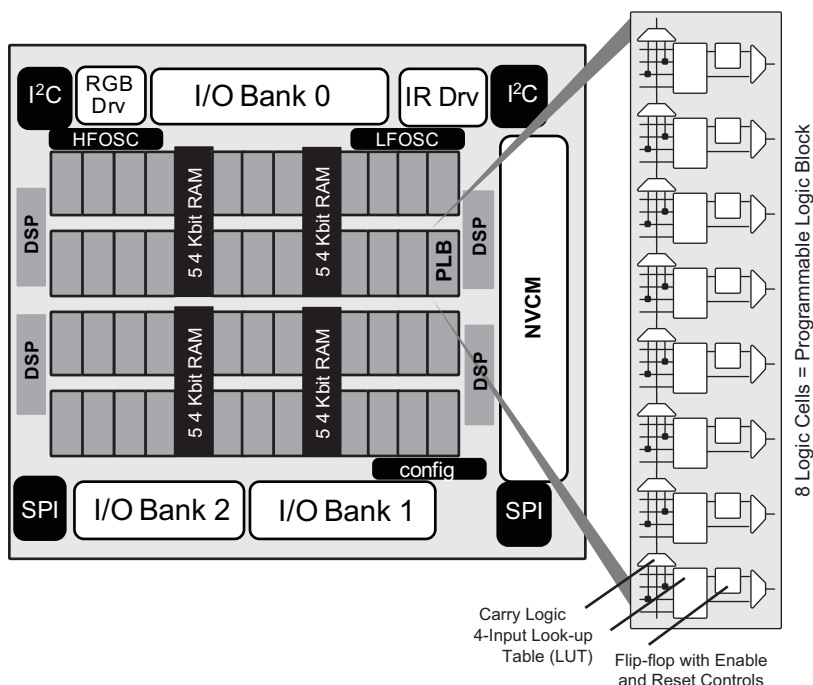
Features

- **Flexible Logic Architecture**
 - Three devices with 1100 to 3520 LUTs
 - Offered in WLCS, ucfBGA and QFN packages
- **Ultra-low Power Devices**
 - Advanced 40 nm ultra-low power process
 - As low as 71 μ A standby current typical
- **Embedded Memory**
 - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I²C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Oscillators**
 - Low Frequency Oscillator – 10 kHz
 - High Frequency Oscillator – 48 MHz
- **24 mA Current Drive RGB LED Outputs**
 - Three drive outputs in each device
 - User selectable sink current up to 24 mA
- **500 mA Current Drive IR LED Output**
 - One IR drive output in each device
 - User selectable sink current up to 500 mA
- **On-chip DSP**
 - Signed and unsigned 8-bit or 16-bit functions
 - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- **Flexible On-Chip Clocking**
 - Eight low skew global signal resource, six can be directly driven from external pins
 - One PLL with dynamic interface per device
- **Flexible Device Configuration**
 - SRAM is configured through:
 - Standard SPI Interface
 - Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
 - As small as 2.078 mm x 2.078 mm
- **Applications**
 - Smartphones
 - Tablets and Consumer Handheld Devices
 - Handheld Commercial and Industrial Devices
 - Multi Sensor Management Applications
 - Sensor Pre-processing and Sensor Fusion
 - Always-On Sensor Applications
 - USB 3.1 Type C Cable Detect / Power Delivery Applications

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks.

Table 2-4. sysMEM Block Configurations¹

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock, falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

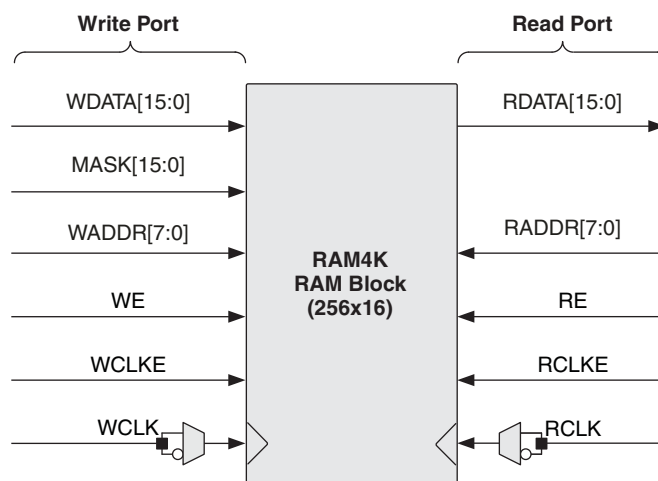


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).

Signal	Primitive Port Name	Width	Input / Output	Function	Default
OHLDA	OLOADTOP	1	Input	High-order (upper half) Accumulator Register Accumulate/Load control. 0 = Accumulate, register is loaded with Adder/Subtractor results 1 = Load, register is loaded with Input C or C Register	0: Accumulate
OHADS	ADDSUBTOP	1	Input	High-order (upper half) Accumulator Add or Subtract select. 0 = Add 1 = Subtract	0: Add
OLHLD	OHOLDBOT	1	Input	Low-order (lower half) Accumulator Register Hold. 0 = Update 1 = Hold	0: Update
OLRST	ORSTBOT	1	Input	Reset input to Low-order (lower half) bits of the Accumulator Register. 0 = No Reset 1 = Reset	0: No Reset
OLLDA	OLOADBOT	1	Input	Low-order (lower half) Accumulator Register Accumulate/Load control. 0 = Accumulate, register is loaded with Adder/Subtractor results 1 = Load, register is loaded with Input C or C Register	0: Accumulate
OLADS	ADDSUBBOT	1	Input	Low-order (lower half) Accumulator Add or Subtract select. 0 = Add 1 = Subtract	0: Add
CICAS	ACCUMCI	1	Input	Cascade Carry/Borrow input from previous sysDSP block	
CI	CI	1	Input	Carry/Borrow input from lower logic tile	
COCAS	ACCUMCO	1	Output	Cascade Carry/Borrow output to next sysDSP block	
CO	CO	1	Output	Carry/Borrow output to higher logic tile	
SIGNEXTIN	SIGNEXTIN	1	Input	Sign extension input from previous sysDSP block	
SIGNEXTOUT	SIGNEXTOUT	1	Output	Sign extension output to next sysDSP block	

The iCE40 Ultra sysDSP can support the following functions:

- 8-bit x 8-bit Multiplier
- 16-bit x 16-bit Multiplier
- 16-bit Adder/Subtractor
- 32-bit Adder/Subtractor
- 16-bit Accumulator
- 32-bit Accumulator
- 8-bit x 8-bit Multiply-Accumulate
- 16-bit x 16-bit Multiply-Accumulate

Figure 2-6 shows the path for an 8-bit x 8-bit Multiplier using the upper half of sysDSP block.

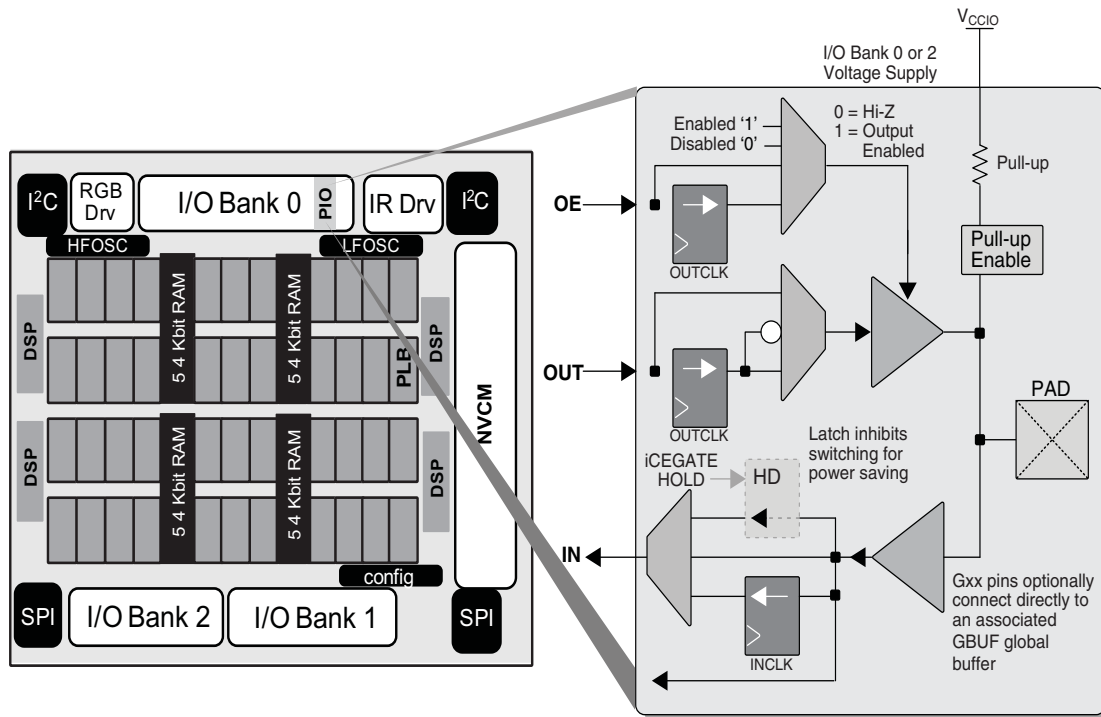
sysIO Buffer Banks

iCE40 Ultra devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_ V_{CCIO1} . Please refer to the [Pin Information Summary](#) table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-8. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-9 shows the input/output register block for the PIOs.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , SPI_V_{CCIO1} , and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the [DC and Switching Characteristics](#) section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO} . The I/O pins maintain the pre-configuration state until V_{CC} , SPI_V_{CCIO1} , and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-8 and Table 2-9 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 Ultra devices.

Differential Comparators

The iCE40 Ultra devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the [Pin Information Summary](#) section to locate the corresponding paired I/Os with differential comparators.

Table 2-8. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-9. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

On-Chip Oscillator

The iCE40 Ultra devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, [iCE40 LED Driver Usage Guide](#).

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration](#).

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_VCCIO1 power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, [iCE40 Programming and Configuration](#).

Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.42 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions¹

Symbol	Parameter		Min.	Max.	Units
V _{CC} ¹	Core Supply Voltage		1.14	1.26	V
V _{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71 ⁴	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V _{CCIO} ^{1, 2, 3}	I/O Driver Supply Voltage	V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}	1.71	3.46	V
V _{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t _{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t _{JIND}	Junction Temperature Industrial Operation		−40	100	°C
t _{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

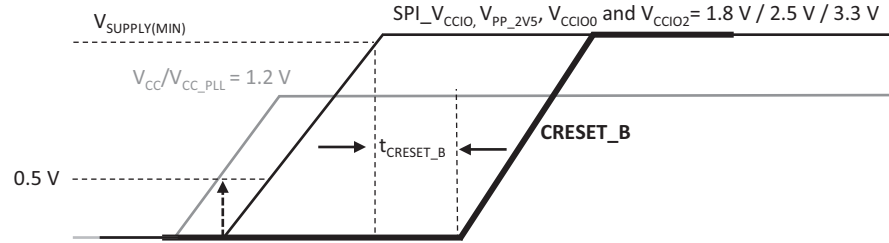
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to [Power-Up Supply Sequencing](#) section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates^{1, 2}

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to [Power-Up Supply Sequencing](#) section.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels¹

Symbol	Parameter		Min.	Max.	Units
V _{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V _{CC} , SPI_V _{CCIO1} , V _{PP_2V5})	V _{CC}	0.62	0.92	V
		SPI_V _{CCIO1}	0.87	1.50	V
		V _{PP_2V5}	0.90	1.53	V
V _{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V _{CC} , SPI_V _{CCIO1} , V _{PP_2V5})	V _{CC}	—	0.79	V
		SPI_V _{CCIO1}	—	1.50	V
		V _{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH} ^{1, 3, 4}	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2 V$	—	—	+/-10	μA
C_1	I/O Capacitance, excluding LED Drivers ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pF
C_2	Global Input Buffer Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pF
C_3	RGB Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	15	—	pF
C_4	IRLED Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	53	—	pF
V_{HYST}	Input Hysteresis	$V_{CCIO} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	$V_{CCIO} = 1.8 V, 0 < V_{IN} < 0.65 V_{CCIO}$	-3	—	-31	μA
		$V_{CCIO} = 2.5 V, 0 < V_{IN} < 0.65 V_{CCIO}$	-8	—	-72	μA
		$V_{CCIO} = 3.3 V, 0 < V_{IN} < 0.65 V_{CCIO}$	-11	—	-128	μA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.

2. T_J 25 °C, $f = 1.0 \text{ MHz}$.

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH} .

Supply Current ^{1, 2, 3, 4, 5}

Symbol	Parameter	Typ. $V_{CC} = 1.2 V^4$	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	71	μA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	0.55	μA
$I_{SPI_VCCIO1STDBY}$	SPI_V_{CCIO1} Power Supply Static Current	0.5	μA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	0.5	μA
I_{CCPEAK}	Core Power Supply Startup Peak Current	8.0	mA
$I_{PP_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	7.0	mA
$I_{SPI_VCCIO1PEAK}$	SPI_V_{CCIO1} Power Supply Startup Peak Current	9.0	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	7.5	mA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J = 25^\circ C$, power supplies at nominal voltage, on devices processed in nominal process conditions.
4. Does not include pull-up.
5. Startup Peak Currents are measured with decoupling capacitance of 0.1 μF , 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.

User I²C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	μs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	μs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	μs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	μs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	μs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	μs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	μs

User SPI Specifications ^{1, 2}

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software tools. These parameters include the following:
 - $t_{SUmater}$ master Setup time (master mode)
 - $t_{HOLDmaster}$ master Hold time (master mode)
 - $t_{SUslave}$ slave Setup time (slave mode)
 - $t_{HOLDslave}$ slave Hold time (slave mode)
 - $t_{SCK2OUT}$ SCK to out (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI} , t_{LO}) time.

Internal Oscillators (HFOSC, LFOSC)¹

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency ($t_J = 0\text{ }^{\circ}\text{C} - 85\text{ }^{\circ}\text{C}$)	-10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency ($t_J = -40\text{ }^{\circ}\text{C} - 100\text{ }^{\circ}\text{C}$)	-20%	48	20%	MHz
f_{CLKLF}		LFOSC CLKK clock frequency	-10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC clock frequency ($t_J = 0\text{ }^{\circ}\text{C} - 85\text{ }^{\circ}\text{C}$)	45	50	55	%
	Industrial Temp	HFOSC clock frequency ($t_J = -45\text{ }^{\circ}\text{C} - 100\text{ }^{\circ}\text{C}$)	40	50	60	%
DCH_{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
T_{sync_on}		Oscillator output synchronizer delay	—	—	5	Cycles
T_{sync_off}		Oscillator output disable delay	—	—	5	Cycles

1. Glitchless enabling and disabling OSC clock outputs.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	$V_{CCIO} + 0.2V$	0.4	$V_{CCIO} - 0.4$	8	-8
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 2.5	-0.3	0.7	1.7	$V_{CCIO} + 0.2V$	0.4	$V_{CCIO} - 0.4$	6	-6
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	$V_{CCIO} + 0.2V$	0.4	$V_{CCIO} - 0.4$	4	-4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{REF}	Reference Voltage to compare, on V_{INM}	$V_{CCIO} = 2.5\text{ V}$	0.25	$V_{CCIO} - 0.25\text{ V}$	V
V_{DIFFIN_H}	Differential input HIGH ($V_{INP} - V_{INM}$)	$V_{CCIO} = 2.5\text{ V}$	250	—	mV
V_{DIFFIN_L}	Differential input LOW ($V_{INP} - V_{INM}$)	$V_{CCIO} = 2.5\text{ V}$	—	-250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	$V_{CCIO} = 2.5\text{ V}$	-10	10	μA

Typical Building Block Function Performance^{1, 2}

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the Lattice Design Software tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Under worst case operating conditions.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance¹

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Measured with a toggling pattern

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1, 5, 6}$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	450	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \geq 100$ MHz	—	750	ps p-p
		$f_{OUT} < 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 25$ MHz	—	275	ps p-p
		$f_{PFD} < 25$ MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	μs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}^4	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{STABLE}^3	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE_PW}^3$	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	μs
$t_{DYNAMIC_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD} . As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

sysDSP Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

SPI Master or NVCM Configuration Time^{1, 2}

Symbol	Parameter	Conditions	Max.	Units
t _{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t _{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t _{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t _{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	μs
f _{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read ¹	—	15	—	MHz
t _{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t _{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t _{STSU}	CCLK setup time		12	—	—	ns
t _{STH}	CCLK hold time		12	—	—	ns
t _{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI³						
f _{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency ²	21.0	33.0	45.0	MHz
		High Frequency ²	33.0	53.0	71.0	MHz
t _{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	μs
t _{SU}	CCLK setup time ⁴		9.9	—	—	ns
t _{HD}	CCLK hold time		1	—	—	ns

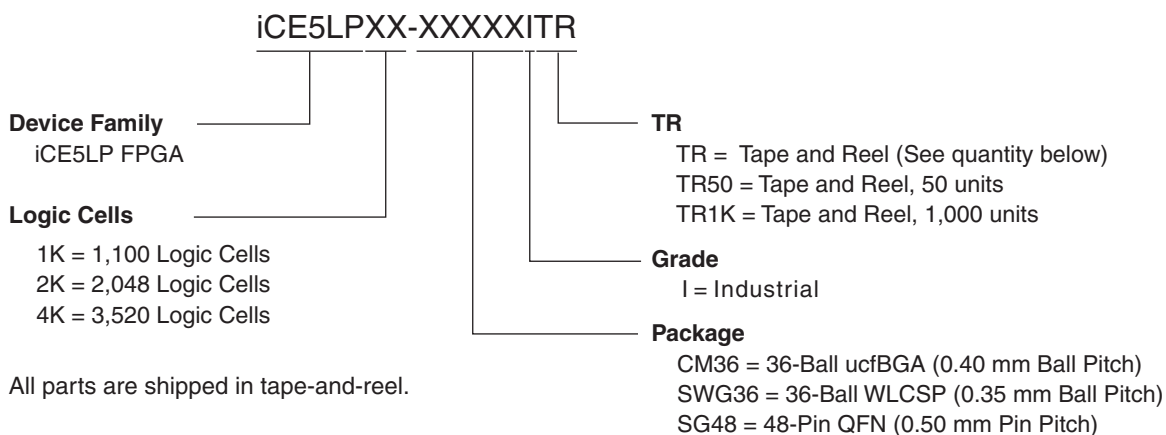
1. Supported with 1.2 V Vcc and at 25 °C.

2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.

3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

4. For considerations of SPI Master Configuration Mode, please refer to TN1248, [iCE40 Programming and Configuration](#).

iCE5LP Part Number Description



Tape and Reel Quantity

Package	TR Quantity
CM36	4,000
SWG36	5,000
SG48	2,000

Date	Version	Section	Change Summary
June 2016	2.0	Introduction	Updated General Description section. Changed “high current driver” to “high current IR driver”.
			Updated Features section. In Table 1-1, iCE40 Ultra Family Selection Guide, corrected HF Oscillator (48 kHz) to (48 MHz).
		Architecture	Updated Architecture Overview section.
			— Changed content to “The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks.”
			— Changed “high current LED sink” to “high current RGB and IR LED sinks”.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. Corrected V_{CCPLL} character format in Figure 2-3, PLL Diagram.
			Updated sysMEM Embedded Block RAM Memory section. Updated footnote in Table 2-4, sysMEM Block Configurations.
			Updated sysIO Buffer Banks section.
			— Changed statement to “The configuration SPI interface signals are powered by SPI_V_{CCIO1} .”
			— Corrected V_{CCIO} character format in Figure 2-8, I/O Bank and Programmable I/O Cell.
			Updated Typical I/O Behavior During Power-up section. Modified text content.
			Updated Supported Standards section. Changed statement to “The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators.”
			Updated On-Chip Oscillator section. Changed statement to “The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option.”
			Updated section heading to High Current LED Drive I/O Pins . Changed “high current drive” to “high current LED drive”.
			Removed Power On Reset section.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section.
			— Corrected symbol character format.
			Updated Recommended Operating Conditions section.
			— Corrected symbol character format.
			— Revised footnote 1.
			— Added footnote 4.
			Updated Power Supply Ramp Rates section. Changed t_{RAMP} Max. value.
			Added Power-On Reset section.
			Updated section heading to Power-Up Supply Sequencing . Revised text content.
			Added External Reset section.
			Updated DC Electrical Characteristics section. Revised footnote 4.

Date	Version	Section	Change Summary
April 2015	1.7	Architecture	Updated sysDSP section. Revised the following figures: — Figure 2-5, sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate) — Figure 2-6, sysDSP 8-bit x 8-bit Multiplier — Figure 2-7, DSP 16-bit x 16-bit Multiplier
		Ordering Information	Updated iCE5LP Part Number Description section. Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
March 2015	1.6	Introduction	Updated Features section. — Added BGA and QFN packages in Flexible Logic Architecture. — Added USB 3.1 Type C Cable Detect / Power Delivery Applications in Applications. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added 36-ball ucFBGA and 48-ball QFN packages. Changed subheading to Total User I/O Count. Changed RBW IP to PWM IP. Deleted footnotes.
		DC and Switching Characteristics	Updated Power-up Sequence section. Indicated all devices in second paragraph.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2.5 V _{OH} Min. (V) from 0.5 to 0.4.
			Replaced the Differential Comparator Electrical Characteristics table.
		Pinout Information	Updated Pin Information Summary section. — Added CM36 and SG48 values. — Changed CRESET_B to Dedicated Config Pins.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added CM36 and SG48 package. — Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
October 2014	1.5	Introduction	Updated Features section. — Removed 26 I/O pins for 36-pin WLCSP under Flexible Logic Architecture. — Changed form factor to 2.078 mm x 2.078 mm. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 20-Ball WLCSP.
			Updated Introduction section. Changed form factor to 2.078 mm x 2.078 mm.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) section. Removed note in heading regarding sysCLOCK PLL support.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Removed footnote on sysCLOCK PLL support.
			Updated Power-up Sequence section. Removed information on 20-pin WLCSP.
		Pinout Information	Updated Signal Descriptions section. Removed references 20-pin WLCSP.
			Updated Pin Information Summary section. Removed references to UWG20 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 20-ball WLCSP.
			Updated Ordering Part Numbers section. Removed UWG20 part numbers.
		Further Information	Added technical note references.

Date	Version	Section	Change Summary
August 2014	1.4	All	Removed Preliminary document status.
		Introduction	Updated General Description section. Added information on high current driver.
			Updated Features section. — Changed standby current typical to as low as 71 μ A. — Changed feature to Embedded Memory. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added NVCM and Embedded PWM IP rows. Added (MULT16 with 32-bit Accumulator) to DSP Block. Added Total I/O (Dedicated I/O) Count data.
			General update to Introduction section.
		Architecture	Updated Architecture Overview section. — Revised and added information on sysIO banks. — Updated reference for embedded PWM IP. Updated iCE40 Ultra Programming and Configuration section. — Changed SPI1 to SPI. — Changed VCCIO_1 to SPI_VCCIO1.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Changed PLL Supply Voltage VCCPLL value.
			Updated Recommended Operating Conditions section. Added footnote to VCCPLL.
			Updated Power-up Sequence section. General update.
			Updated Power-On-Reset Voltage Levels section. Changed the V _{PORUP} V _{CC} Max. value.
			Updated DC Electrical Characteristics section. Added C ₃ and C ₄ information.
			Updated Supply Current section. — Completed Typ. VCC = 1.2 V4 data. — Changed symbols to I _{SPI_VCCIO1STDBY} and I _{SPI_VCCIO1PEAK} . — Added information to footnote 3.
			Updated Internal Oscillators (HFOSC, LFOSC) section. General update.
			Updated iCE40 Ultra External Switching Characteristics section. Added Max. value for t _{COPLL} . Added Min. values for t _{SUPLL} and t _{HPLL} .
			Updated sysCLOCK PLL Timing section. Added Max. value for t _{OPJIT} .
			Updated sysCONFIG Port Timing Specifications section. — Added T _{SU} and T _{HD} information. — Added footnote 3 to Master SPI.
			Updated High Current LED and IR LED Drive section. Updated Min. value.
July 2014	1.3	All	Changed document status from Advance to Preliminary.
		Introduction	Updated Features section. Adjusted Ultra-low Power Devices standby current.
		DC and Switching Characteristics	Updated AC/DC specifications numbers.

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
			Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
			Replaced RGB PWM Block section with Embedded PWM IP section.
		DC and Switching Characteristics	Removed RGB PWM Block Timing section.
April 2014	01.0	All	Initial release.