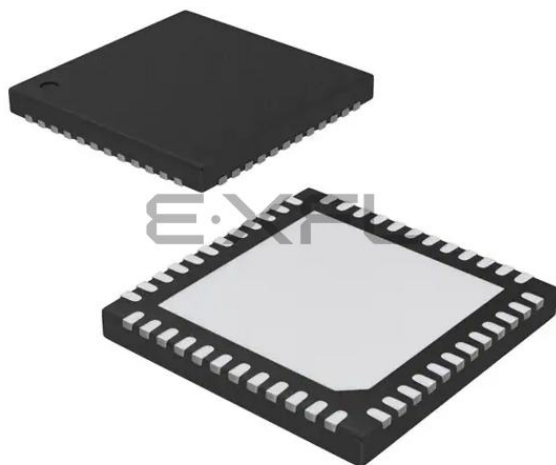




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	138
Number of Logic Elements/Cells	1100
Total RAM Bits	65536
Number of I/O	39
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp1k-sg48itr50

General Description

iCE40 Ultra family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 Ultra family includes integrated SPI and I²C blocks to interface with virtually all mobile sensors and application processors. The iCE40 Ultra family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 Ultra family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile sensors. The embedded RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 Ultra provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 500 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the modulation logic that meets his needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. This high current IR driver can also be used as Barcode Emulation, sending barcode information to external Barcode Reader.

The iCE40 Ultra family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 Ultra family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I²C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
 - Three devices with 1100 to 3520 LUTs
 - Offered in WLCS, ucfBGA and QFN packages
- **Ultra-low Power Devices**
 - Advanced 40 nm ultra-low power process
 - As low as 71 μ A standby current typical
- **Embedded Memory**
 - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I²C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Oscillators**
 - Low Frequency Oscillator – 10 kHz
 - High Frequency Oscillator – 48 MHz
- **24 mA Current Drive RGB LED Outputs**
 - Three drive outputs in each device
 - User selectable sink current up to 24 mA
- **500 mA Current Drive IR LED Output**
 - One IR drive output in each device
 - User selectable sink current up to 500 mA
- **On-chip DSP**
 - Signed and unsigned 8-bit or 16-bit functions
 - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- **Flexible On-Chip Clocking**
 - Eight low skew global signal resource, six can be directly driven from external pins
 - One PLL with dynamic interface per device
- **Flexible Device Configuration**
 - SRAM is configured through:
 - Standard SPI Interface
 - Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
 - As small as 2.078 mm x 2.078 mm
- **Applications**
 - Smartphones
 - Tablets and Consumer Handheld Devices
 - Handheld Commercial and Industrial Devices
 - Multi Sensor Management Applications
 - Sensor Pre-processing and Sensor Fusion
 - Always-On Sensor Applications
 - USB 3.1 Type C Cable Detect / Power Delivery Applications

Table 1-1. iCE40 Ultra Family Selection Guide

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
Logic Cells (LUT + Flip-Flop)	1100	2048	3520
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
Packages, ball pitch, dimension	Total User I/O Count		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39

Introduction

The iCE40 Ultra family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), on-chip Oscillators (LFOSC, HFOSC), two hardened I²C Controllers, two hardened SPI Controllers, three 24 mA RGB LED open-drain drivers, a 500 mA IR LED open-drain drivers, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 Ultra FPGAs are available in very small form factor packages, as small as 2.078 mm x 2.078 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 Ultra devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 Ultra devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 Ultra family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 Ultra. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 Ultra device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

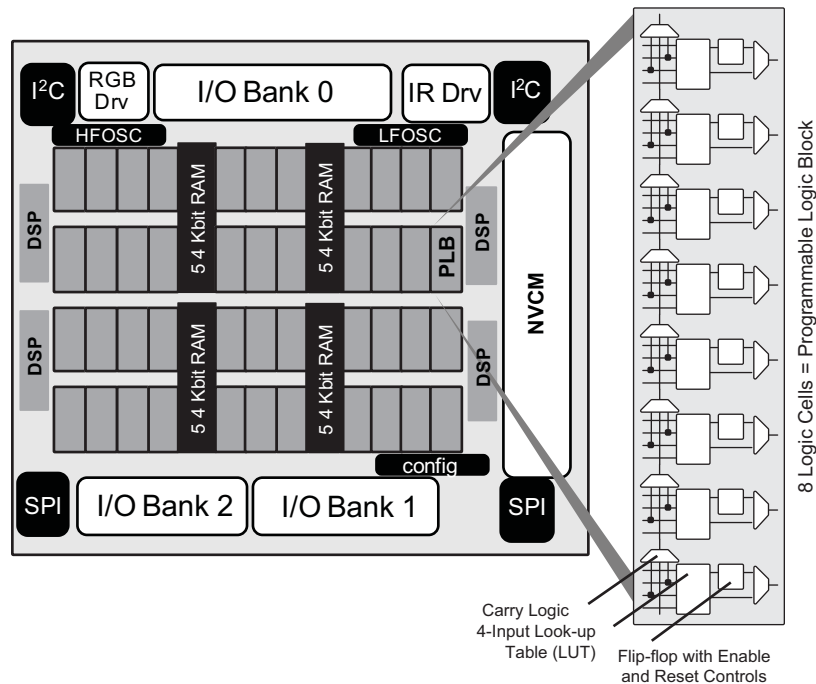
Lattice provides in the iCE40 Ultra 1K and 2K device the embedded RGB PWM IP at no extra cost of LUT available to the user, to perform controlling the RGB LED function. This embedded IP allow users to control color, LED ON/OFF time, and breathe rate of the LED. For more information, please refer to Usage Guide in Lattice Design Software.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 Ultra FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, please contact your local Lattice representative.

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks.

Routing

There are many resources provided in the iCE40 Ultra devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 Ultra device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40 Ultra External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 Ultra device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 Ultra device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

Table 2-4. sysMEM Block Configurations¹

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock, falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

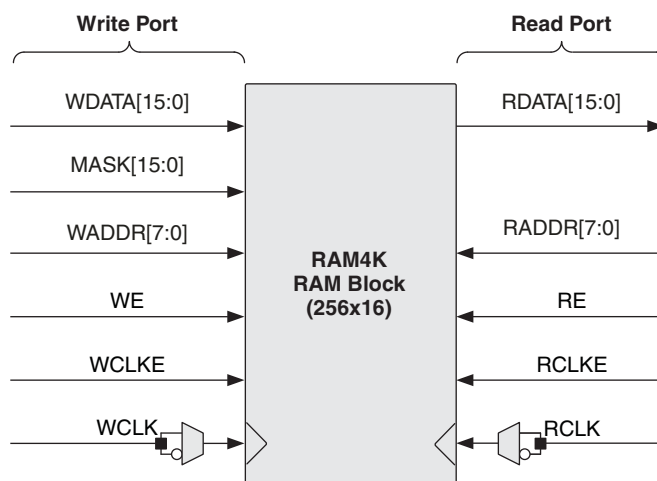


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtractor functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

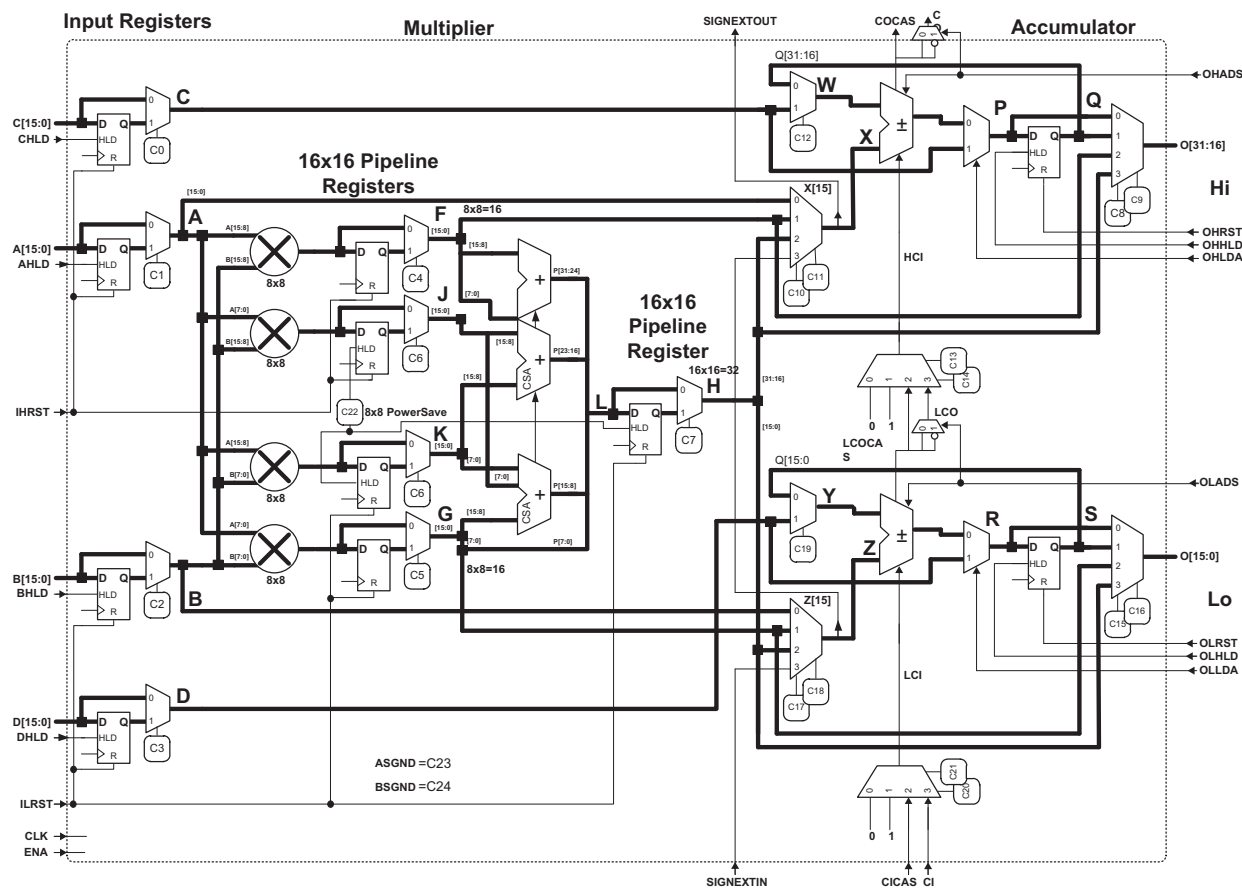


Figure 2-6. sysDSP 8-bit x 8-bit Multiplier

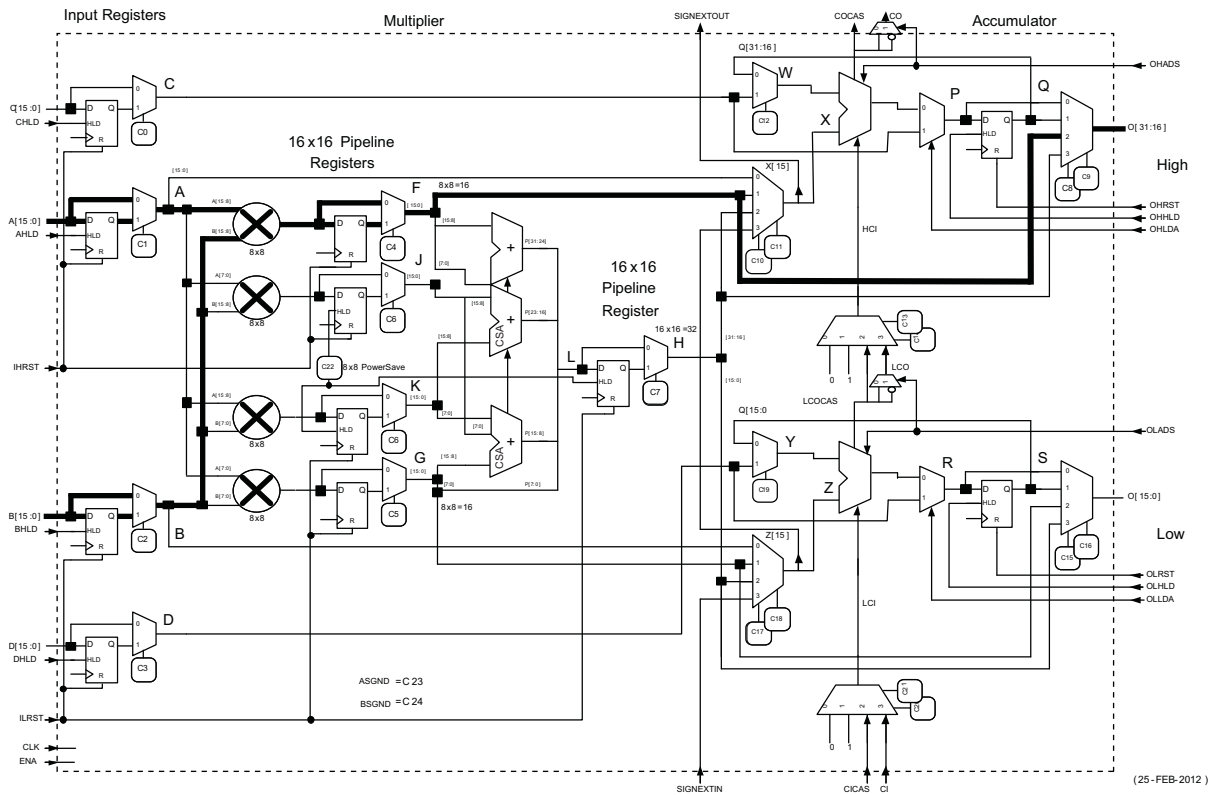


Figure 2-7 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

[illegible]

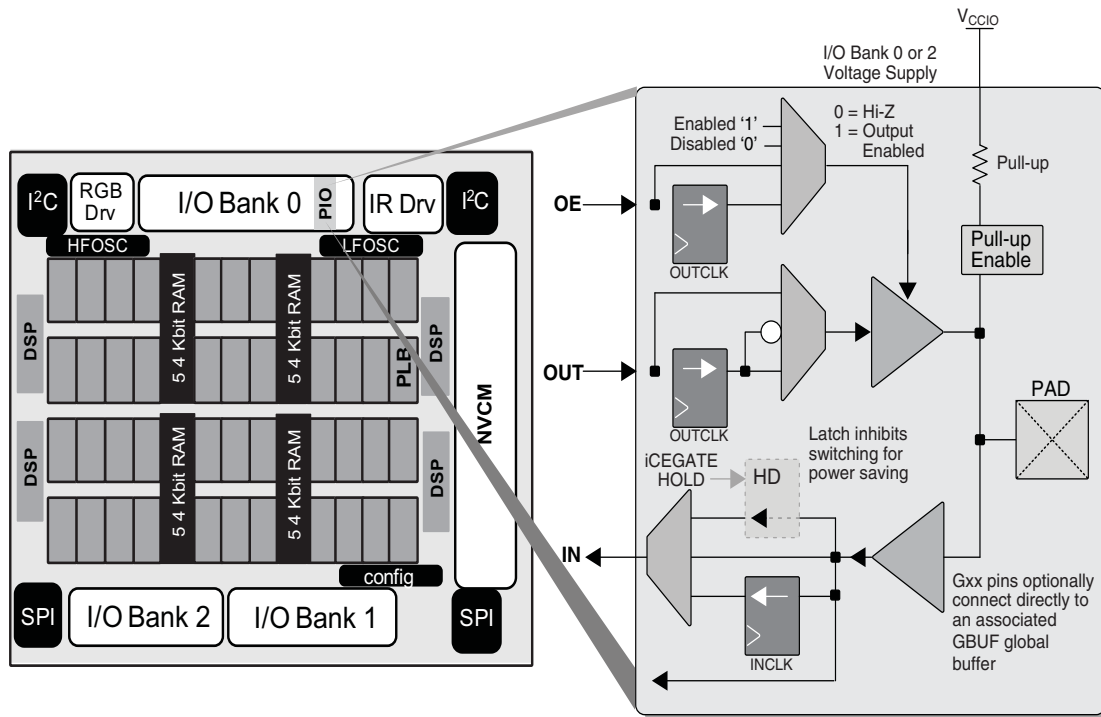
sysIO Buffer Banks

iCE40 Ultra devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1} . Please refer to the [Pin Information Summary](#) table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-8. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-9 shows the input/output register block for the PIOs.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, [iCE40 LED Driver Usage Guide](#).

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration](#).

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, [iCE40 Programming and Configuration](#).

Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.42 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions¹

Symbol	Parameter		Min.	Max.	Units
V _{CC} ¹	Core Supply Voltage		1.14	1.26	V
V _{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71 ⁴	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V _{CCIO} ^{1, 2, 3}	I/O Driver Supply Voltage	V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}	1.71	3.46	V
V _{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t _{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t _{JIND}	Junction Temperature Industrial Operation		−40	100	°C
t _{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

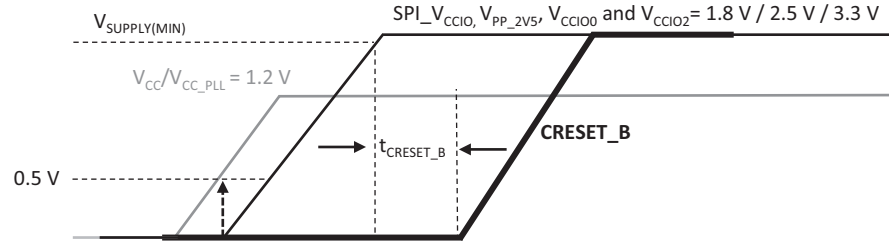
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to [Power-Up Supply Sequencing](#) section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates^{1, 2}

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to [Power-Up Supply Sequencing](#) section.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels¹

Symbol	Parameter		Min.	Max.	Units
V _{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V _{CC} , SPI_V _{CCIO1} , V _{PP_2V5})	V _{CC}	0.62	0.92	V
		SPI_V _{CCIO1}	0.87	1.50	V
		V _{PP_2V5}	0.90	1.53	V
V _{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V _{CC} , SPI_V _{CCIO1} , V _{PP_2V5})	V _{CC}	—	0.79	V
		SPI_V _{CCIO1}	—	1.50	V
		V _{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{IL} , I _{IH} ^{1,3,4}	Input or I/O Leakage	0V < V _{IN} < V _{CCIO} + 0.2 V	—	—	+/-10	μA
C ₁	I/O Capacitance, excluding LED Drivers ²	V _{CCIO} = 3.3 V, 2.5 V, 1.8 V V _{CC} = Typ., V _{IO} = 0 to V _{CCIO} + 0.2 V	—	6	—	pF
C ₂	Global Input Buffer Capacitance ²	V _{CCIO} = 3.3 V, 2.5 V, 1.8 V V _{CC} = Typ., V _{IO} = 0 to V _{CCIO} + 0.2 V	—	6	—	pF
C ₃	RGB Pin Capacitance ²	V _{CC} = Typ., V _{IO} = 0 to 3.5 V	—	15	—	pF
C ₄	IRLED Pin Capacitance ²	V _{CC} = Typ., V _{IO} = 0 to 3.5 V	—	53	—	pF
V _{HYST}	Input Hysteresis	V _{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I _{PU}	Internal PIO Pull-up Current	V _{CCIO} = 1.8 V, 0 ≤ V _{IN} ≤ 0.65 V _{CCIO}	-3	—	-31	μA
		V _{CCIO} = 2.5 V, 0 ≤ V _{IN} ≤ 0.65 V _{CCIO}	-8	—	-72	μA
		V _{CCIO} = 3.3 V, 0 ≤ V _{IN} ≤ 0.65 V _{CCIO}	-11	—	-128	μA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.

2. T_J 25 °C, f = 1.0 MHz.

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

SPI Master or NVCM Configuration Time^{1, 2}

Symbol	Parameter	Conditions	Max.	Units
t _{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t _{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t _{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t _{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	μs
f _{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read ¹	—	15	—	MHz
t _{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t _{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t _{STSU}	CCLK setup time		12	—	—	ns
t _{STH}	CCLK hold time		12	—	—	ns
t _{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI³						
f _{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency ²	21.0	33.0	45.0	MHz
		High Frequency ²	33.0	53.0	71.0	MHz
t _{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	μs
t _{SU}	CCLK setup time ⁴		9.9	—	—	ns
t _{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.

2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.

3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

4. For considerations of SPI Master Configuration Mode, please refer to TN1248, [iCE40 Programming and Configuration](#).

Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V _{CC}		Power	—	Core Power Supply
V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1 and 2.
V _{PP_2V5}		Power	—	Power for NVCM programming and operations.
V _{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V _{CCIO_1} .
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V _{CCIO1} .
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V _{CCIO1} .
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V _{CCIO1} .
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM361TR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM361TR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM361TR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG361TR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG361TR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG361TR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG481TR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG481TR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM361TR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM361TR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM361TR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG361TR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG361TR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG361TR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG481TR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG481TR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM361TR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM361TR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM361TR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG361TR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG361TR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG361TR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG481TR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG481TR50	3520	1.2 V	Halogen-Free QFN	48	IND

For Further Information

A variety of technical notes for the iCE40 Ultra family are available on the Lattice web site.

- TN1248, [iCE40 Programming and Configuration](#)
- TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#)
- TN1276, [Advanced iCE40 SPI/I2C Hardened IP Usage Guide](#)
- TN1250, [Memory Usage Guide for iCE40 Devices](#)
- TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#)
- TN1252, [iCE40 Hardware Checklist](#)
- TN1288, [iCE40 LED Driver Usage Guide](#)
- TN1295, [DSP Function Usage Guide for iCE40 Devices](#)
- TN1296, [iCE40 Oscillator Usage Guide](#)
- [iCE40 Ultra Pinout Files](#)
- [iCE40 Ultra Pin Migration Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)
- [Schematic Symbols](#)

Date	Version	Section	Change Summary
			Updated Supply Current section. — Corrected $I_{PP2V5STDBY}$ parameter. — Added Typ. $V_{CC} = 1.2\text{ V}$ values for I_{CCPEAK}, $I_{PP_2V5PEAK}$, $I_{SPI_VCCIO1PEAK}$, and $I_{CCIOPEAK}$. — Added footnote 5. — Corrected S_{PI_VCCIO1} character format. Updated User SPI Specifications section. Removed parameters and added footnotes. Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for DCH_{CLKHF}. Updated sysIO Single-Ended DC Electrical Characteristics section. Removed footnote. Updated Register-to-Register Performance section. Modified footnotes. Updated iCE40 Ultra External Switching Characteristics section. Modified footnote. Updated sysCLOCK PLL Timing section. Reversed t_{OPJIT} conditions. Updated sysCONFIG Port Timing Specifications section. — Modified t_{CR_SCK} Min. value. — Added footnote 4 to t_{SU} parameter. — Modified t_{SU} Min. value. — Modified t_{HD} parameter. Updated section heading to RGB LED and IR LED Drive. Modified $I_{LED_ACCURACY}$ and $I_{IR_ACCURACY}$ parameters, Min. and Max. values.
		Pinout Information	Updated Signal Descriptions section. Changed V_{CCIO_1} to SPI_V_{CCIO1} in the CDONE, CRESETB and PIOB_xx descriptions. Updated Pin Information Summary section. — Corrected symbol character format. — Corrected V_{CPP_2V5} to V_{PP_2V5}.
	1.9	Introduction	Updated Features section. Updated BGA package to ucfBGA.
		DC and Switching Characteristics	Updated Differential Comparator Electrical Characteristics section. Corrected typo in V_{REF} Max. value.
		Pinout Information	Updated Signal Descriptions section. — Changed PIOB_12a to PIOB_xx — Changed SPI_CSN to SPI_SS_B and revised description when in Slave SPI mode. — Corrected minor typo errors. Updated Pin Information Summary section. Added footnote to SG48.
		Ordering Information	Updated iCE5LP Part Number Description section. Updated BGA package to ucfBGA. Updated Ordering Part Numbers section. Updated BGA package to ucfBGA.
June 2015	1.8	DC and Switching Characteristics	Updated Internal Oscillators (HFOSC, LFOSC) section. Removed decimals.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added TR items. — Corrected formatting errors. Updated Ordering Part Numbers section. Updated CM36 and SG48 packages.

Date	Version	Section	Change Summary
August 2014	1.4	All	Removed Preliminary document status.
		Introduction	Updated General Description section. Added information on high current driver.
			Updated Features section. — Changed standby current typical to as low as 71 μ A. — Changed feature to Embedded Memory. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added NVCM and Embedded PWM IP rows. Added (MULT16 with 32-bit Accumulator) to DSP Block. Added Total I/O (Dedicated I/O) Count data.
			General update to Introduction section.
		Architecture	Updated Architecture Overview section. — Revised and added information on sysIO banks. — Updated reference for embedded PWM IP. Updated iCE40 Ultra Programming and Configuration section. — Changed SPI1 to SPI. — Changed VCCIO_1 to SPI_VCCIO1.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Changed PLL Supply Voltage VCCPLL value.
			Updated Recommended Operating Conditions section. Added footnote to VCCPLL.
			Updated Power-up Sequence section. General update.
			Updated Power-On-Reset Voltage Levels section. Changed the V _{PORUP} V _{CC} Max. value.
			Updated DC Electrical Characteristics section. Added C ₃ and C ₄ information.
			Updated Supply Current section. — Completed Typ. VCC = 1.2 V4 data. — Changed symbols to I _{SPI_VCCIO1STDBY} and I _{SPI_VCCIO1PEAK} . — Added information to footnote 3.
			Updated Internal Oscillators (HFOSC, LFOSC) section. General update.
			Updated iCE40 Ultra External Switching Characteristics section. Added Max. value for t _{COPLL} . Added Min. values for t _{SUPLL} and t _{HPLL} .
			Updated sysCLOCK PLL Timing section. Added Max. value for t _{OPJIT} .
			Updated sysCONFIG Port Timing Specifications section. — Added T _{SU} and T _{HD} information. — Added footnote 3 to Master SPI.
			Updated High Current LED and IR LED Drive section. Updated Min. value.
July 2014	1.3	All	Changed document status from Advance to Preliminary.
		Introduction	Updated Features section. Adjusted Ultra-low Power Devices standby current.
		DC and Switching Characteristics	Updated AC/DC specifications numbers.

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
			Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
			Replaced RGB PWM Block section with Embedded PWM IP section.
		DC and Switching Characteristics	Removed RGB PWM Block Timing section.
April 2014	01.0	All	Initial release.