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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	138
Number of Logic Elements/Cells	1100
Total RAM Bits	65536
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-XFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.1x2.1)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp1k-swg36itr1k">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp1k-swg36itr1k</a>

## General Description

iCE40 Ultra family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 Ultra family includes integrated SPI and I<sup>2</sup>C blocks to interface with virtually all mobile sensors and application processors. The iCE40 Ultra family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 Ultra family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile sensors. The embedded RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 Ultra provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 500 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the modulation logic that meets his needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. This high current IR driver can also be used as Barcode Emulation, sending barcode information to external Barcode Reader.

The iCE40 Ultra family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 Ultra family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I<sup>2</sup>C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

## Features

- **Flexible Logic Architecture**
  - Three devices with 1100 to 3520 LUTs
  - Offered in WLCS, ucfBGA and QFN packages
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - As low as 71  $\mu$ A standby current typical
- **Embedded Memory**
  - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I<sup>2</sup>C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Oscillators**
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- **500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 500 mA
- **On-chip DSP**
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
  - As small as 2.078 mm x 2.078 mm
- **Applications**
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

**Table 1-1. iCE40 Ultra Family Selection Guide**

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
<b>Logic Cells (LUT + Flip-Flop)</b>	<b>1100</b>	<b>2048</b>	<b>3520</b>
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
<b>Packages, ball pitch, dimension</b>	<b>Total User I/O Count</b>		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39

## Introduction

The iCE40 Ultra family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), on-chip Oscillators (LFOSC, HFOSC), two hardened I<sup>2</sup>C Controllers, two hardened SPI Controllers, three 24 mA RGB LED open-drain drivers, a 500 mA IR LED open-drain drivers, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 Ultra FPGAs are available in very small form factor packages, as small as 2.078 mm x 2.078 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 Ultra devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 Ultra devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 Ultra family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 Ultra. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 Ultra device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides in the iCE40 Ultra 1K and 2K device the embedded RGB PWM IP at no extra cost of LUT available to the user, to perform controlling the RGB LED function. This embedded IP allow users to control color, LED ON/OFF time, and breathe rate of the LED. For more information, please refer to Usage Guide in Lattice Design Software.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 Ultra FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, please contact your local Lattice representative.

## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 Ultra devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 Ultra global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 Ultra PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

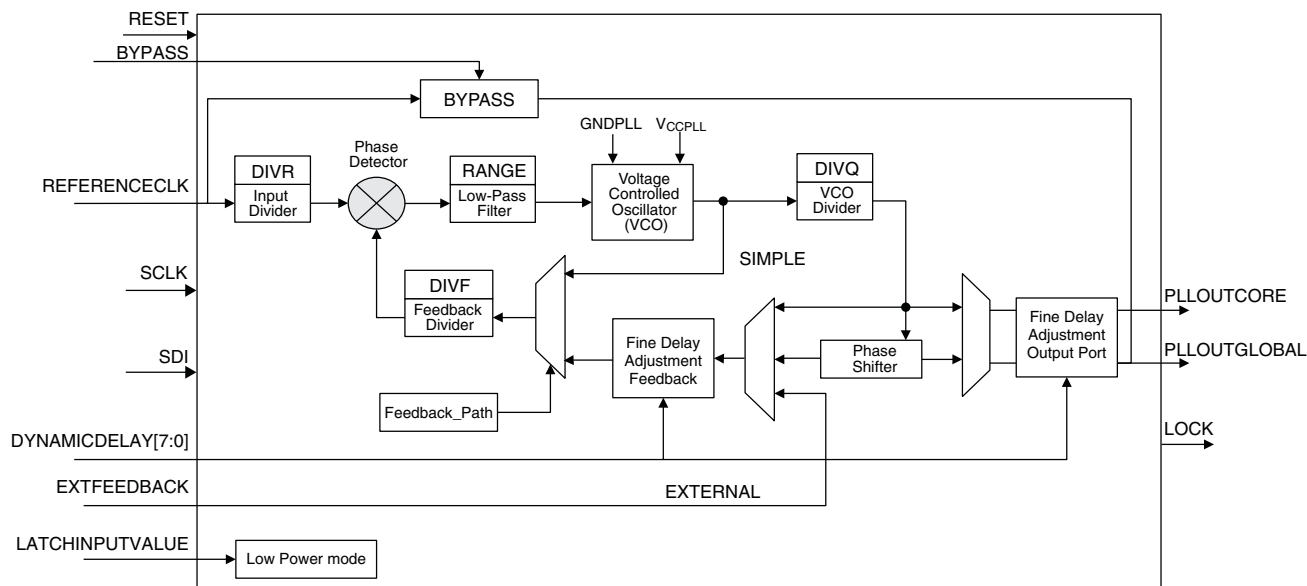


Table 2-3 provides signal descriptions of the PLL block.

## sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

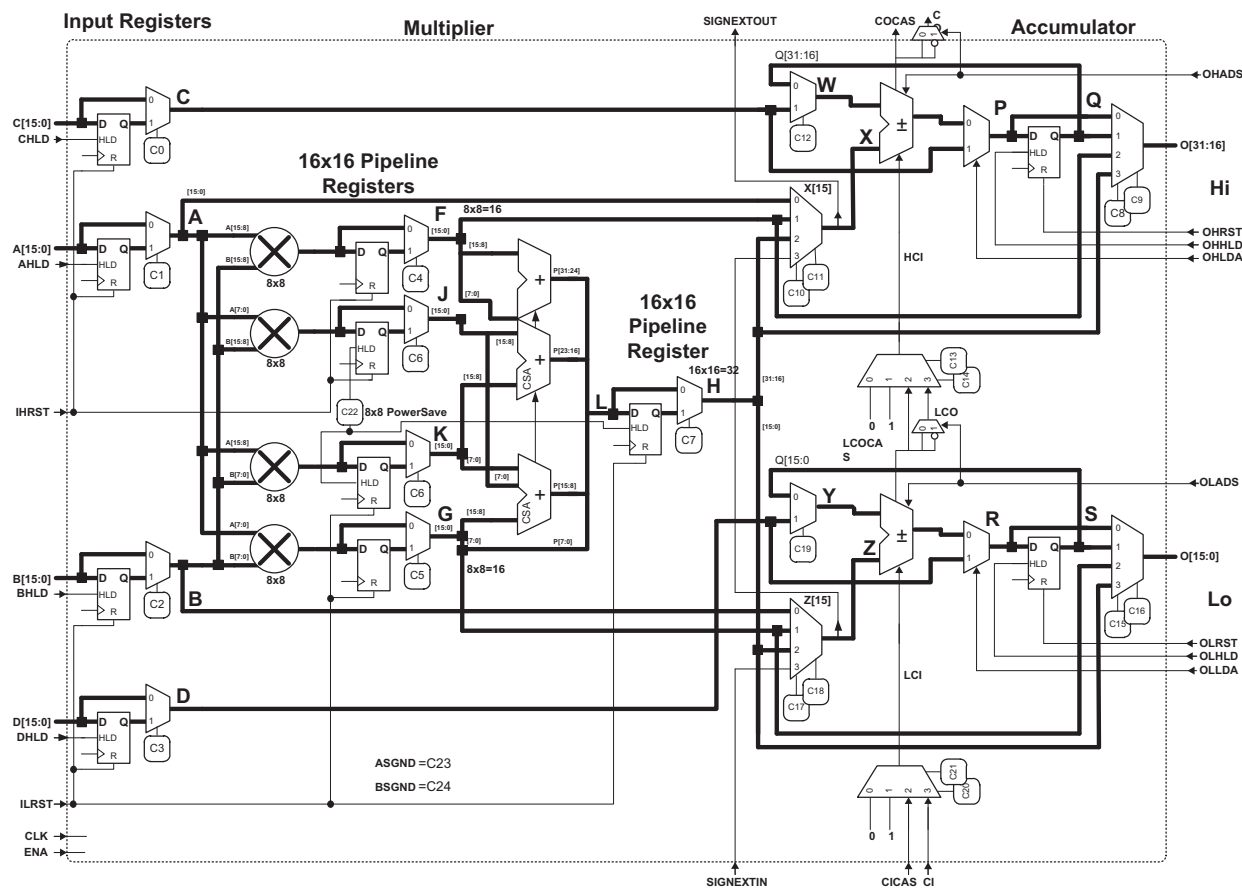
### iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtractor functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

**Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)**



**Figure 2-6. sysDSP 8-bit x 8-bit Multiplier**

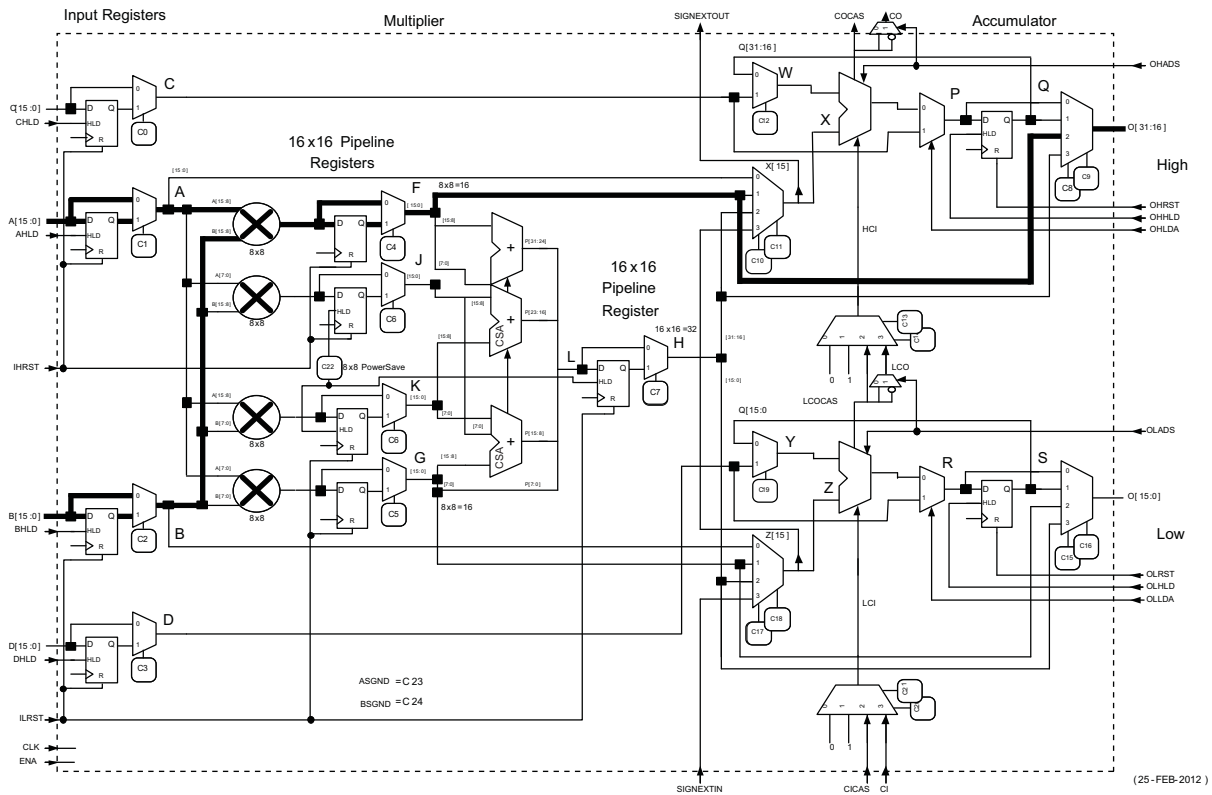
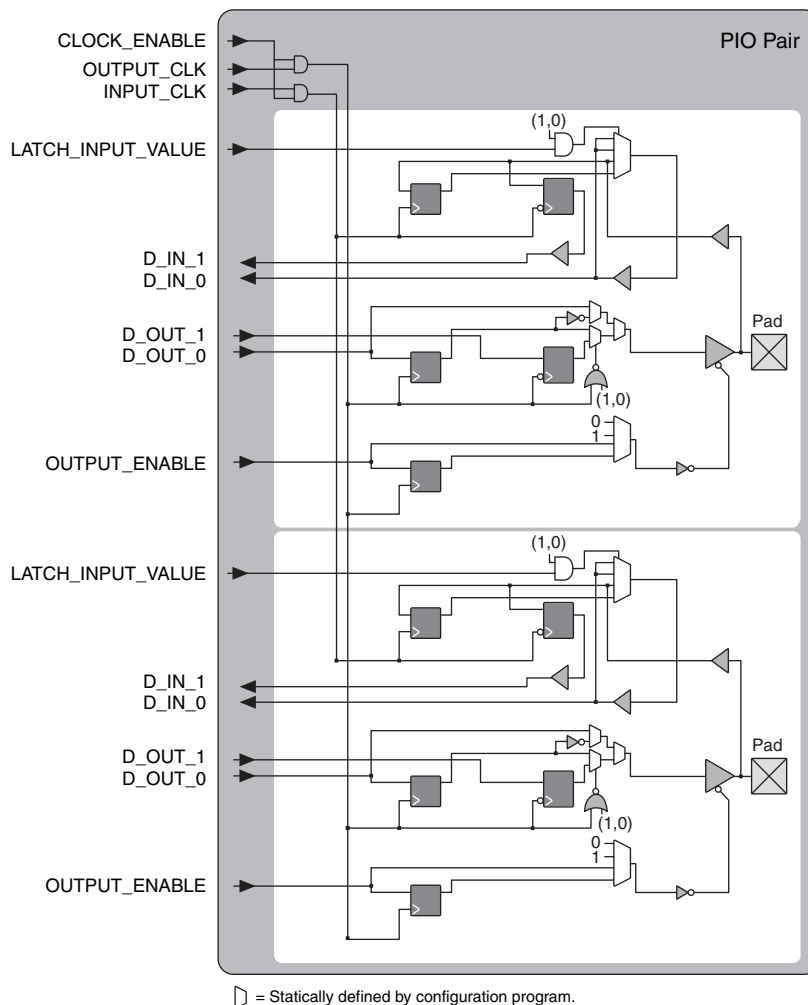


Figure 2-7 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.



**Figure 2-9. iCE I/O Register Block Diagram**



**Table 2-7. PIO Signal List**

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.



## User I<sup>2</sup>C IP

The iCE40 Ultra devices have two I<sup>2</sup>C IP cores. Either of the two cores can be configured either as an I<sup>2</sup>C master or as an I<sup>2</sup>C slave. The pins for the I<sup>2</sup>C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I<sup>2</sup>C components.

When the IP core is configured as master, it will be able to control other devices on the I<sup>2</sup>C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I<sup>2</sup>C Master. The I<sup>2</sup>C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both

For further information on the User I<sup>2</sup>C, please refer to TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#).

## User SPI IP

The iCE40 Ultra devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#).

## High Current LED Drive I/O Pins

The iCE40 Ultra family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 Ultra product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RGB LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

Supply Voltage $V_{CC}$	–0.5 V to 1.42 V
Output Supply Voltage $V_{CCIO}$	–0.5 V to 3.60 V
NVCM Supply Voltage $V_{PP\_2V5}$	–0.5 V to 3.60 V
PLL Supply Voltage $V_{CCPLL}$	–0.5 V to 1.42 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature ( $T_J$ )	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

### Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter		Min.	Max.	Units
V <sub>CC</sub> <sup>1</sup>	Core Supply Voltage		1.14	1.26	V
V <sub>PP_2V5</sub>	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71 <sup>4</sup>	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage	V <sub>CCIO_0</sub> , SPI_V <sub>CCIO1</sub> , V <sub>CCIO_2</sub>	1.71	3.46	V
V <sub>CCPLL</sub>	PLL Supply Voltage		1.14	1.26	V
t <sub>JCOM</sub>	Junction Temperature Commercial Operation		0	85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation		−40	100	°C
t <sub>PROG</sub>	Junction Temperature NVCM Programming		10.00	30.00	°C

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to [Power-Up Supply Sequencing](#) section.  $V_{CC}$  and  $V_{CCPLL}$  are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.
4.  $V_{PP\_2V5}$  can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise,  $V_{PP\_2V5}$  must be connected to a power supply with a minimum 2.30 V level.

### Power Supply Ramp Rates<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
$t_{RAMP}$	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to [Power-Up Supply Sequencing](#) section.

### Power-On Reset

All iCE40 Ultra devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1)  $V_{CC}$ , (2)  $SPI\_V_{CCIO1}$  and (3)  $V_{PP\_2V5}$ . All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

### Power-Up Supply Sequencing

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5V, or higher, before any subsequent power supplies in the sequence are applied.

1.  **$V_{CC}$  and  $V_{CCPLL}$**  should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the  $V_{CCPLL}$  (Please refer to TN1252, [iCE40 Hardware Checklist](#).)
2.  **$SPI\_V_{CCIO1}$**  should be the next supply, and can be applied any time after the previous supplies ( $V_{CC}$  and  $V_{CCPLL}$ ) have reached as level of 0.5 V or higher.
3.  **$V_{PP\_2V5}$**  should be the next supply, and can be applied any time after previous supplies ( $V_{CC}$ ,  $V_{CCPLL}$  and  $SPI\_V_{CCIO1}$ ) have reached a level of 0.5 V or higher.
4. **Other Supplies** ( $V_{CCIO0}$  and  $V_{CCIO2}$ ) do not affect device power-up functionality, and they can be applied any time after the initial power supplies ( $V_{CC}$  and  $V_{CCPLL}$ ) have reached a level of 0.5 V or greater.

There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are repowered up again.

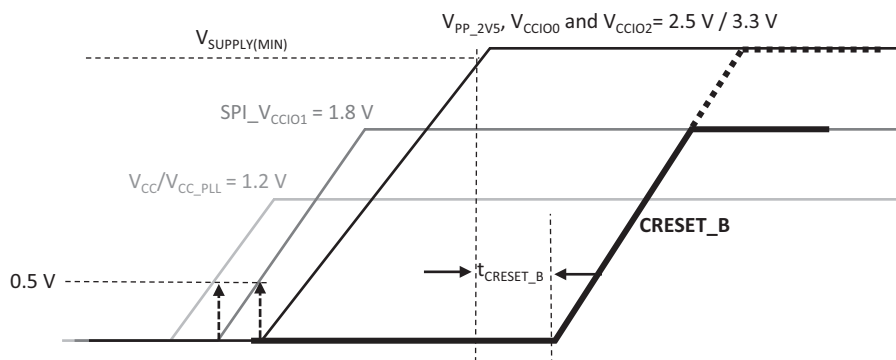
### External Reset

When all power supplies have reached to their minimum operating voltage defined in Minimum Operation Condition Table, it is required to either keep  $CRESET\_B$  LOW, or toggle  $CRESET\_B$  from HIGH to LOW, for a duration of  $t_{CRESET\_B}$ , and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory.

Figure 3-1 shows Power-Up sequence when  $SPI\_V_{CCIO1}$  and  $V_{PP\_2V5}$  are connected separately, and the  $CRESET\_B$  signal triggers configuration download. Figure 3-2 shows when  $SPI\_V_{CCIO1}$  and  $V_{PP\_2V5}$  connected together.

All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

**Figure 3-1. Power Up Sequence with  $SPI\_V_{CCIO1}$  and  $V_{PP\_2V5}$  Not Connected Together**



### Supply Current <sup>1, 2, 3, 4, 5</sup>

Symbol	Parameter	Typ. $V_{CC} = 1.2 V^4$	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	71	$\mu A$
$I_{PP2V5STDBY}$	$V_{PP\_2V5}$ Power Supply Static Current	0.55	$\mu A$
$I_{SPI\_VCCIO1STDBY}$	$SPI\_V_{CCIO1}$ Power Supply Static Current	0.5	$\mu A$
$I_{CCIOSTDBY}$	$V_{CCIO}$ Power Supply Static Current	0.5	$\mu A$
$I_{CCPEAK}$	Core Power Supply Startup Peak Current	8.0	mA
$I_{PP\_2V5PEAK}$	$V_{PP\_2V5}$ Power Supply Startup Peak Current	7.0	mA
$I_{SPI\_VCCIO1PEAK}$	$SPI\_V_{CCIO1}$ Power Supply Startup Peak Current	9.0	mA
$I_{CCIOPEAK}$	$V_{CCIO}$ Power Supply Startup Peak Current	7.5	mA

- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
- Frequency = 0 MHz.
- $T_J = 25^\circ C$ , power supplies at nominal voltage, on devices processed in nominal process conditions.
- Does not include pull-up.
- Startup Peak Currents are measured with decoupling capacitance of 0.1  $\mu F$ , 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.

### User I<sup>2</sup>C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
$f_{SCL}$	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
$t_{HI}$	SCL clock HIGH Time	4	—	—	0.6	—	—	$\mu s$
$t_{LO}$	SCL clock LOW Time	4.7	—	—	1.3	—	—	$\mu s$
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	$\mu s$
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	$\mu s$
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	$\mu s$
$t_{BUF}$	Bus free time between STOP and START	4.7	—	—	1.3	—	—	$\mu s$
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	$\mu s$

### User SPI Specifications <sup>1, 2</sup>

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
$f_{MAX}$	Maximum SCK clock frequency	—	—	45	MHz

- All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software tools. These parameters include the following:
  - $t_{SUmater}$  master Setup time (master mode)
  - $t_{HOLDmaster}$  master Hold time (master mode)
  - $t_{SUslave}$  slave Setup time (slave mode)
  - $t_{HOLDslave}$  slave Hold time (slave mode)
  - $t_{SCK2OUT}$  SCK to out (slave mode)
- The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW ( $t_{HI}$ ,  $t_{LO}$ ) time.

## Internal Oscillators (HFOSC, LFOSC)<sup>1</sup>

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f <sub>CLKHF</sub>	Commercial Temp	HFOSC clock frequency (t <sub>J</sub> = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t <sub>J</sub> = –40 °C–100 °C)	–20%	48	20%	MHz
f <sub>CLKLF</sub>		LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH <sub>CLKHF</sub>	Commercial Temp	HFOSC clock frequency (t <sub>J</sub> = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC clock frequency (t <sub>J</sub> = –45 °C–100 °C)	40	50	60	%
DCH <sub>CLKLF</sub>		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

1. Glitchless enabling and disabling OSC clock outputs.

## sysIO Recommended Operating Conditions

Standard	V <sub>CCIO</sub> (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89

## sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> Max. (V)	V <sub>OH</sub> Min. (V)	I <sub>OL</sub> Max. (mA)	I <sub>OH</sub> Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	–0.3	0.8	2.0	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> – 0.4	8	–8
					0.2	V <sub>CCIO</sub> – 0.2	0.1	–0.1
LVC MOS 2.5	–0.3	0.7	1.7	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> – 0.4	6	–6
					0.2	V <sub>CCIO</sub> – 0.2	0.1	–0.1
LVC MOS 1.8	–0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> – 0.4	4	–4
					0.2	V <sub>CCIO</sub> – 0.2	0.1	–0.1

## Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V <sub>REF</sub>	Reference Voltage to compare, on V <sub>INM</sub>	V <sub>CCIO</sub> = 2.5 V	0.25	V <sub>CCIO</sub> – 0.25 V	V
V <sub>DIFFIN_H</sub>	Differential input HIGH (V <sub>INP</sub> – V <sub>INM</sub> )	V <sub>CCIO</sub> = 2.5 V	250	—	mV
V <sub>DIFFIN_L</sub>	Differential input LOW (V <sub>INP</sub> – V <sub>INM</sub> )	V <sub>CCIO</sub> = 2.5 V	—	–250	mV
I <sub>IN</sub>	Input Current, V <sub>INP</sub> and V <sub>INM</sub>	V <sub>CCIO</sub> = 2.5 V	–10	10	μA

### iCE40 Ultra Family Timing Adders

Over Recommended Commercial Operating Conditions<sup>1, 2, 3</sup>

Buffer Type	Description	Timing (Typ.)	Units
<b>Input Adjusters</b>			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.18	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.19	ns
<b>Output Adjusters</b>			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	-0.12	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.32	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

### iCE40 Ultra External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	Min	Max	Units
<b>Clocks</b>					
<b>Global Clocks</b>					
$f_{\text{MAX\_GBUF}}$	Frequency for Global Buffer Clock network	All devices	—	185	MHz
$t_{\text{W\_GBUF}}$	Clock Pulse Width for Global Buffer	All devices	2	—	ns
$t_{\text{SKEW\_GBUF}}$	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
<b>Pin-LUT-Pin Propagation Delay</b>					
$t_{\text{PD}}$	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock without PLL)<sup>1</sup></b>					
$t_{\text{SKEW\_IO}}$	Data bus skew across a bank of IOs	All devices	—	410	ps
$t_{\text{CO}}$	Clock to Output – PIO Output Register	All devices	—	9.0	ns
$t_{\text{SU}}$	Clock to Data Setup – PIO Input Register	All devices	-0.5	—	ns
$t_{\text{H}}$	Clock to Data Hold – PIO Input Register	All devices	5.55	—	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock with PLL)</b>					
$t_{\text{COPLL}}$	Clock to Output – PIO Output Register	All Devices	—	2.9	ns
$t_{\text{SUPLL}}$	Clock to Data Setup – PIO Input Register	All Devices	5.9	—	ns
$t_{\text{HPLL}}$	Clock to Data Hold – PIO Input Register	All Devices	-0.6	—	ns

1. All the data is from the worst case condition.

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
$f_{OUT}$	Output Clock Frequency (PLLOUT)		16	275	MHz
$f_{VCO}$	PLL VCO Frequency		533	1066	MHz
$f_{PFD}$	Phase Detector Input Frequency		10	133	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle		40	60	%
$t_{PH}$	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1, 5, 6}$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	450	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \geq 100$ MHz	—	750	ps p-p
		$f_{OUT} < 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 25$ MHz	—	275	ps p-p
		$f_{PFD} < 25$ MHz	—	0.05	UIPP
$t_W$	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	μs
$t_{UNLOCK}$	PLL Unlock Time		—	50	ns
$t_{IPJIT}^4$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{STABLE}^3$	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE\_PW}^3$	LATCHINPUTVALUE Pulse Width		100	—	ns
$t_{RST}$	RESET Pulse Width		10	—	ns
$t_{RSTREC}$	RESET Recovery Time		10	—	μs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## sysDSP Timing

### Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

### Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V <sub>CC</sub>		Power	—	Core Power Supply
V <sub>CCIO_0</sub> , SPI_V <sub>CCIO1</sub> , V <sub>CCIO_2</sub>		Power	—	Power for I/Os in Bank 0, 1 and 2.
V <sub>PP_2V5</sub>		Power	—	Power for NVCM programming and operations.
V <sub>CCPLL</sub>		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V <sub>CCIO_1</sub> .
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V <sub>CCIO1</sub> .
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V <sub>CCIO1</sub> .
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V <sub>CCIO1</sub> .
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.



Signal Name		Function	I/O	Description
PIOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer
PIOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer
PIOT_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer
PIOT_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer
PIOT_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED

## Pin Information Summary

Pin Type		iCE5LP1K			iCE5LP2K			iCE5LP4K		
		CM36	SWG36	SG48 <sup>1</sup>	CM36	SWG36	SG48 <sup>1</sup>	CM36	SWG36	SG48 <sup>1</sup>
General Purpose I/O Per Bank	Bank 0	12	5	17	12	5	17	12	5	17
	Bank 1	4	15	14	4	15	14	4	15	14
	Bank 2	10	6	8	10	6	8	10	6	8
Total General Purpose I/Os		26	26	39	26	26	39	26	26	39
V <sub>CC</sub>		1	1	2	1	1	2	1	1	2
V <sub>CCIO</sub>	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V <sub>CCPLL</sub>		1	1	1	1	1	1	1	1	1
V <sub>PP_2V5</sub>		1	1	1	1	1	1	1	1	1
Dedicated Config Pins		1	1	2	1	1	2	1	1	2
GND		2	2	0	2	2	0	2	2	0
GND_LED		1	1	0	1	1	0	1	1	0
Total Balls		36	36	48	36	36	48	36	36	48

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.



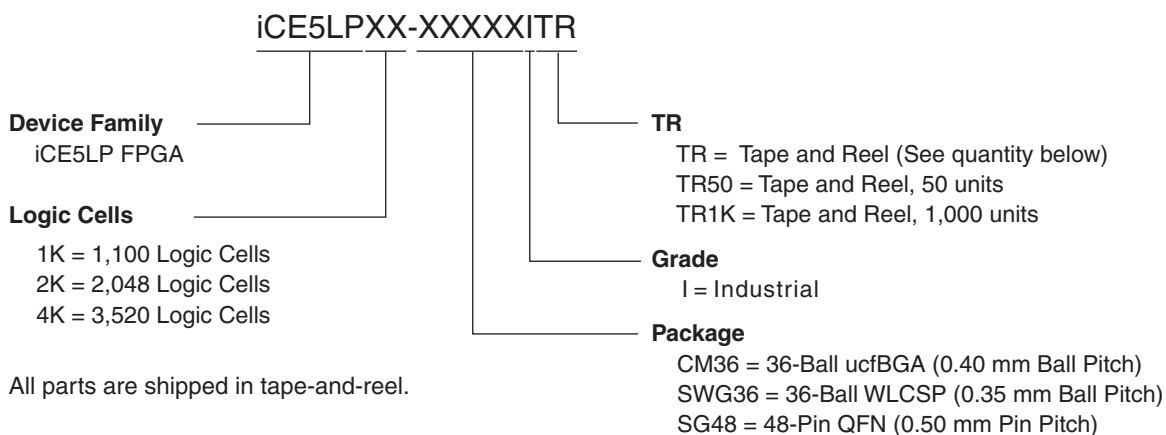
# iCE40 Ultra Family Data Sheet

## Ordering Information

June 2016

Data Sheet DS1048

### iCE5LP Part Number Description



### Tape and Reel Quantity

Package	TR Quantity
CM36	4,000
SWG36	5,000
SG48	2,000

## Ordering Part Numbers

### Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM361TR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM361TR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM361TR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG361TR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG361TR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG361TR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG481TR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG481TR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM361TR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM361TR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM361TR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG361TR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG361TR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG361TR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG481TR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG481TR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM361TR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM361TR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM361TR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG361TR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG361TR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG361TR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG481TR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG481TR50	3520	1.2 V	Halogen-Free QFN	48	IND

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
			Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
			Replaced RGB PWM Block section with Embedded PWM IP section.
		DC and Switching Characteristics	Removed RGB PWM Block Timing section.
April 2014	01.0	All	Initial release.