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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	256
Number of Logic Elements/Cells	2048
Total RAM Bits	81920
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-XFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.1x2.1)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp2k-swg36itr

Table 1-1. iCE40 Ultra Family Selection Guide

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
Logic Cells (LUT + Flip-Flop)	**1100**	**2048**	**3520**
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
Packages, ball pitch, dimension	**Total User I/O Count**		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39

Introduction

The iCE40 Ultra family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), on-chip Oscillators (LFOSC, HFOSC), two hardened I^2C Controllers, two hardened SPI Controllers, three 24 mA RGB LED open-drain drivers, a 500 mA IR LED open-drain drivers, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 Ultra FPGAs are available in very small form factor packages, as small as 2.078 mm x 2.078 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 Ultra devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 Ultra devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 Ultra family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 Ultra. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 Ultra device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides in the iCE40 Ultra 1K and 2K device the embedded RGB PWM IP at no extra cost of LUT available to the user, to perform controlling the RGB LED function. This embedded IP allow users to control color, LED ON/OFF time, and breathe rate of the LED. For more information, please refer to Usage Guide in Lattice Design Software.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 Ultra FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, please contact your local Lattice representative.

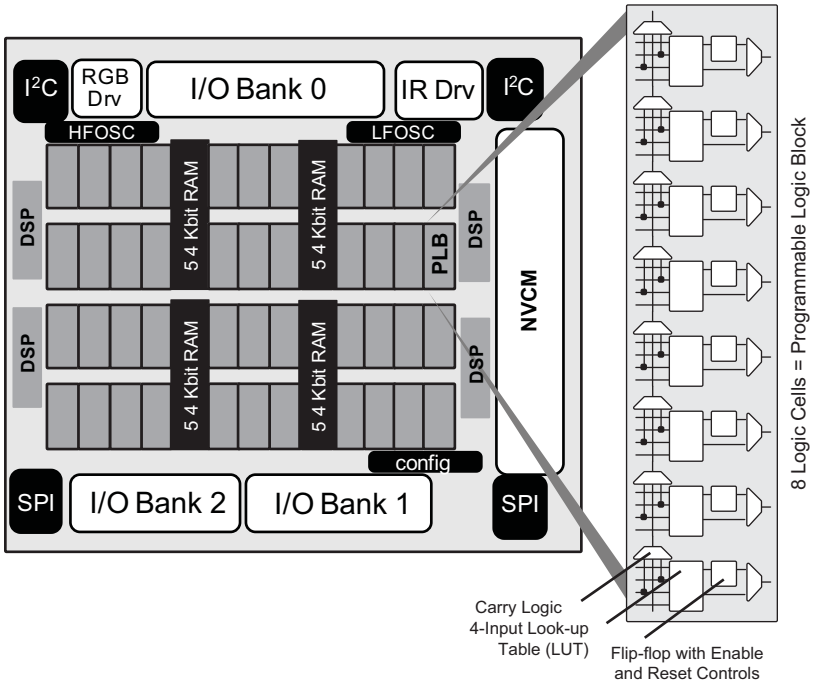
iCE40 Ultra Family Data Sheet Architecture

June 2016 Data Sheet DS1048

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks.

Routing

There are many resources provided in the iCE40 Ultra devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 Ultra device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40 Ultra External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 Ultra device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 Ultra device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 Ultra devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 Ultra global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 Ultra PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

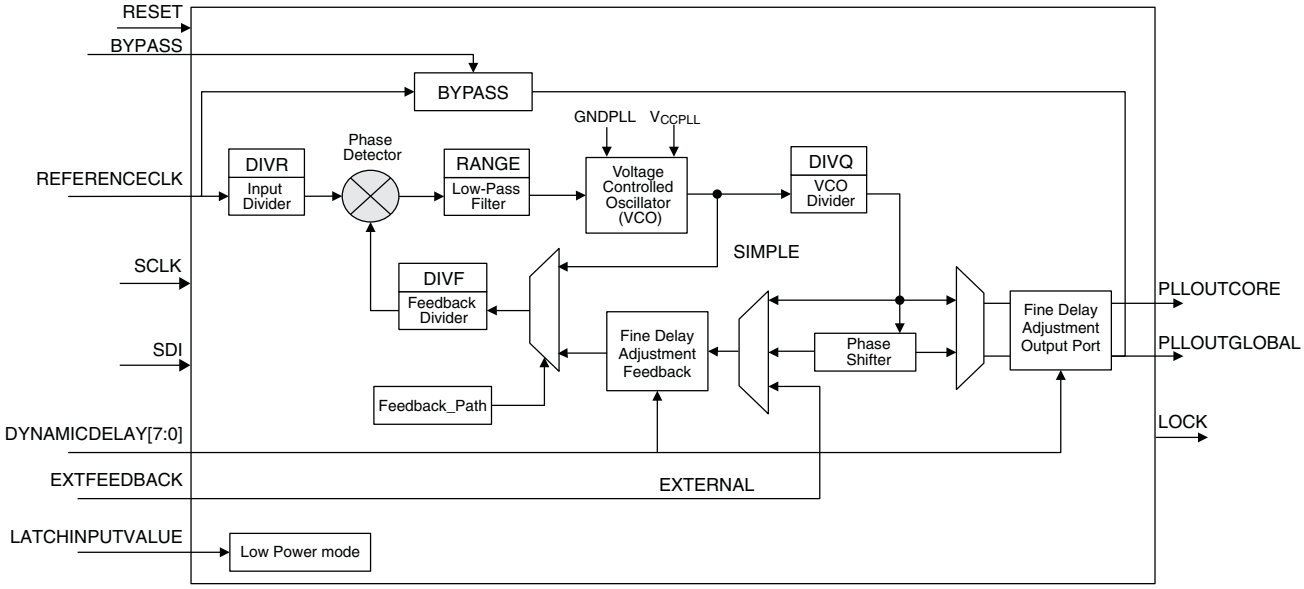


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 Ultra device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock, falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

Figure 2-6. sysDSP 8-bit x 8-bit Multiplier

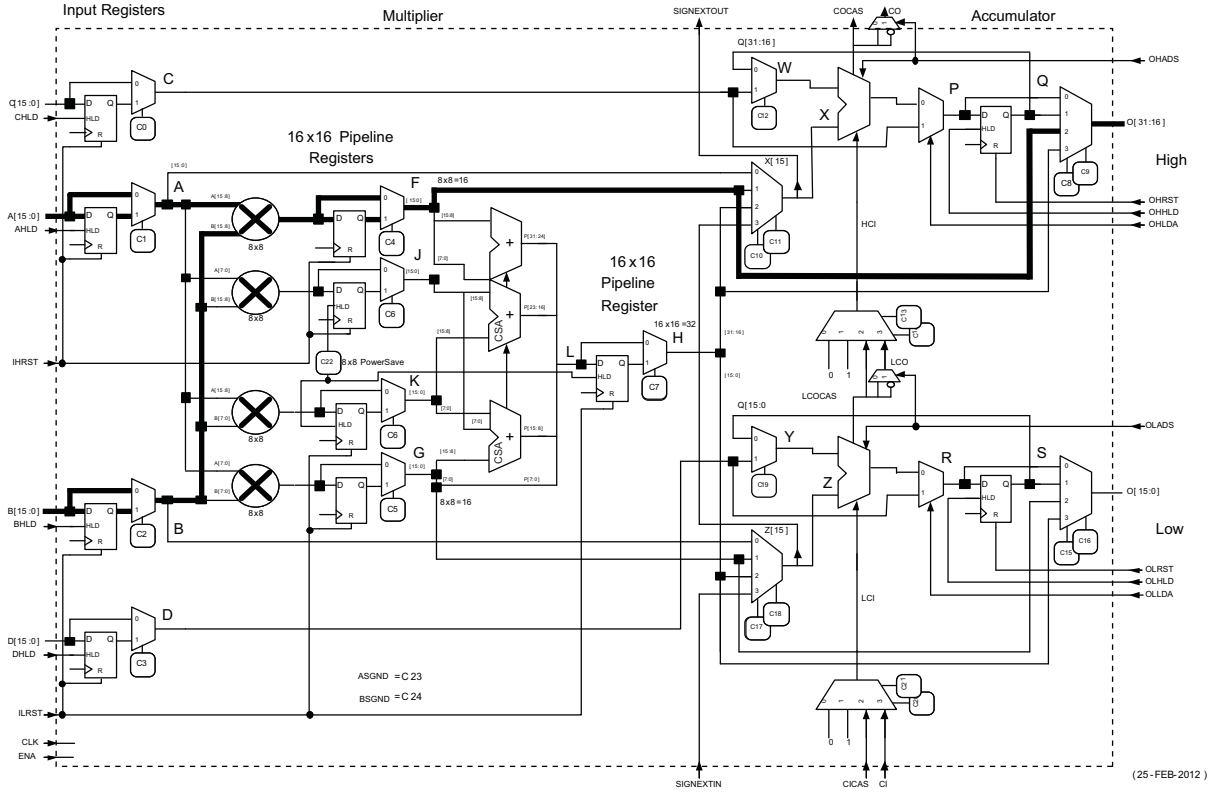


Figure 2-7 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

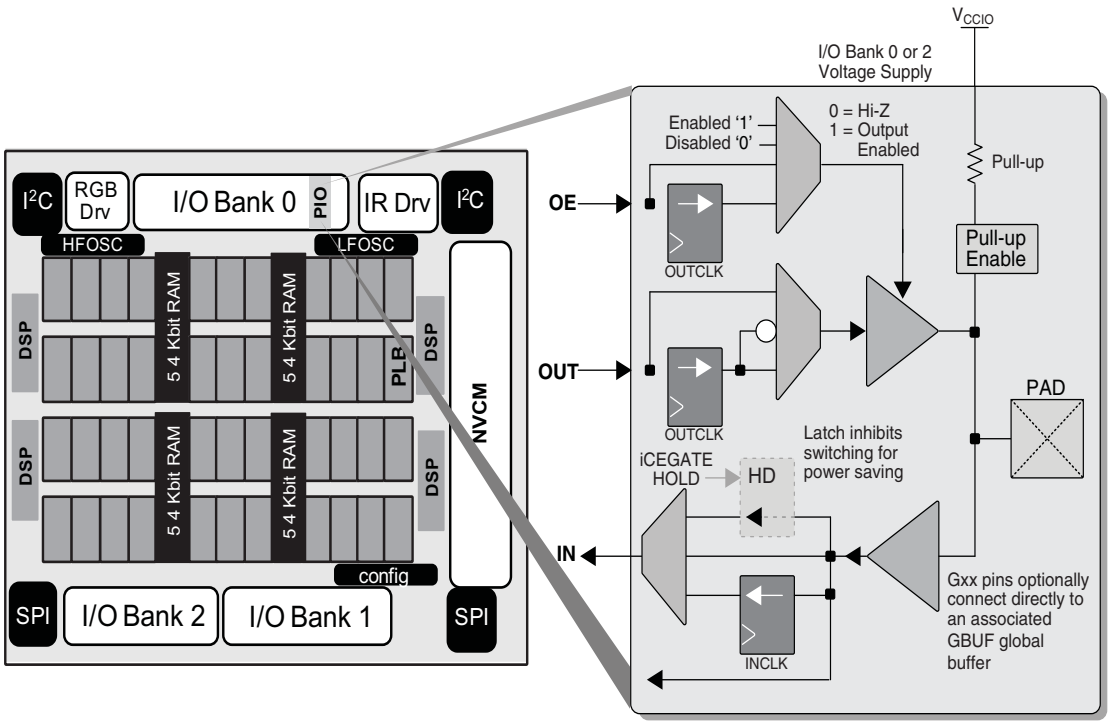
sysIO Buffer Banks

iCE40 Ultra devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-8. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-9 shows the input/output register block for the PIOs.

iCE40 Ultra Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.60 V

NVCM Supply Voltage V_{PP_2V5} . . . . . –0.5 V to 3.60 V

PLL Supply Voltage V_{CCPLL} . . . . . –0.5 V to 1.42 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . . –65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

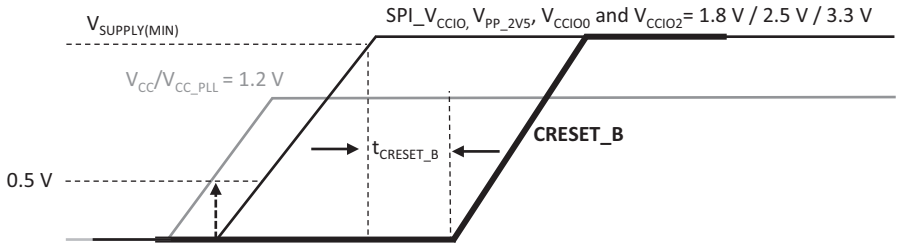
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	0V < V_{IN} < V_{CCIO} + 0.2 V	—	—	+/–10	µA
C_1	I/O Capacitance, excluding LED Drivers[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_3	RGB Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	15	—	pF
C_4	IRLED Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	53	—	pF
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Supply Current [1, 2, 3, 4, 5]

Symbol	Parameter	Typ. V_{CC} = 1.2 V[4]	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	71	µA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	0.55	µA
$I_{SPI\_VCCIO1STDBY}$	SPI_V_{CCIO1} Power Supply Static Current	0.5	µA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	0.5	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	8.0	mA
$I_{PP\_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	7.0	mA
$I_{SPI\_VCCIO1PEAK}$	SPI_V_{CCIO1} Power Supply Startup Peak Current	9.0	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	7.5	mA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage, on devices processed in nominal process conditions.
4. Does not include pull-up.
5. Startup Peak Currents are measured with decoupling capacitance of 0.1 uF, 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.

User I^2C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

User SPI Specifications[1, 2]

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software tools. These parameters include the following:
   - — $t_{SUmaster}$ master Setup time (master mode)
   - — $t_{HOLDmaster}$ master Hold time (master mode)
   - — $t_{SUslave}$ slave Setup time (slave mode)
   - — $t_{HOLDslave}$ slave Hold time (slave mode)
   - — $t_{SCK2OUT}$ SCK to out (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI}, t_{LO}) time.

Typical Building Block Function Performance[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the Lattice Design Software tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Under worst case operating conditions.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Measured with a toggling pattern

iCE40 Ultra Family Timing Adders

Over Recommended Commercial Operating Conditions[1, 2, 3]

Buffer Type	Description	Timing (Typ.)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

iCE40 Ultra External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	Min	Max	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	410	ps
t_{CO}	Clock to Output – PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	5.9	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–0.6	—	ns

1. All the data is from the worst case condition.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time[4]		9.9	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

Pin Information Summary

Pin Type		iCE5LP1K			iCE5LP2K			iCE5LP4K		
		CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]
General Purpose I/O Per Bank	Bank 0	12	5	17	12	5	17	12	5	17
	Bank 1	4	15	14	4	15	14	4	15	14
	Bank 2	10	6	8	10	6	8	10	6	8
Total General Purpose I/Os		26	26	39	26	26	39	26	26	39
V_{CC}		1	1	2	1	1	2	1	1	2
V_{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V_{CCPLL}		1	1	1	1	1	1	1	1	1
V_{PP_2V5}		1	1	1	1	1	1	1	1	1
Dedicated Config Pins		1	1	2	1	1	2	1	1	2
GND		2	2	0	2	2	0	2	2	0
GND_LED		1	1	0	1	1	0	1	1	0
Total Balls		36	36	48	36	36	48	36	36	48

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM36ITR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG36ITR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG48ITR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG48ITR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM36ITR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG36ITR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG48ITR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG48ITR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM36ITR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG36ITR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG48ITR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG48ITR50	3520	1.2 V	Halogen-Free QFN	48	IND

iCE40 Ultra Family Data Sheet Revision History

June 2016 **Data Sheet DS1048**

Date	Version	Section	Change Summary
June 2016	2.0	Introduction	Updated General Description section. Changed “high current driver” to “high current IR driver”.
			Updated Features section. In Table 1-1, iCE40 Ultra Family Selection Guide, corrected HF Oscillator (48 kHz) to (48 MHz).
		Architecture	Updated Architecture Overview section. — Changed content to “The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks." — Changed “high current LED sink” to "high current RGB and IR LED sinks".
			Updated sysCLOCK Phase Locked Loops (PLLs) section. Corrected V_{CCPLL} character format in Figure 2-3, PLL Diagram.
			Updated sysMEM Embedded Block RAM Memory section. Updated footnote in Table 2-4, sysMEM Block Configurations.
			Updated sysIO Buffer Banks section. — Changed statement to “The configuration SPI interface signals are powered by SPI_V_{CCIO1}.” — Corrected V_{CCIO} character format in Figure 2-8, I/O Bank and Programmable I/O Cell.
			Updated Typical I/O Behavior During Power-up section. Modified text content.
			Updated Supported Standards section. Changed statement to “The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators.”
			Updated On-Chip Oscillator section. Changed statement to “The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option.”
			Updated section heading to High Current LED Drive I/O Pins. Changed “high current drive” to “high current LED drive”.
			Removed Power On Reset section.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. — Corrected symbol character format.
			Updated Recommended Operating Conditions section. — Corrected symbol character format. — Revised footnote 1. — Added footnote 4.
			Updated Power Supply Ramp Rates section. Changed t_{RAMP} Max. value.
			Added Power-On Reset section.
			Updated section heading to Power-Up Supply Sequencing. Revised text content.
			Added External Reset section.
			Updated DC Electrical Characteristics section. Revised footnote 4.

Date	Version	Section	Change Summary
			Updated Supply Current section. — Corrected $I_{PP2V5STDBY}$ parameter. — Added Typ. VCC = 1.2 V values for I_{CCPEAK}, $I_{PP\_2V5PEAK}$, $I_{SPI\_VCCIO1PEAK}$, and $I_{CCIOPEAK}$. — Added footnote 5. — Corrected S_{PI_VCCIO1} character format.
			Updated User SPI Specifications section. Removed parameters and added footnotes.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for DCH_{CLKHF}.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Removed footnote.
			Updated Register-to-Register Performance section. Modified footnotes.
			Updated iCE40 Ultra External Switching Characteristics section. Modified footnote.
			Updated sysCLOCK PLL Timing section. Reversed t_{OPJIT} conditions.
			Updated sysCONFIG Port Timing Specifications section. — Modified t_{CR_SCK} Min. value. — Added footnote 4 to t_{SU} parameter. — Modified t_{SU} Min. value. — Modified t_{HD} parameter.
			Updated section heading to RGB LED and IR LED Drive. Modified ILED_ACCURACY and IIR_ACCURACY parameters, Min. and Max. values.
		Pinout Information	Updated Signal Descriptions section. Changed V_{CCIO_1} to SPI_V_{CCIO1} in the CDONE, CRESETB and PIOB_xx descriptions.
			Updated Pin Information Summary section. — Corrected symbol character format. — Corrected VCPP_2V5 to V_{PP_2V5}.
	1.9	Introduction	Updated Features section. Updated BGA package to ucfBGA.
		DC and Switching Characteristics	Updated Differential Comparator Electrical Characteristics section. Corrected typo in V_{REF} Max. value.
		Pinout Information	Updated Signal Descriptions section. — Changed PIOB_12a to PIOB_xx — Changed SPI_CSN to SPI_SS_B and revised description when in Slave SPI mode. — Corrected minor typo errors.
			Updated Pin Information Summary section. Added footnote to SG48.
		Ordering Information	Updated iCE5LP Part Number Description section. Updated BGA package to ucfBGA.
			Updated Ordering Part Numbers section. Updated BGA package to ucfBGA.
June 2015	1.8	DC and Switching Characteristics	Updated Internal Oscillators (HFOSC, LFOSC) section. Removed decimals.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added TR items. — Corrected formatting errors.
			Updated Ordering Part Numbers section. Updated CM36 and SG48 packages.

Date	Version	Section	Change Summary
April 2015	1.7	Architecture	Updated sysDSP section. Revised the following figures: — Figure 2-5, sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate) — Figure 2-6, sysDSP 8-bit x 8-bit Multiplier — Figure 2-7, DSP 16-bit x 16-bit Multiplier
		Ordering Information	Updated iCE5LP Part Number Description section. Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
March 2015	1.6	Introduction	Updated Features section. — Added BGA and QFN packages in Flexible Logic Architecture. — Added USB 3.1 Type C Cable Detect / Power Delivery Applications in Applications. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added 36-ball ucfBGA and 48-ball QFN packages. Changed subheading to Total User I/O Count. Changed RBW IP to PWM IP. Deleted footnotes.
		DC and Switching Characteristics	Updated Power-up Sequence section. Indicated all devices in second paragraph.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.
			Replaced the Differential Comparator Electrical Characteristics table.
		Pinout Information	Updated Pin Information Summary section. — Added CM36 and SG48 values. — Changed CRESET_B to Dedicated Config Pins.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added CM36 and SG48 package. — Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
October 2014	1.5	Introduction	Updated Features section. — Removed 26 I/O pins for 36-pin WLCSP under Flexible Logic Architecture. — Changed form factor to 2.078 mm x 2.078 mm. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 20-Ball WLCSP.
			Updated Introduction section. Changed form factor to 2.078 mm x 2.078 mm.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) section. Removed note in heading regarding sysCLOCK PLL support.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Removed footnote on sysCLOCK PLL support.
			Updated Power-up Sequence section. Removed information on 20-pin WLCSP.
		Pinout Information	Updated Signal Descriptions section. Removed references 20-pin WLCSP.
			Updated Pin Information Summary section. Removed references to UWG20 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 20-ball WLCSP.
			Updated Ordering Part Numbers section. Removed UWG20 part numbers.
		Further Information	Added technical note references.

Date	Version	Section	Change Summary
August 2014	1.4	All	Removed Preliminary document status.
		Introduction	Updated General Description section. Added information on high current driver.
			Updated Features section. — Changed standby current typical to as low as 71 µA. — Changed feature to Embedded Memory. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added NVCM and Embedded PWM IP rows. Added (MULT16 with 32-bit Accumulator) to DSP Block. Added Total I/O (Dedicated I/O) Count data.
			General update to Introduction section.
		Architecture	Updated Architecture Overview section. — Revised and added information on sysIO banks. — Updated reference for embedded PWM IP.
			Updated iCE40 Ultra Programming and Configuration section. — Changed SPI1 to SPI. — Changed VCCIO_1 to SPI_V_{CCIO1}.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Changed PLL Supply Voltage VCCPLL value.
			Updated Recommended Operating Conditions section. Added footnote to VCCPLL.
			Updated Power-up Sequence section. General update.
			Updated Power-On-Reset Voltage Levels section. Changed the V_{PORUP} V_{CC} Max.value.
			Updated DC Electrical Characteristics section. Added C_3 and C_4 information.
			Updated Supply Current section. — Completed Typ. VCC =1.2 V4 data. — Changed symbols to $I_{SPI\_VCCIO1STDBY}$ and $I_{SPI\_VCCIO1PEAK}$. — Added information to footnote 3.
			Updated Internal Oscillators (HFOSC, LFOSC) section. General update.
			Updated iCE40 Ultra External Switching Characteristics section. Added Max. value for t_{COPLL}. Added Min. values for t_{SUPLL} and t_{HPLL}.
			Updated sysCLOCK PLL Timing section. Added Max. value for t_{OPJIT}.
			Updated sysCONFIG Port Timing Specifications section. — Added T_{SU} and T_{HD} information. — Added footnote 3 to Master SPI.
			Updated High Current LED and IR LED Drive section. Updated Min. value.
July 2014	1.3	All	Changed document status from Advance to Preliminary.
		Introduction	Updated Features section. Adjusted Ultra-low Power Devices standby current.
		DC and Switching Characteristics	Updated AC/DC specifications numbers.