Lattice Semiconductor Corporation - ICE5LP2K-UWG20ITR Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	256
Number of Logic Elements/Cells	2048
Total RAM Bits	81920
Number of I/O	12
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (1.71x2.06)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp2k-uwg20itr

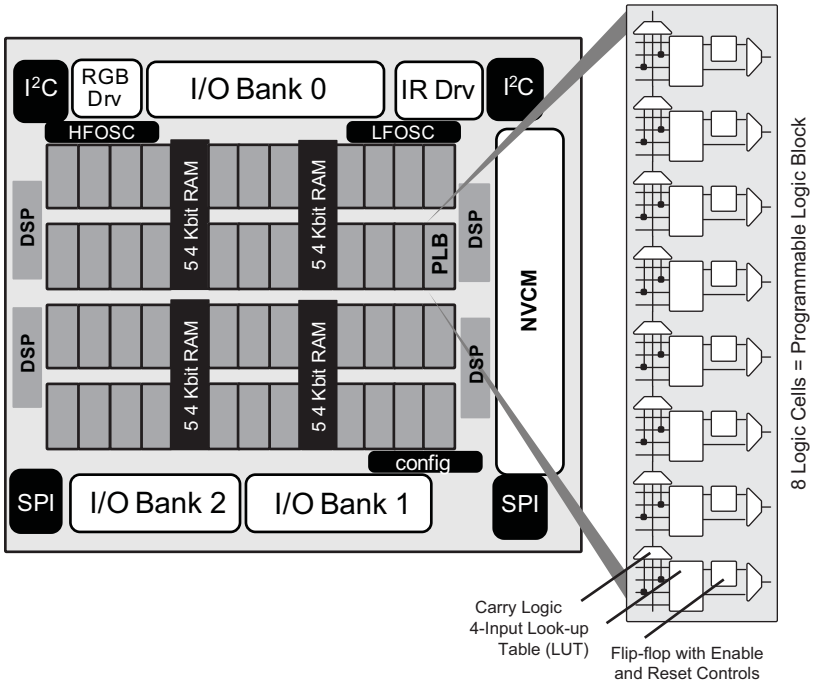
iCE40 Ultra Family Data Sheet Architecture

June 2016 Data Sheet DS1048

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks.

Routing

There are many resources provided in the iCE40 Ultra devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 Ultra device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40 Ultra External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 Ultra device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 Ultra device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 Ultra device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock, falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

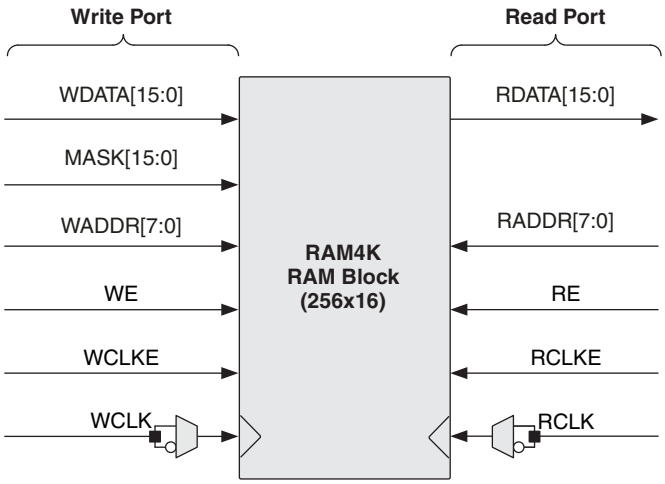


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

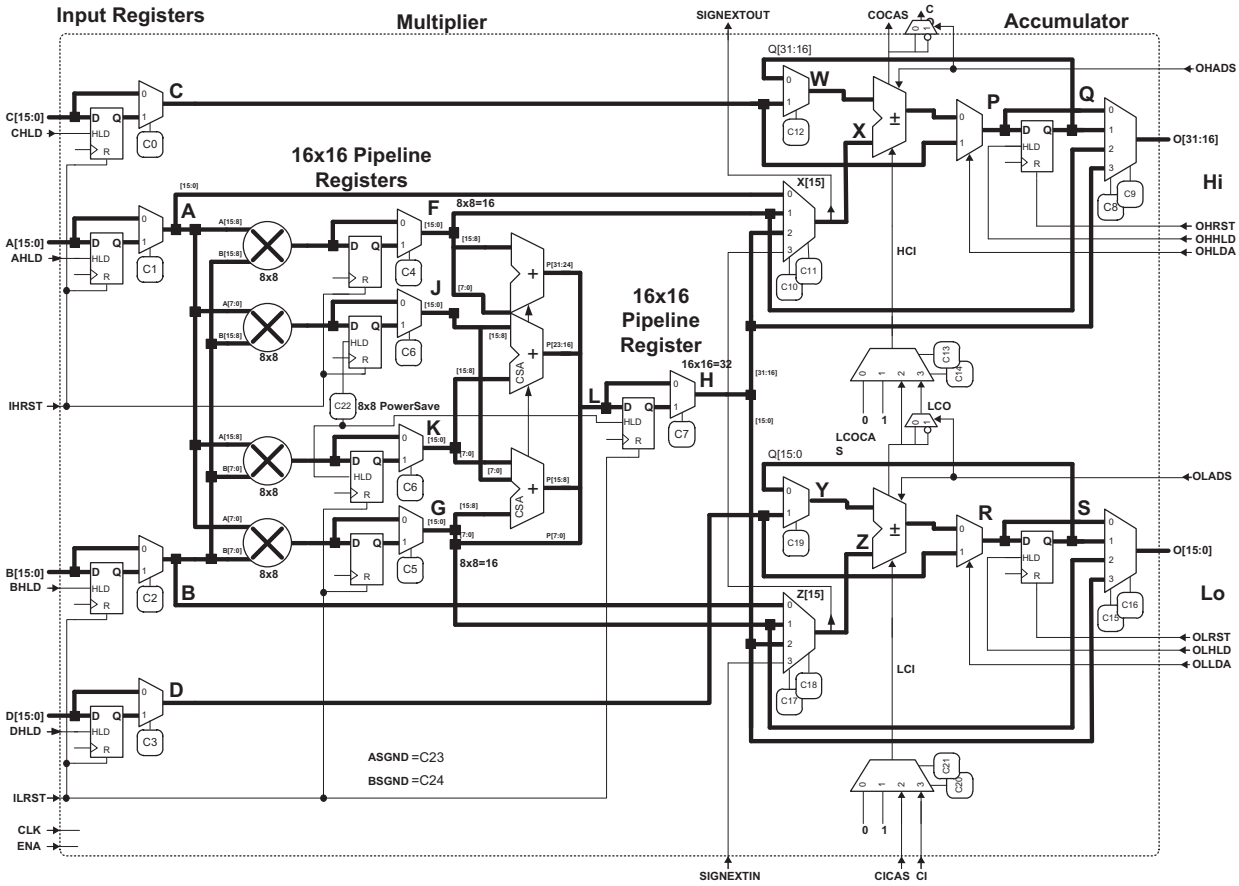
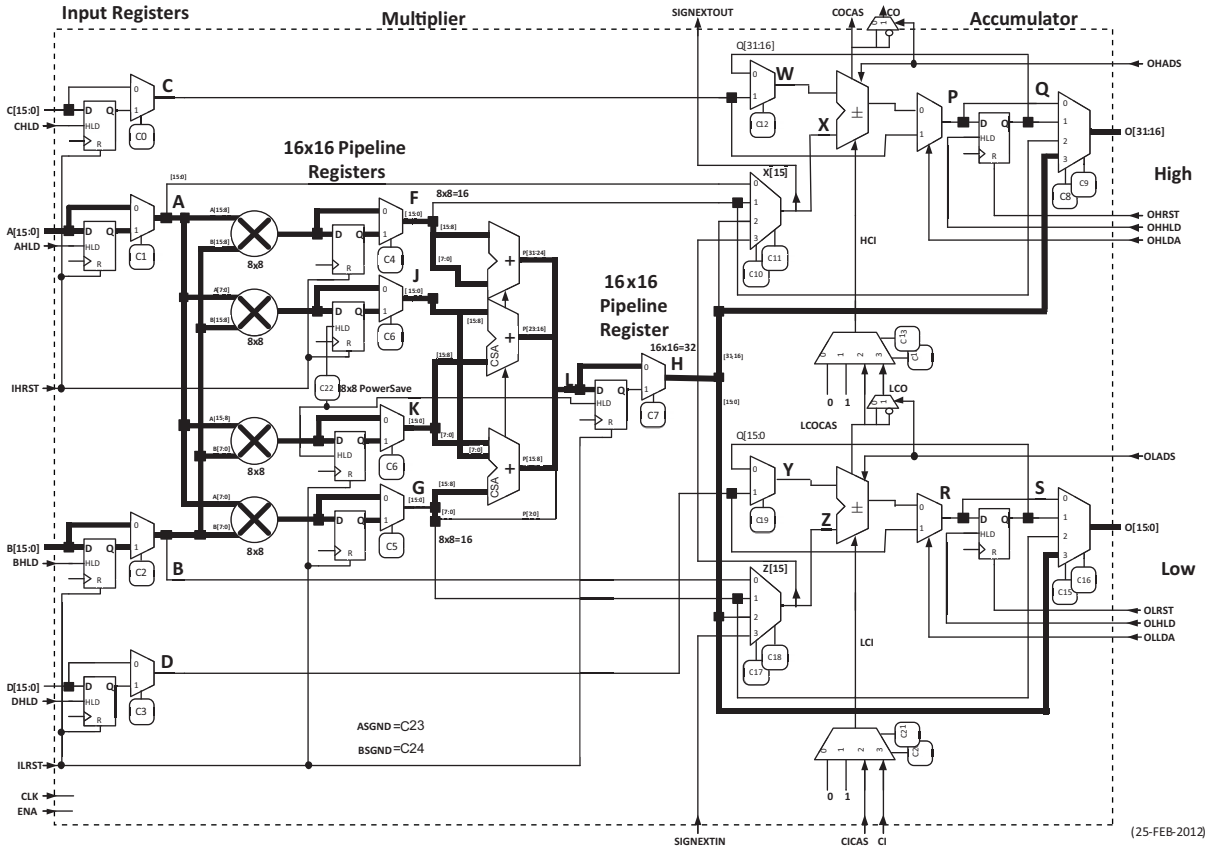


Figure 2-7. DSP 16-bit x 16-bit Multiplier



Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-8 and Table 2-9 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 Ultra devices.

Differential Comparators

The iCE40 Ultra devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-8. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-9. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

On-Chip Oscillator

The iCE40 Ultra devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

User I²C IP

The iCE40 Ultra devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both

For further information on the User I²C, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

User SPI IP

The iCE40 Ultra devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

High Current LED Drive I/O Pins

The iCE40 Ultra family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 Ultra product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, iCE40 LED Driver Usage Guide.

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration.

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40 Ultra Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.60 V

NVCM Supply Voltage V_{PP_2V5} . . . . . –0.5 V to 3.60 V

PLL Supply Voltage V_{CCPLL} . . . . . –0.5 V to 1.42 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . . –65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

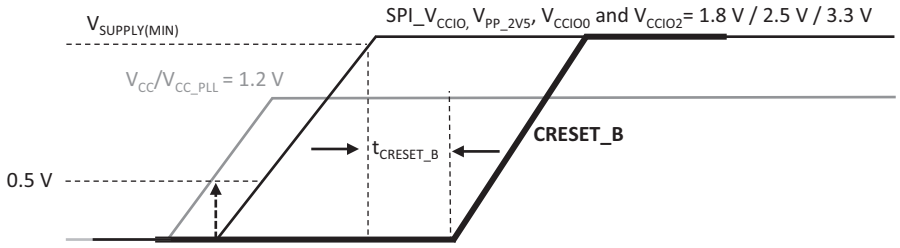
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	0V < V_{IN} < V_{CCIO} + 0.2 V	—	—	+/–10	µA
C_1	I/O Capacitance, excluding LED Drivers[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_3	RGB Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	15	—	pF
C_4	IRLED Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	53	—	pF
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

iCE40 Ultra Family Timing Adders

Over Recommended Commercial Operating Conditions[1, 2, 3]

Buffer Type	Description	Timing (Typ.)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

iCE40 Ultra External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	Min	Max	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	410	ps
t_{CO}	Clock to Output – PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	5.9	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–0.6	—	ns

1. All the data is from the worst case condition.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time[4]		9.9	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1 and 2.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations.
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V_{CCIO_1}.
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V_{CCIO1}.
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Signal Name	Function	I/O	Description
RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 500mA output to drive external LED
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location)
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location)

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM36ITR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG36ITR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG48ITR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG48ITR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM36ITR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG36ITR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG48ITR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG48ITR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM36ITR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG36ITR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG48ITR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG48ITR50	3520	1.2 V	Halogen-Free QFN	48	IND

Date	Version	Section	Change Summary
			Updated Supply Current section. — Corrected $I_{PP2V5STDBY}$ parameter. — Added Typ. VCC = 1.2 V values for I_{CCPEAK}, $I_{PP\_2V5PEAK}$, $I_{SPI\_VCCIO1PEAK}$, and $I_{CCIOPEAK}$. — Added footnote 5. — Corrected S_{PI_VCCIO1} character format.
			Updated User SPI Specifications section. Removed parameters and added footnotes.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for DCH_{CLKHF}.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Removed footnote.
			Updated Register-to-Register Performance section. Modified footnotes.
			Updated iCE40 Ultra External Switching Characteristics section. Modified footnote.
			Updated sysCLOCK PLL Timing section. Reversed t_{OPJIT} conditions.
			Updated sysCONFIG Port Timing Specifications section. — Modified t_{CR_SCK} Min. value. — Added footnote 4 to t_{SU} parameter. — Modified t_{SU} Min. value. — Modified t_{HD} parameter.
			Updated section heading to RGB LED and IR LED Drive. Modified ILED_ACCURACY and IIR_ACCURACY parameters, Min. and Max. values.
		Pinout Information	Updated Signal Descriptions section. Changed V_{CCIO_1} to SPI_V_{CCIO1} in the CDONE, CRESETB and PIOB_xx descriptions.
			Updated Pin Information Summary section. — Corrected symbol character format. — Corrected VCPP_2V5 to V_{PP_2V5}.
	1.9	Introduction	Updated Features section. Updated BGA package to ucfBGA.
		DC and Switching Characteristics	Updated Differential Comparator Electrical Characteristics section. Corrected typo in V_{REF} Max. value.
		Pinout Information	Updated Signal Descriptions section. — Changed PIOB_12a to PIOB_xx — Changed SPI_CSN to SPI_SS_B and revised description when in Slave SPI mode. — Corrected minor typo errors.
			Updated Pin Information Summary section. Added footnote to SG48.
		Ordering Information	Updated iCE5LP Part Number Description section. Updated BGA package to ucfBGA.
			Updated Ordering Part Numbers section. Updated BGA package to ucfBGA.
June 2015	1.8	DC and Switching Characteristics	Updated Internal Oscillators (HFOSC, LFOSC) section. Removed decimals.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added TR items. — Corrected formatting errors.
			Updated Ordering Part Numbers section. Updated CM36 and SG48 packages.

Date	Version	Section	Change Summary
August 2014	1.4	All	Removed Preliminary document status.
		Introduction	Updated General Description section. Added information on high current driver.
			Updated Features section. — Changed standby current typical to as low as 71 µA. — Changed feature to Embedded Memory. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added NVCM and Embedded PWM IP rows. Added (MULT16 with 32-bit Accumulator) to DSP Block. Added Total I/O (Dedicated I/O) Count data.
			General update to Introduction section.
		Architecture	Updated Architecture Overview section. — Revised and added information on sysIO banks. — Updated reference for embedded PWM IP.
			Updated iCE40 Ultra Programming and Configuration section. — Changed SPI1 to SPI. — Changed VCCIO_1 to SPI_V_{CCIO1}.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Changed PLL Supply Voltage VCCPLL value.
			Updated Recommended Operating Conditions section. Added footnote to VCCPLL.
			Updated Power-up Sequence section. General update.
			Updated Power-On-Reset Voltage Levels section. Changed the V_{PORUP} V_{CC} Max.value.
			Updated DC Electrical Characteristics section. Added C_3 and C_4 information.
			Updated Supply Current section. — Completed Typ. VCC =1.2 V4 data. — Changed symbols to $I_{SPI\_VCCIO1STDBY}$ and $I_{SPI\_VCCIO1PEAK}$. — Added information to footnote 3.
			Updated Internal Oscillators (HFOSC, LFOSC) section. General update.
			Updated iCE40 Ultra External Switching Characteristics section. Added Max. value for t_{COPLL}. Added Min. values for t_{SUPLL} and t_{HPLL}.
			Updated sysCLOCK PLL Timing section. Added Max. value for t_{OPJIT}.
			Updated sysCONFIG Port Timing Specifications section. — Added T_{SU} and T_{HD} information. — Added footnote 3 to Master SPI.
			Updated High Current LED and IR LED Drive section. Updated Min. value.
July 2014	1.3	All	Changed document status from Advance to Preliminary.
		Introduction	Updated Features section. Adjusted Ultra-low Power Devices standby current.
		DC and Switching Characteristics	Updated AC/DC specifications numbers.

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
			Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
			Replaced RGB PWM Block section with Embedded PWM IP section.
		DC and Switching Characteristics	Removed RGB PWM Block Timing section.
April 2014	01.0	All	Initial release.