Lattice Semiconductor Corporation - ICE5LP2K-UWG20ITR50 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	256
Number of Logic Elements/Cells	2048
Total RAM Bits	81920
Number of I/O	12
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (1.71x2.06)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp2k-uwg20itr50

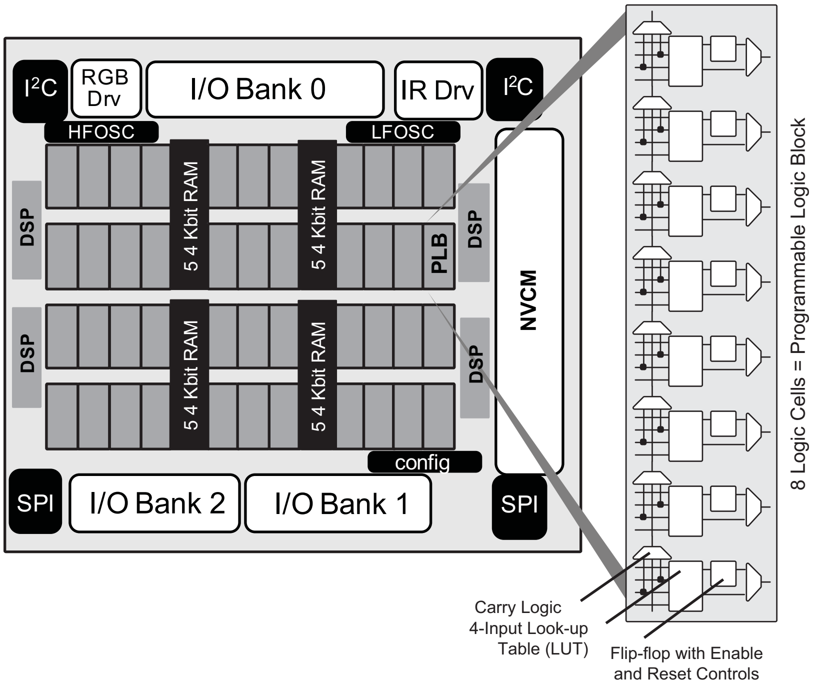
iCE40 Ultra Family Data Sheet
Architecture

June 2016 Data Sheet DS1048

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I^2C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

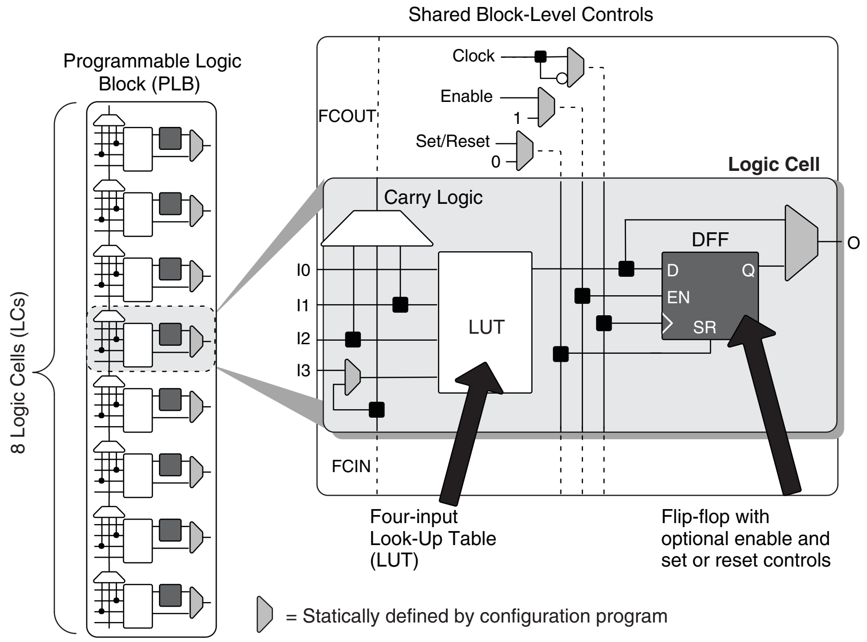
In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I^2C ports, two Oscillators, and high current RGB and IR LED sinks.

PLB Blocks

The core of the iCE40 Ultra device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

[1] If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 Ultra devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 Ultra global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 Ultra PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

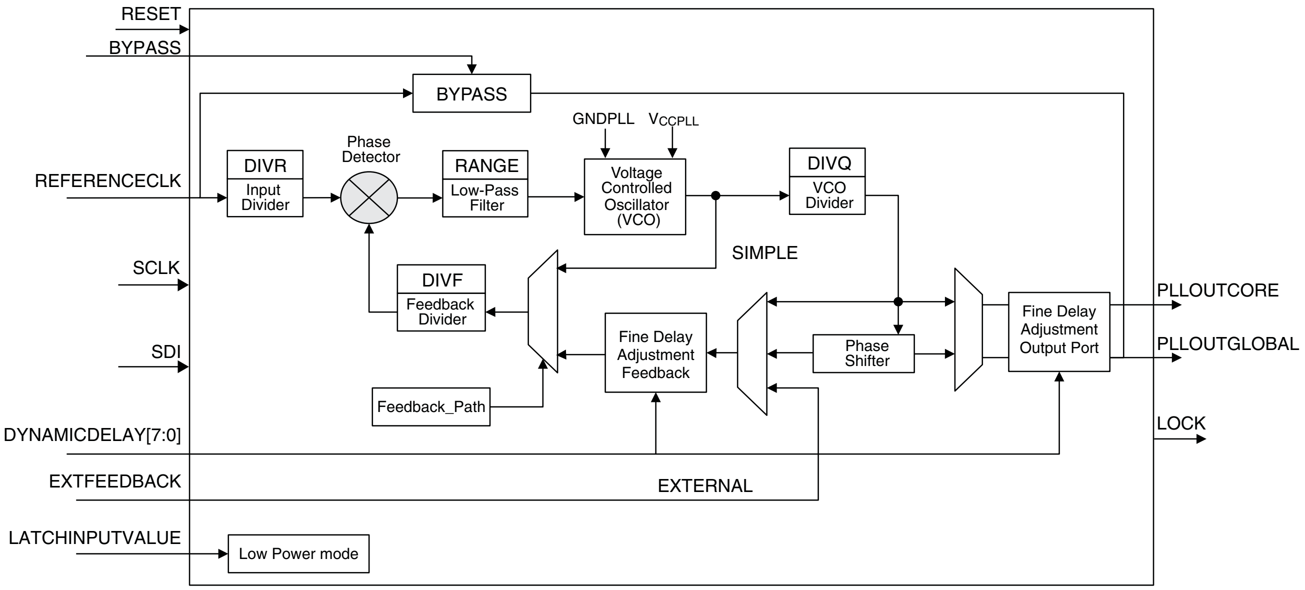


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 Ultra device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

***Table 2-4. sysMEM Block Configurations*[1]**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock, falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

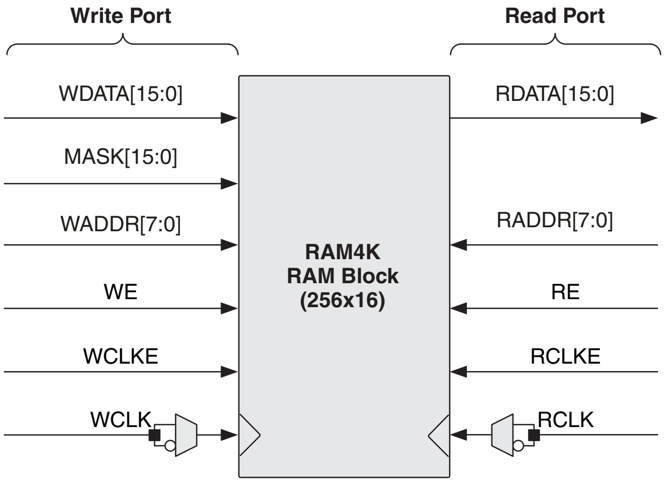


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

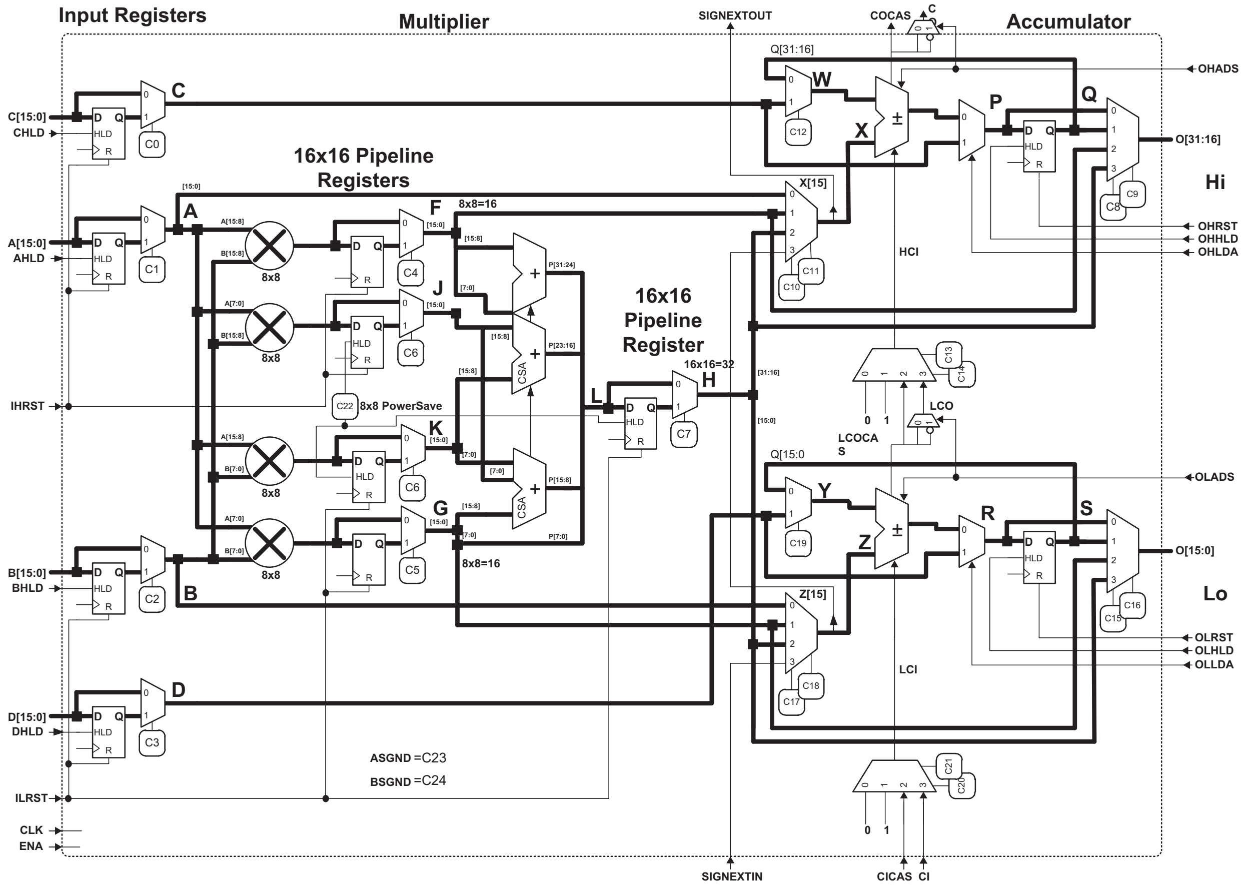
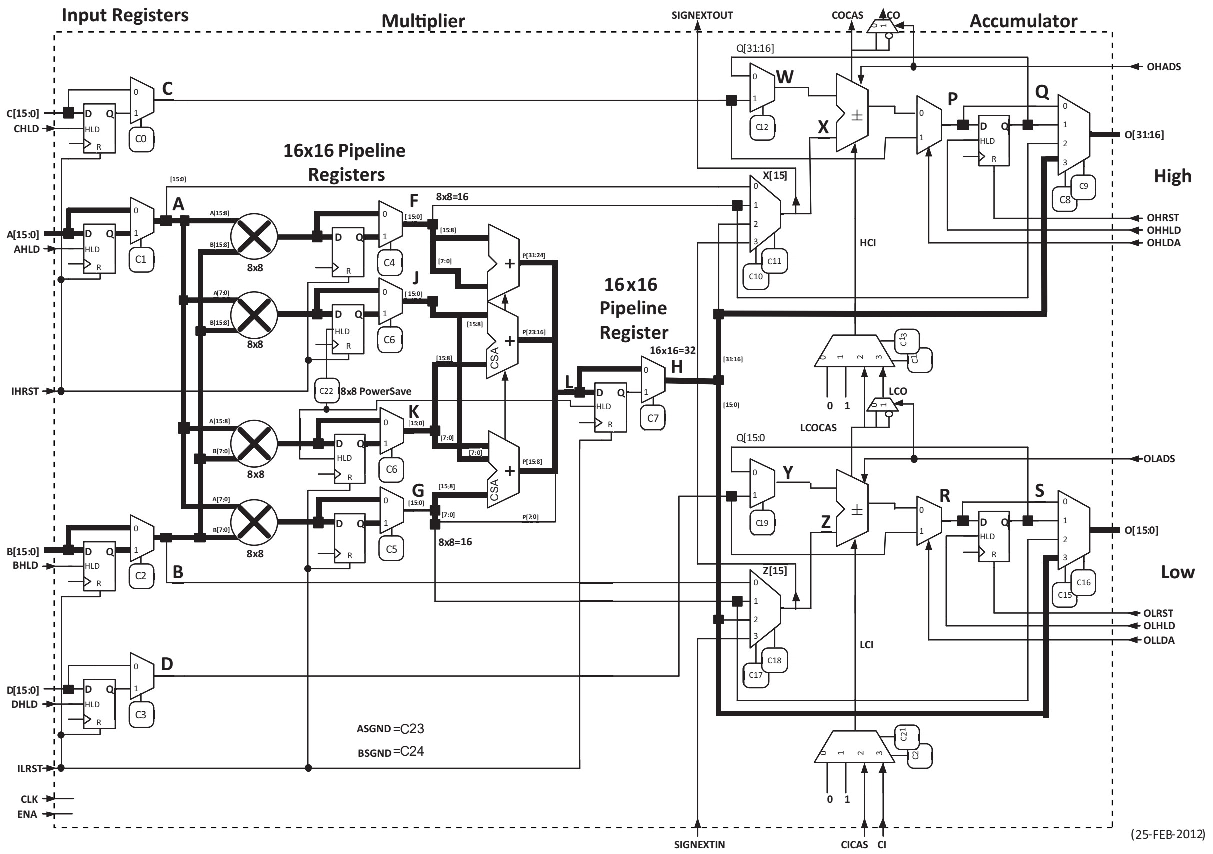


Figure 2-7. DSP 16-bit x 16-bit Multiplier



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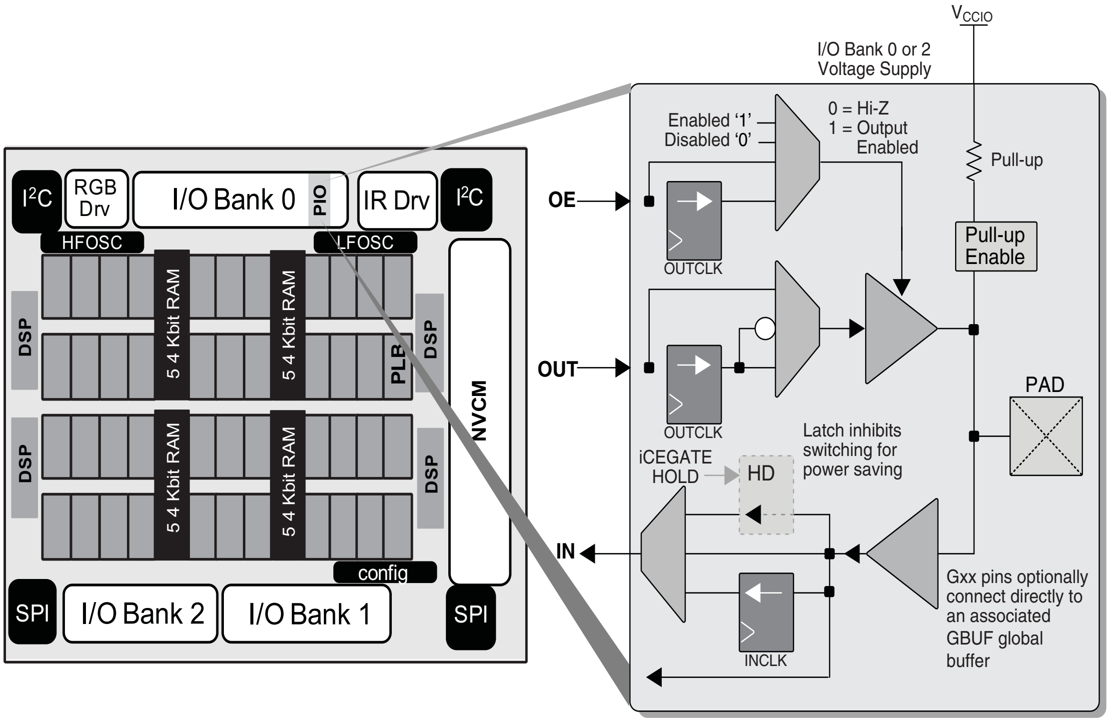
sysIO Buffer Banks

iCE40 Ultra devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-8. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-9 shows the input/output register block for the PIOs.

Figure 2-9. iCE I/O Register Block Diagram

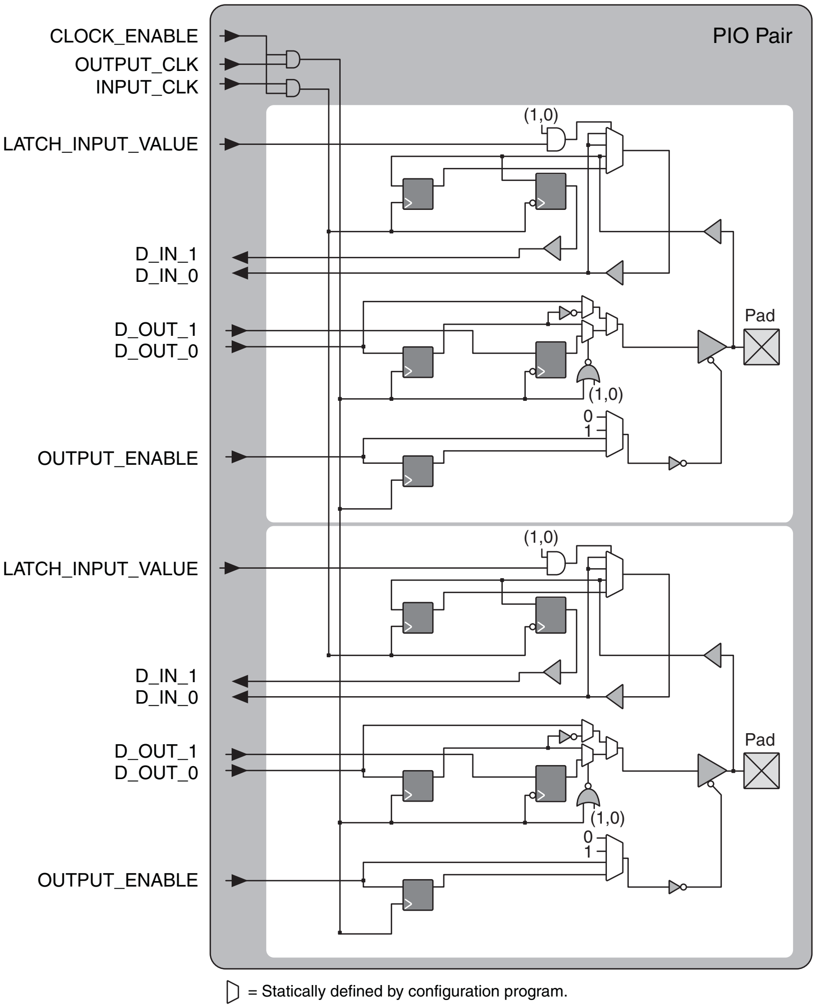


Table 2-7. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-8 and Table 2-9 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 Ultra devices.

Differential Comparators

The iCE40 Ultra devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-8. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-9. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

On-Chip Oscillator

The iCE40 Ultra devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

User I^{2}C IP

The iCE40 Ultra devices have two I^{2}C IP cores. Either of the two cores can be configured either as an I^{2}C master or as an I^{2}C slave. The pins for the I^{2}C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I^{2}C components.

When the IP core is configured as master, it will be able to control other devices on the I^{2}C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^{2}C Master. The I^{2}C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both

For further information on the User I^{2}C, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

User SPI IP

The iCE40 Ultra devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

High Current LED Drive I/O Pins

The iCE40 Ultra family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 Ultra product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, iCE40 LED Driver Usage Guide.

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration.

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, iCE40 Programming and Configuration.

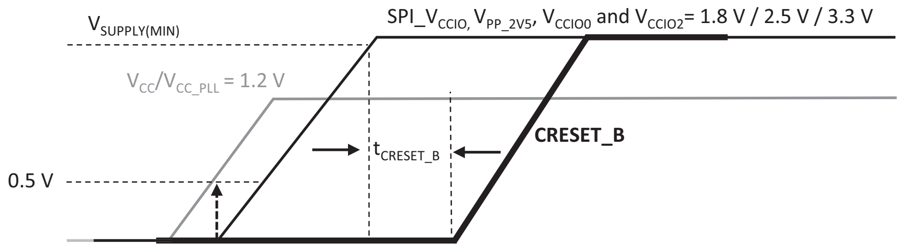
Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/–10	µA
C_1	I/O Capacitance, excluding LED Drivers[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_3	RGB Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	15	—	pF
C_4	IRLED Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	53	—	pF
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, $0 \le V_{IN} \le 0.65\ V_{CCIO}$	–3	—	–31	µA
		V_{CCIO} = 2.5 V, $0 \le V_{IN} \le 0.65\ V_{CCIO}$	–8	—	–72	µA
		V_{CCIO} = 3.3 V, $0 \le V_{IN} \le 0.65\ V_{CCIO}$	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Internal Oscillators (HFOSC, LFOSC)[1]

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	–20%	48	20%	MHz
f_{CLKLF}		LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC clock frequency (t_J = –45 °C–100 °C)	40	50	60	%
DCH_{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

1. Glitchless enabling and disabling OSC clock outputs.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{REF}	Reference Voltage to compare, on V_{INM}	V_{CCIO} = 2.5 V	0.25	V_{CCIO} –0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	—	–250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	V_{CCIO} = 2.5 V	–10	10	µA

iCE40 Ultra Family Timing Adders

Over Recommended Commercial Operating Conditions[1, 2, 3]

Buffer Type	Description	Timing (Typ.)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

iCE40 Ultra External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	Min	Max	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	410	ps
t_{CO}	Clock to Output – PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	5.9	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–0.6	—	ns

1. All the data is from the worst case condition.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

sysDSP Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time[4]		9.9	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

iCE40 Ultra Family Data Sheet
Pinout Information

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Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1 and 2.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations.
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V_{CCIO_1}.
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V_{CCIO1}.
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

iCE40 Ultra Family Data Sheet Revision History

June 2016 **Data Sheet DS1048**

Date	Version	Section	Change Summary
June 2016	2.0	Introduction	Updated General Description section. Changed “high current driver” to “high current IR driver”.
			Updated Features section. In Table 1-1, iCE40 Ultra Family Selection Guide, corrected HF Oscillator (48 kHz) to (48 MHz).
		Architecture	Updated Architecture Overview section. — Changed content to “The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks." — Changed “high current LED sink” to "high current RGB and IR LED sinks".
			Updated sysCLOCK Phase Locked Loops (PLLs) section. Corrected V_{CCPLL} character format in Figure 2-3, PLL Diagram.
			Updated sysMEM Embedded Block RAM Memory section. Updated footnote in Table 2-4, sysMEM Block Configurations.
			Updated sysIO Buffer Banks section. — Changed statement to “The configuration SPI interface signals are powered by SPI_V_{CCIO1}.” — Corrected V_{CCIO} character format in Figure 2-8, I/O Bank and Programmable I/O Cell.
			Updated Typical I/O Behavior During Power-up section. Modified text content.
			Updated Supported Standards section. Changed statement to “The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators.”
			Updated On-Chip Oscillator section. Changed statement to “The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option.”
			Updated section heading to High Current LED Drive I/O Pins. Changed “high current drive” to “high current LED drive”.
			Removed Power On Reset section.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. — Corrected symbol character format.
			Updated Recommended Operating Conditions section. — Corrected symbol character format. — Revised footnote 1. — Added footnote 4.
			Updated Power Supply Ramp Rates section. Changed t_{RAMP} Max. value.
			Added Power-On Reset section.
			Updated section heading to Power-Up Supply Sequencing. Revised text content.
			Added External Reset section.
			Updated DC Electrical Characteristics section. Revised footnote 4.