Lattice Semiconductor Corporation - ICE5LP4K-CM36ITR50 Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCFBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp4k-cm36itr50

iCE40 Ultra Family Data Sheet Introduction

June 2016 Data Sheet DS1048

General Description

iCE40 Ultra family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 Ultra family includes integrated SPI and I^2C blocks to interface with virtually all mobile sensors and application processors. The iCE40 Ultra family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 Ultra family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile sensors. The embedded RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 Ultra provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 500 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the modulation logic that meets his needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. This high current IR driver can also be used as Barcode Emulation, sending barcode information to external Barcode Reader.

The iCE40 Ultra family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 Ultra family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. It also has up to 80 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
  - Three devices with 1100 to 3520 LUTs
  - Offered in WLCS, ucfBGA and QFN packages
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - As low as 71 µA standby current typical
- **Embedded Memory**
  - Up to 80 kbits sysMEM™ Embedded Block RAM
- **Two Hardened I^2C Interfaces**
- **Two Hardened SPI Interfaces**
- **Two On-Chip Oscillators**
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- **500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 500 mA
- **On-chip DSP**
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - — Standard SPI Interface
    - — Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
  - As small as 2.078 mm x 2.078 mm
- **Applications**
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

Table 1-1. iCE40 Ultra Family Selection Guide

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
Logic Cells (LUT + Flip-Flop)	**1100**	**2048**	**3520**
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
Packages, ball pitch, dimension	**Total User I/O Count**		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39

Introduction

The iCE40 Ultra family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), on-chip Oscillators (LFOSC, HFOSC), two hardened I^2C Controllers, two hardened SPI Controllers, three 24 mA RGB LED open-drain drivers, a 500 mA IR LED open-drain drivers, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 Ultra FPGAs are available in very small form factor packages, as small as 2.078 mm x 2.078 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 Ultra devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 Ultra devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 Ultra family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 Ultra. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 Ultra device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

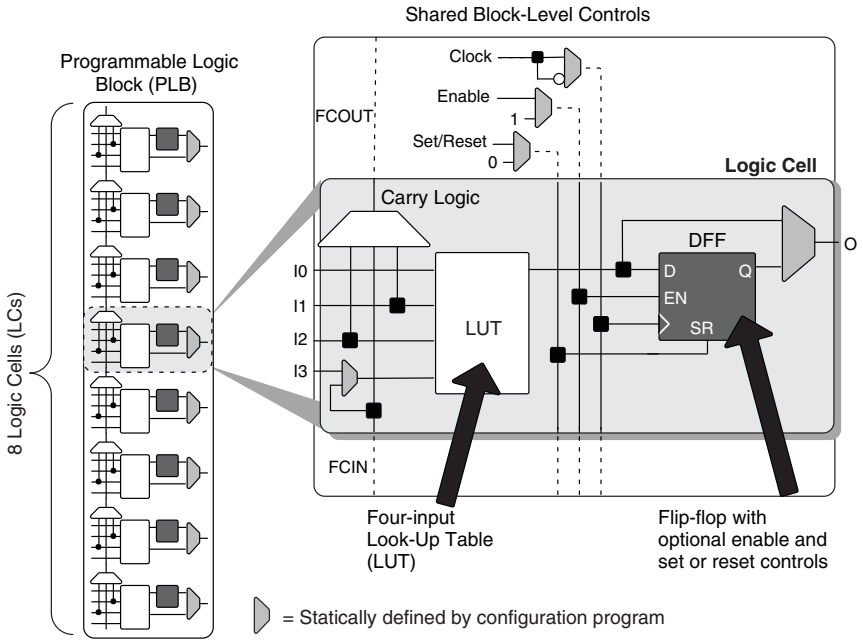
Lattice provides in the iCE40 Ultra 1K and 2K device the embedded RGB PWM IP at no extra cost of LUT available to the user, to perform controlling the RGB LED function. This embedded IP allow users to control color, LED ON/OFF time, and breathe rate of the LED. For more information, please refer to Usage Guide in Lattice Design Software.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 Ultra FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, please contact your local Lattice representative.

PLB Blocks

The core of the iCE40 Ultra device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Routing

There are many resources provided in the iCE40 Ultra devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 Ultra device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40 Ultra External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 Ultra device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 Ultra device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 Ultra devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 Ultra global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 Ultra PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

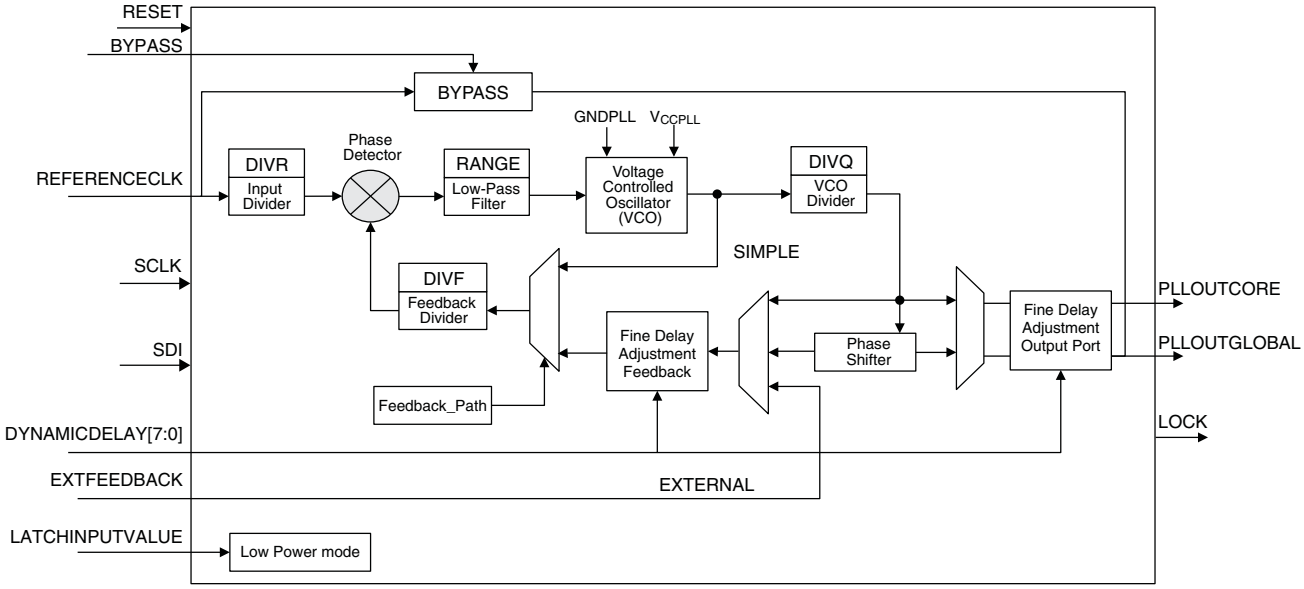


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 Ultra device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

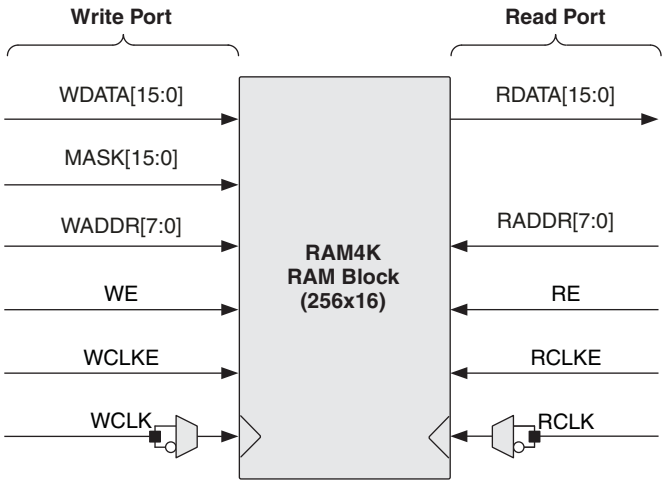


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

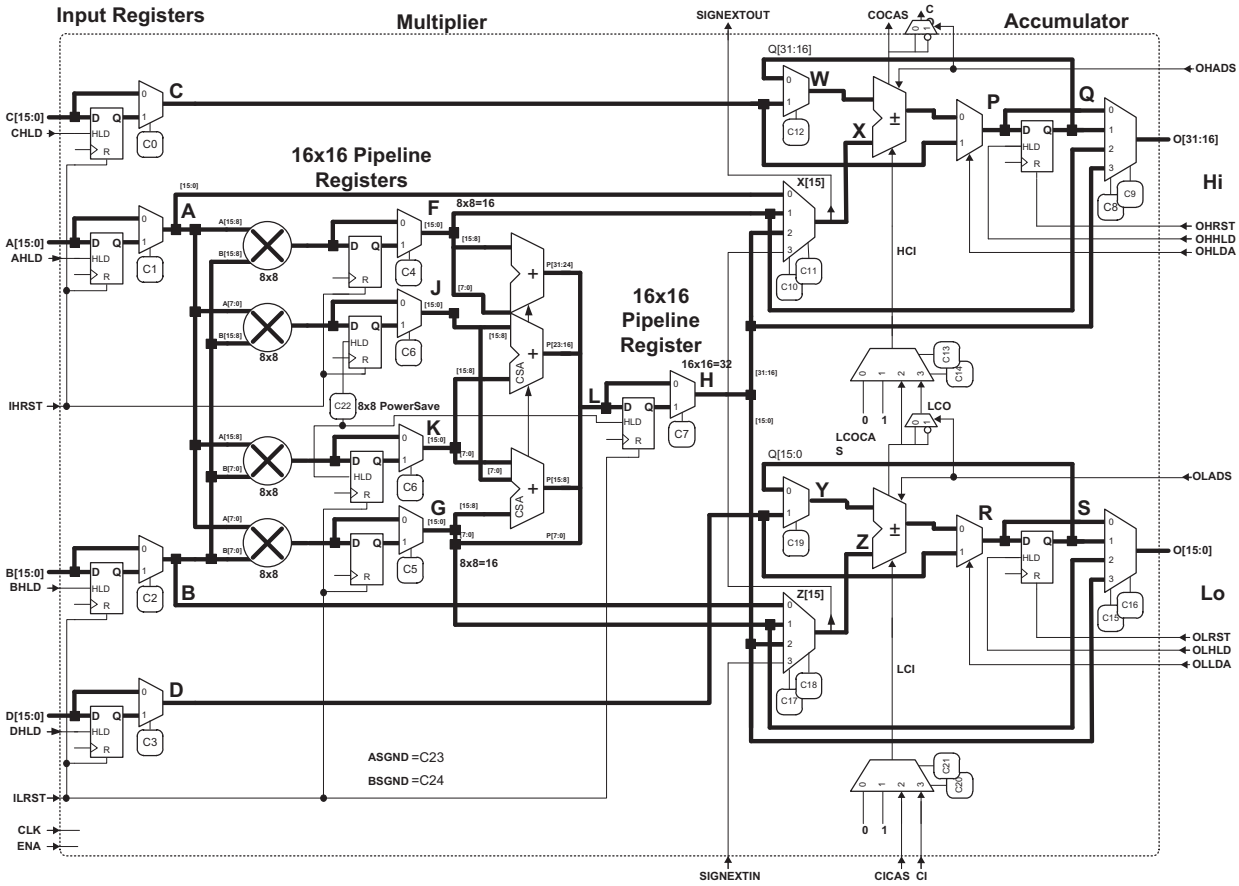
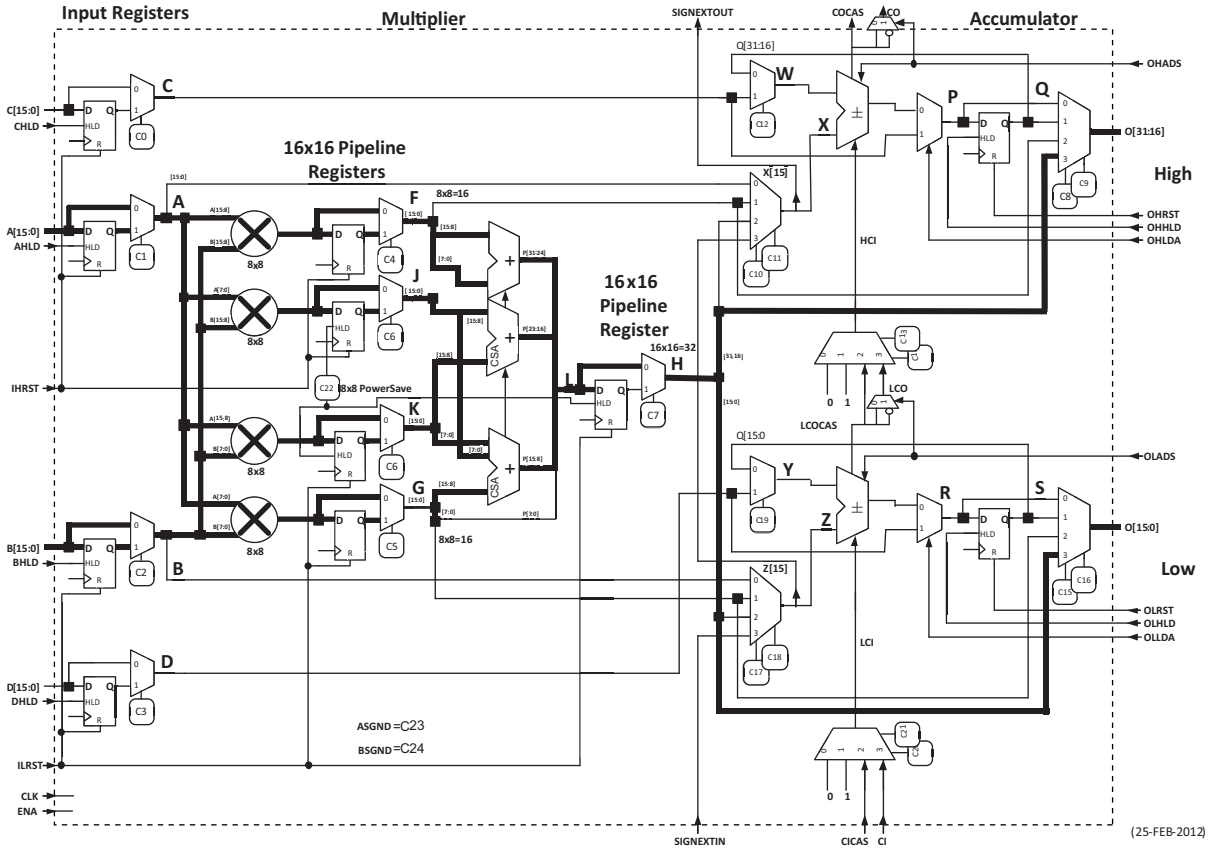


Figure 2-7. DSP 16-bit x 16-bit Multiplier



User I²C IP

The iCE40 Ultra devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both

For further information on the User I²C, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

User SPI IP

The iCE40 Ultra devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

High Current LED Drive I/O Pins

The iCE40 Ultra family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 Ultra product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

iCE40 Ultra Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.60 V

NVCM Supply Voltage V_{PP_2V5} . . . . . –0.5 V to 3.60 V

PLL Supply Voltage V_{CCPLL} . . . . . –0.5 V to 1.42 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . . –65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Power-On Reset

All iCE40 Ultra devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) V_{CC}, (2) SPI_V_{CCIO1} and (3) V_{PP_2V5}. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

Power-Up Supply Sequencing

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5V, or higher, before any subsequent power supplies in the sequence are applied.

1. **V_{CC}** and **V_{CCPLL}** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL} (Please refer to TN1252, iCE40 Hardware Checklist.)

2. **SPI_V_{CCIO1}** should be the next supply, and can be applied any time after the previous supplies (V_{CC} and V_{CCPLL}) have reached as level of 0.5 V or higher.

3. **V_{PP_2V5}** should be the next supply, and can be applied any time after previous supplies (V_{CC}, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.

4. **Other Supplies** (V_{CCIO0} and V_{CCIO2}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (V_{CC} and V_{CCPLL}) have reached a level of 0.5 V or greater.

There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are repowered up again.

External Reset

When all power supplies have reached to their minimum operating voltage defined in Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of t_{CRESET_B}, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory.

Figure 3-1 shows Power-Up sequence when SPI_V_{CCIO1} and V_{PP_2V5} are connected separately, and the CRESET_B signal triggers configuration download. Figure 3-2 shows when SPI_V_{CCIO1} and V_{PP_2V5} connected together.

All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

Figure 3-1. Power Up Sequence with SPI_V_{CCIO1} and V_{PP_2V5} Not Connected Together

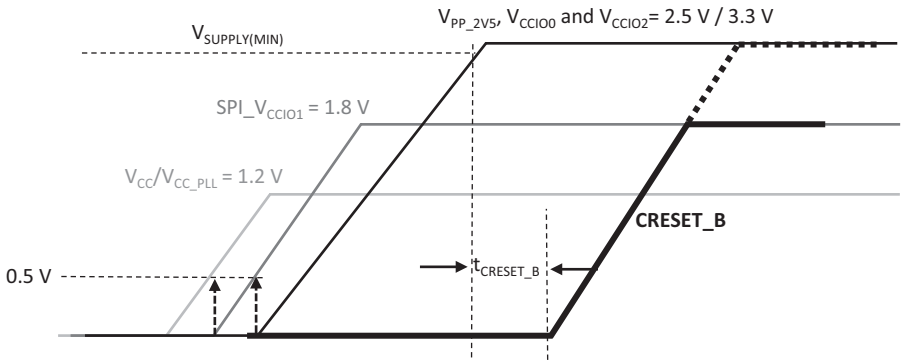
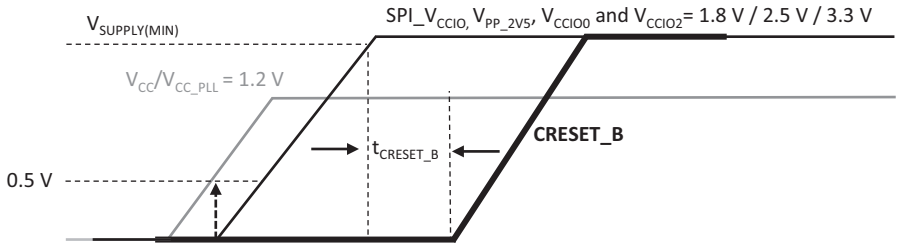


Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	0V < V_{IN} < V_{CCIO} + 0.2 V	—	—	+/–10	µA
C_1	I/O Capacitance, excluding LED Drivers[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pF
C_3	RGB Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	15	—	pF
C_4	IRLED Pin Capacitance[2]	V_{CC} = Typ., V_{IO} = 0 to 3.5 V	—	53	—	pF
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time[4]		9.9	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1 and 2.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations.
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V_{CCIO_1}.
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V_{CCIO1}.
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Signal Name		Function	I/O	Description
PIOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer
PIOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer
PIOT_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer
PIOT_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer
PIOT_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED

Pin Information Summary

Pin Type		iCE5LP1K			iCE5LP2K			iCE5LP4K		
		CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]
General Purpose I/O Per Bank	Bank 0	12	5	17	12	5	17	12	5	17
	Bank 1	4	15	14	4	15	14	4	15	14
	Bank 2	10	6	8	10	6	8	10	6	8
Total General Purpose I/Os		26	26	39	26	26	39	26	26	39
V_{CC}		1	1	2	1	1	2	1	1	2
V_{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V_{CCPLL}		1	1	1	1	1	1	1	1	1
V_{PP_2V5}		1	1	1	1	1	1	1	1	1
Dedicated Config Pins		1	1	2	1	1	2	1	1	2
GND		2	2	0	2	2	0	2	2	0
GND_LED		1	1	0	1	1	0	1	1	0
Total Balls		36	36	48	36	36	48	36	36	48

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM36ITR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG36ITR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG48ITR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG48ITR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM36ITR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG36ITR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG48ITR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG48ITR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM36ITR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG36ITR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG48ITR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG48ITR50	3520	1.2 V	Halogen-Free QFN	48	IND

iCE40 Ultra Family Data Sheet Revision History

June 2016 **Data Sheet DS1048**

Date	Version	Section	Change Summary
June 2016	2.0	Introduction	Updated General Description section. Changed “high current driver” to “high current IR driver”.
			Updated Features section. In Table 1-1, iCE40 Ultra Family Selection Guide, corrected HF Oscillator (48 kHz) to (48 MHz).
		Architecture	Updated Architecture Overview section. — Changed content to “The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks." — Changed “high current LED sink” to "high current RGB and IR LED sinks".
			Updated sysCLOCK Phase Locked Loops (PLLs) section. Corrected V_{CCPLL} character format in Figure 2-3, PLL Diagram.
			Updated sysMEM Embedded Block RAM Memory section. Updated footnote in Table 2-4, sysMEM Block Configurations.
			Updated sysIO Buffer Banks section. — Changed statement to “The configuration SPI interface signals are powered by SPI_V_{CCIO1}.” — Corrected V_{CCIO} character format in Figure 2-8, I/O Bank and Programmable I/O Cell.
			Updated Typical I/O Behavior During Power-up section. Modified text content.
			Updated Supported Standards section. Changed statement to “The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators.”
			Updated On-Chip Oscillator section. Changed statement to “The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option.”
			Updated section heading to High Current LED Drive I/O Pins. Changed “high current drive” to “high current LED drive”.
			Removed Power On Reset section.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. — Corrected symbol character format.
			Updated Recommended Operating Conditions section. — Corrected symbol character format. — Revised footnote 1. — Added footnote 4.
			Updated Power Supply Ramp Rates section. Changed t_{RAMP} Max. value.
			Added Power-On Reset section.
			Updated section heading to Power-Up Supply Sequencing. Revised text content.
			Added External Reset section.
			Updated DC Electrical Characteristics section. Revised footnote 4.

Date	Version	Section	Change Summary
			Updated Supply Current section. — Corrected $I_{PP2V5STDBY}$ parameter. — Added Typ. VCC = 1.2 V values for I_{CCPEAK}, $I_{PP\_2V5PEAK}$, $I_{SPI\_VCCIO1PEAK}$, and $I_{CCIOPEAK}$. — Added footnote 5. — Corrected S_{PI_VCCIO1} character format.
			Updated User SPI Specifications section. Removed parameters and added footnotes.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for DCH_{CLKHF}.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Removed footnote.
			Updated Register-to-Register Performance section. Modified footnotes.
			Updated iCE40 Ultra External Switching Characteristics section. Modified footnote.
			Updated sysCLOCK PLL Timing section. Reversed t_{OPJIT} conditions.
			Updated sysCONFIG Port Timing Specifications section. — Modified t_{CR_SCK} Min. value. — Added footnote 4 to t_{SU} parameter. — Modified t_{SU} Min. value. — Modified t_{HD} parameter.
			Updated section heading to RGB LED and IR LED Drive. Modified ILED_ACCURACY and IIR_ACCURACY parameters, Min. and Max. values.
		Pinout Information	Updated Signal Descriptions section. Changed V_{CCIO_1} to SPI_V_{CCIO1} in the CDONE, CRESETB and PIOB_xx descriptions.
			Updated Pin Information Summary section. — Corrected symbol character format. — Corrected VCPP_2V5 to V_{PP_2V5}.
	1.9	Introduction	Updated Features section. Updated BGA package to ucfBGA.
		DC and Switching Characteristics	Updated Differential Comparator Electrical Characteristics section. Corrected typo in V_{REF} Max. value.
		Pinout Information	Updated Signal Descriptions section. — Changed PIOB_12a to PIOB_xx — Changed SPI_CSN to SPI_SS_B and revised description when in Slave SPI mode. — Corrected minor typo errors.
			Updated Pin Information Summary section. Added footnote to SG48.
		Ordering Information	Updated iCE5LP Part Number Description section. Updated BGA package to ucfBGA.
			Updated Ordering Part Numbers section. Updated BGA package to ucfBGA.
June 2015	1.8	DC and Switching Characteristics	Updated Internal Oscillators (HFOSC, LFOSC) section. Removed decimals.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added TR items. — Corrected formatting errors.
			Updated Ordering Part Numbers section. Updated CM36 and SG48 packages.