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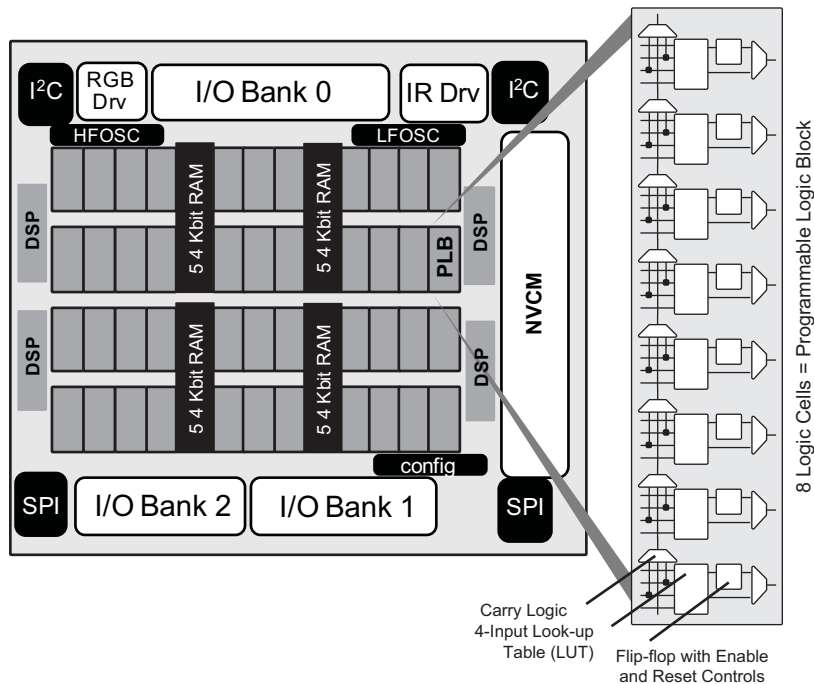
Details

Product Status	Active
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	39
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp4k-sg48itr

Architecture Overview

The iCE40 Ultra family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE5LP-4K device.

Figure 2-1. iCE5LP-4K Device, Top View



The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 Ultra family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document on Power Up Sequence. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40 Ultra also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks.

Routing

There are many resources provided in the iCE40 Ultra devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 Ultra device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40 Ultra External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 Ultra device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 Ultra device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

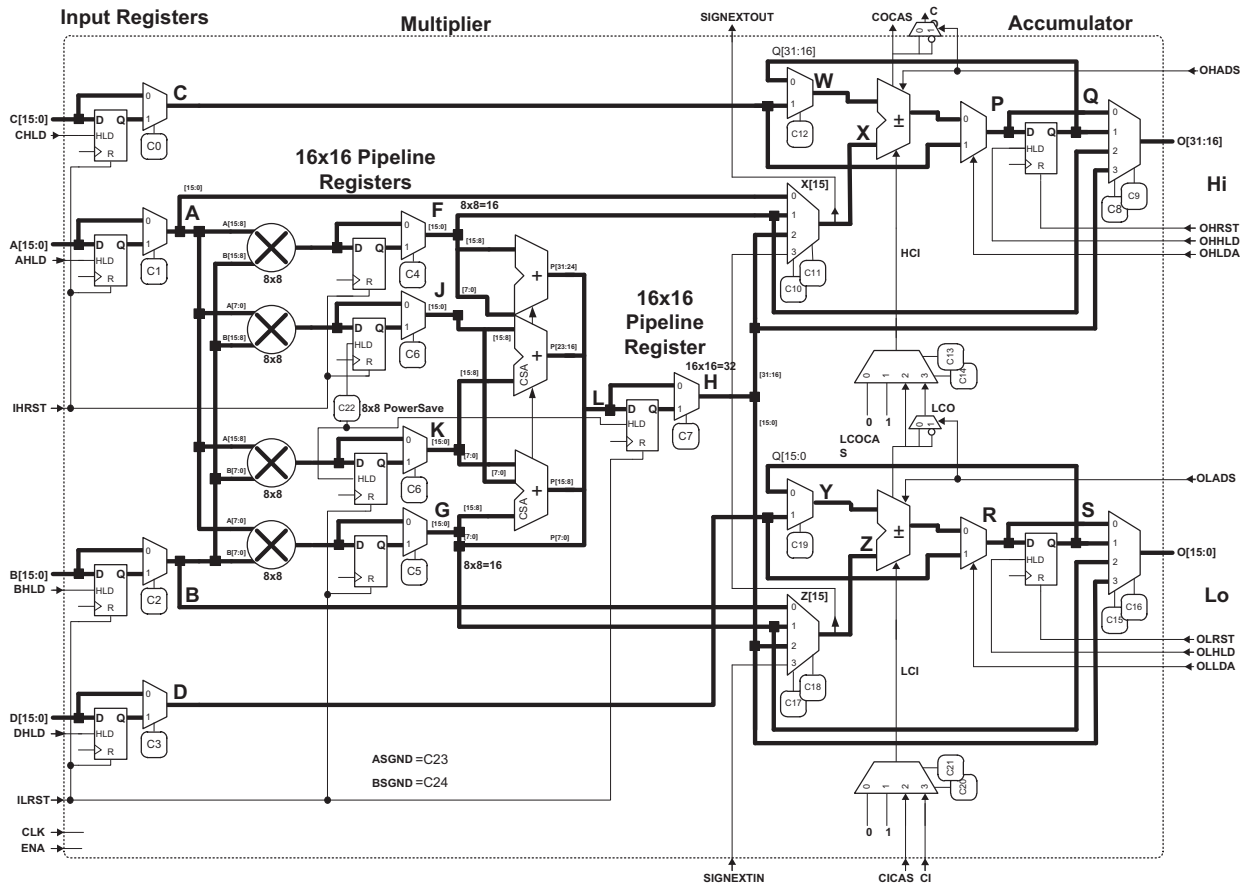
iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtractor functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)



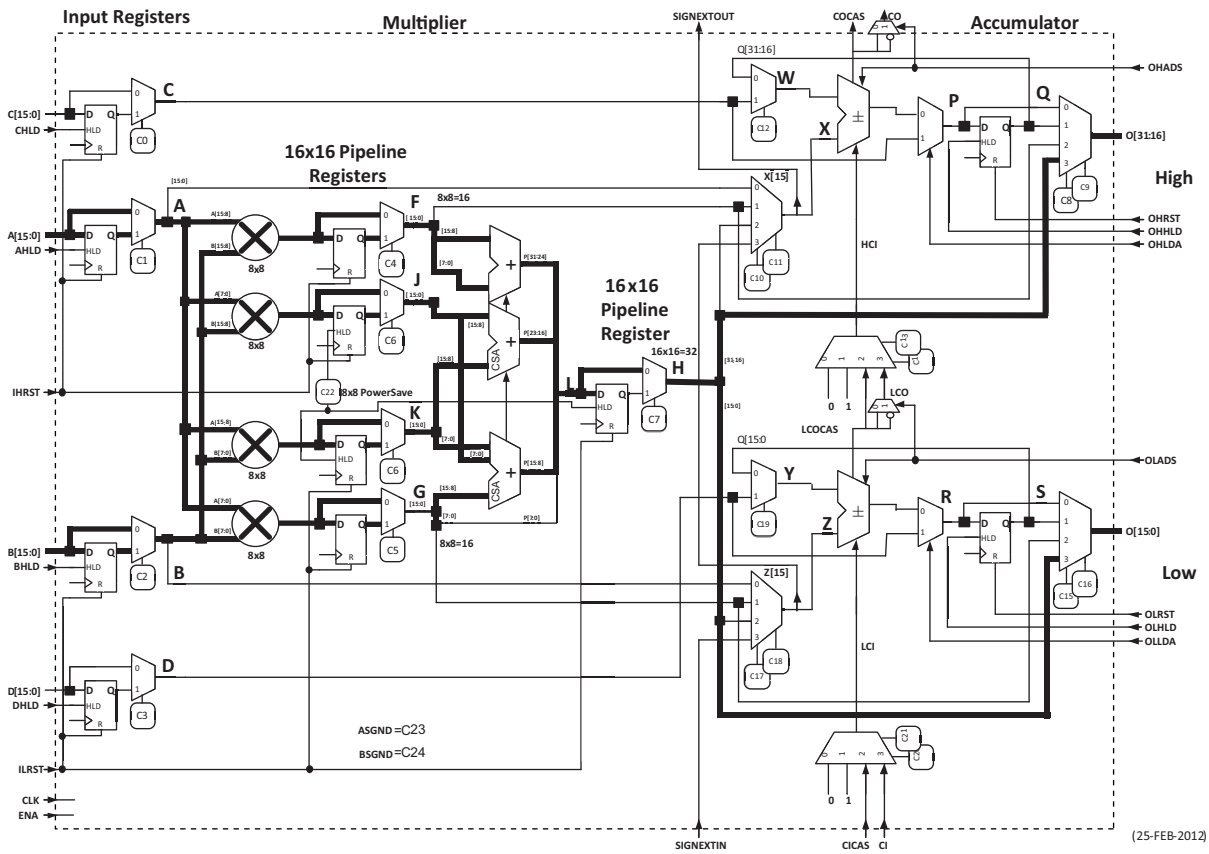
Signal	Primitive Port Name	Width	Input / Output	Function	Default
OHLDA	OLOADTOP	1	Input	High-order (upper half) Accumulator Register Accumulate/Load control. 0 = Accumulate, register is loaded with Adder/Subtractor results 1 = Load, register is loaded with Input C or C Register	0: Accumulate
OHADS	ADDSUBTOP	1	Input	High-order (upper half) Accumulator Add or Subtract select. 0 = Add 1 = Subtract	0: Add
OLHLD	OHOLDBOT	1	Input	Low-order (lower half) Accumulator Register Hold. 0 = Update 1 = Hold	0: Update
OLRST	ORSTBOT	1	Input	Reset input to Low-order (lower half) bits of the Accumulator Register. 0 = No Reset 1 = Reset	0: No Reset
OLLDA	OLOADBOT	1	Input	Low-order (lower half) Accumulator Register Accumulate/Load control. 0 = Accumulate, register is loaded with Adder/Subtractor results 1 = Load, register is loaded with Input C or C Register	0: Accumulate
OLADS	ADDSUBBOT	1	Input	Low-order (lower half) Accumulator Add or Subtract select. 0 = Add 1 = Subtract	0: Add
CICAS	ACCUMCI	1	Input	Cascade Carry/Borrow input from previous sysDSP block	
CI	CI	1	Input	Carry/Borrow input from lower logic tile	
COCAS	ACCUMCO	1	Output	Cascade Carry/Borrow output to next sysDSP block	
CO	CO	1	Output	Carry/Borrow output to higher logic tile	
SIGNEXTIN	SIGNEXTIN	1	Input	Sign extension input from previous sysDSP block	
SIGNEXTOUT	SIGNEXTOUT	1	Output	Sign extension output to next sysDSP block	

The iCE40 Ultra sysDSP can support the following functions:

- 8-bit x 8-bit Multiplier
- 16-bit x 16-bit Multiplier
- 16-bit Adder/Subtractor
- 32-bit Adder/Subtractor
- 16-bit Accumulator
- 32-bit Accumulator
- 8-bit x 8-bit Multiply-Accumulate
- 16-bit x 16-bit Multiply-Accumulate

Figure 2-6 shows the path for an 8-bit x 8-bit Multiplier using the upper half of sysDSP block.

Figure 2-7. DSP 16-bit x 16-bit Multiplier



Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , SPI_V_{CCIO1} , and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the [DC and Switching Characteristics](#) section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO} . The I/O pins maintain the pre-configuration state until V_{CC} , SPI_V_{CCIO1} , and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-8 and Table 2-9 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 Ultra devices.

Differential Comparators

The iCE40 Ultra devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the [Pin Information Summary](#) section to locate the corresponding paired I/Os with differential comparators.

Table 2-8. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-9. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

On-Chip Oscillator

The iCE40 Ultra devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

User I²C IP

The iCE40 Ultra devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both

For further information on the User I²C, please refer to TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#).

User SPI IP

The iCE40 Ultra devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#).

High Current LED Drive I/O Pins

The iCE40 Ultra family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 Ultra product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RGB LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, [iCE40 LED Driver Usage Guide](#).

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration](#).

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, [iCE40 Programming and Configuration](#).

Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	-0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	-0.5 V to 1.42 V
I/O Tri-state Voltage Applied	-0.5 V to 3.60 V
Dedicated Input Voltage Applied	-0.5 V to 3.60 V
Storage Temperature (Ambient)	-65 °C to 150 °C
Junction Temperature (T_J)	-65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units	
V_{CC}^1	Core Supply Voltage	1.14	1.26	V	
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71 ⁴	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
$V_{CCIO}^{1,2,3}$	I/O Driver Supply Voltage	$V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}$	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V	
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C	
t_{JIND}	Junction Temperature Industrial Operation	-40	100	°C	
t_{PROG}	Junction Temperature NVCM Programming	10.00	30.00	°C	

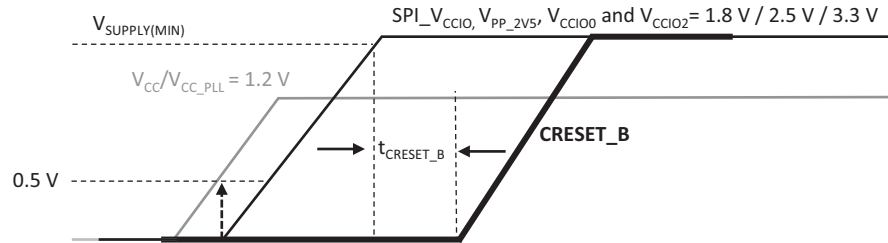
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to [Power-Up Supply Sequencing](#) section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates^{1, 2}

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to [Power-Up Supply Sequencing](#) section.

Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels¹

Symbol	Parameter	Min.	Max.	Units	
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC} , SPI_V_{CCI01} , V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCI01}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC} , SPI_V_{CCI01} , V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCI01}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH} ^{1,3,4}	Input or I/O Leakage	$0V < V_{IN} < V_{CCI0} + 0.2 V$	—	—	+/-10	μA
C_1	I/O Capacitance, excluding LED Drivers ²	$V_{CCI0} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCI0} + 0.2 V$	—	6	—	pF
C_2	Global Input Buffer Capacitance ²	$V_{CCI0} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCI0} + 0.2 V$	—	6	—	pF
C_3	RGB Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	15	—	pF
C_4	IRLED Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	53	—	pF
V_{HYST}	Input Hysteresis	$V_{CCI0} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	$V_{CCI0} = 1.8 V, 0 \leq V_{IN} \leq 0.65 V_{CCI0}$	-3	—	-31	μA
		$V_{CCI0} = 2.5 V, 0 \leq V_{IN} \leq 0.65 V_{CCI0}$	-8	—	-72	μA
		$V_{CCI0} = 3.3 V, 0 \leq V_{IN} \leq 0.65 V_{CCI0}$	-11	—	-128	μA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.

2. T_J 25 °C, $f = 1.0$ MHz.

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

4. Input pins are clamped to V_{CCI0} and GND by a diode. When input is higher than V_{CCI0} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH} .

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1,5,6}$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	450	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \geq 100$ MHz	—	750	ps p-p
		$f_{OUT} < 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 25$ MHz	—	275	ps p-p
		$f_{PFD} < 25$ MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	μ s
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}^4	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{STABLE}^3	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE_PW}^3$	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	μ s
$t_{DYNAMIC_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD} . As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

sysDSP Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

SPI Master or NVCM Configuration Time^{1, 2}

Symbol	Parameter	Conditions	Max.	Units
t _{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t _{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t _{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t _{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	μs
f _{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read ¹	—	15	—	MHz
t _{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t _{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t _{STSU}	CCLK setup time		12	—	—	ns
t _{STH}	CCLK hold time		12	—	—	ns
t _{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI³						
f _{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency ²	21.0	33.0	45.0	MHz
		High Frequency ²	33.0	53.0	71.0	MHz
t _{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	μs
t _{SU}	CCLK setup time ⁴		9.9	—	—	ns
t _{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, [iCE40 Programming and Configuration](#).

Signal Descriptions

Signal Name	Function	I/O	Description	
Power Supplies				
V _{CC}	Power	—	Core Power Supply	
V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}	Power	—	Power for I/Os in Bank 0, 1 and 2.	
V _{PP_2V5}	Power	—	Power for NVCM programming and operations.	
V _{CCPLL}	Power	—	Power for PLL	
GND	GROUND	—	Ground	
GND_LED	GROUND	—	Ground for LED drivers. Should connect to GND on board.	
Configuration				
CRESETB	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V _{CCIO_1} .	
CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V _{CCIO1} .	
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.	
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V _{CCIO1} .
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V _{CCIO1} .
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Signal Name		Function	I/O	Description
PIOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer
PIOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer
PIOT_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer
PIOT_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer
PIOT_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED

Signal Name	Function	I/O	Description
RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 500mA output to drive external LED
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location)
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location)

Pin Information Summary

Pin Type		iCE5LP1K			iCE5LP2K			iCE5LP4K		
		CM36	SWG36	SG48 ¹	CM36	SWG36	SG48 ¹	CM36	SWG36	SG48 ¹
General Purpose I/O Per Bank	Bank 0	12	5	17	12	5	17	12	5	17
	Bank 1	4	15	14	4	15	14	4	15	14
	Bank 2	10	6	8	10	6	8	10	6	8
Total General Purpose I/Os		26	26	39	26	26	39	26	26	39
V _{CC}		1	1	2	1	1	2	1	1	2
V _{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V _{CCPLL}		1	1	1	1	1	1	1	1	1
V _{PP_2V5}		1	1	1	1	1	1	1	1	1
Dedicated Config Pins		1	1	2	1	1	2	1	1	2
GND		2	2	0	2	2	0	2	2	0
GND_LED		1	1	0	1	1	0	1	1	0
Total Balls		36	36	48	36	36	48	36	36	48

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

For Further Information

A variety of technical notes for the iCE40 Ultra family are available on the Lattice web site.

- [TN1248, iCE40 Programming and Configuration](#)
- [TN1274, iCE40 SPI/I2C Hardened IP Usage Guide](#)
- [TN1276, Advanced iCE40 SPI/I2C Hardened IP Usage Guide](#)
- [TN1250, Memory Usage Guide for iCE40 Devices](#)
- [TN1251, iCE40 sysCLOCK PLL Design and Usage Guide](#)
- [TN1252, iCE40 Hardware Checklist](#)
- [TN1288, iCE40 LED Driver Usage Guide](#)
- [TN1295, DSP Function Usage Guide for iCE40 Devices](#)
- [TN1296, iCE40 Oscillator Usage Guide](#)
- [iCE40 Ultra Pinout Files](#)
- [iCE40 Ultra Pin Migration Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)
- [Schematic Symbols](#)

Date	Version	Section	Change Summary
			<p>Updated Supply Current section.</p> <ul style="list-style-type: none"> — Corrected $I_{PP2V5STDBY}$ parameter. — Added Typ. $V_{CC} = 1.2\text{ V}$ values for I_{CCPEAK}, $I_{PP_2V5PEAK}$, $I_{SPI_VCCIO1PEAK}$, and $I_{CCIOPEAK}$. — Added footnote 5. — Corrected S_{PI_VCCIO1} character format.
			Updated User SPI Specifications section. Removed parameters and added footnotes.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for DCH_{CLKHF} .
			Updated sysIO Single-Ended DC Electrical Characteristics section. Removed footnote.
			Updated Register-to-Register Performance section. Modified footnotes.
			Updated iCE40 Ultra External Switching Characteristics section. Modified footnote.
			Updated sysCLOCK PLL Timing section. Reversed t_{OPJIT} conditions.
			<p>Updated sysCONFIG Port Timing Specifications section.</p> <ul style="list-style-type: none"> — Modified t_{CR_SCK} Min. value. — Added footnote 4 to t_{SU} parameter. — Modified t_{SU} Min. value. — Modified t_{HD} parameter.
			Updated section heading to RGB LED and IR LED Drive . Modified $I_{LED_ACCURACY}$ and $I_{IR_ACCURACY}$ parameters, Min. and Max. values.
		Pinout Information	<p>Updated Signal Descriptions section. Changed V_{CCIO_1} to S_{PI_VCCIO1} in the CDONE, CRESETB and PIOB_xx descriptions.</p> <p>Updated Pin Information Summary section.</p> <ul style="list-style-type: none"> — Corrected symbol character format. — Corrected V_{CPP_2V5} to V_{PP_2V5}.
	1.9	Introduction	Updated Features section. Updated BGA package to ucfBGA.
		DC and Switching Characteristics	Updated Differential Comparator Electrical Characteristics section. Corrected typo in V_{REF} Max. value.
		Pinout Information	<p>Updated Signal Descriptions section.</p> <ul style="list-style-type: none"> — Changed PIOB_12a to PIOB_xx — Changed SPI_CSN to SPI_SS_B and revised description when in Slave SPI mode. — Corrected minor typo errors. <p>Updated Pin Information Summary section. Added footnote to SG48.</p>
		Ordering Information	Updated iCE5LP Part Number Description section. Updated BGA package to ucfBGA.
			Updated Ordering Part Numbers section. Updated BGA package to ucfBGA.
June 2015	1.8	DC and Switching Characteristics	Updated Internal Oscillators (HFOSC, LFOSC) section. Removed decimals.
		Ordering Information	<p>Updated iCE5LP Part Number Description section.</p> <ul style="list-style-type: none"> — Added TR items. — Corrected formatting errors. <p>Updated Ordering Part Numbers section. Updated CM36 and SG48 packages.</p>

Date	Version	Section	Change Summary
April 2015	1.7	Architecture	Updated sysDSP section. Revised the following figures: — Figure 2-5, sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate) — Figure 2-6, sysDSP 8-bit x 8-bit Multiplier — Figure 2-7, DSP 16-bit x 16-bit Multiplier
		Ordering Information	Updated iCE5LP Part Number Description section. Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
March 2015	1.6	Introduction	Updated Features section. — Added BGA and QFN packages in Flexible Logic Architecture. — Added USB 3.1 Type C Cable Detect / Power Delivery Applications in Applications. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added 36-ball ucFBGA and 48-ball QFN packages. Changed subheading to Total User I/O Count. Changed RBW IP to PWM IP. Deleted footnotes.
		DC and Switching Characteristics	Updated Power-up Sequence section. Indicated all devices in second paragraph.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2.5 V _{OH} Min. (V) from 0.5 to 0.4.
			Replaced the Differential Comparator Electrical Characteristics table.
		Pinout Information	Updated Pin Information Summary section. — Added CM36 and SG48 values. — Changed CRESET_B to Dedicated Config Pins.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added CM36 and SG48 package. — Added TR items.
Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.			
October 2014	1.5	Introduction	Updated Features section. — Removed 26 I/O pins for 36-pin WLCSP under Flexible Logic Architecture. — Changed form factor to 2.078 mm x 2.078 mm. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 20-Ball WLCSP.
			Updated Introduction section. Changed form factor to 2.078 mm x 2.078 mm.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) section. Removed note in heading regarding sysCLOCK PLL support.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Removed footnote on sysCLOCK PLL support.
			Updated Power-up Sequence section. Removed information on 20-pin WLCSP.
		Pinout Information	Updated Signal Descriptions section. Removed references 20-pin WLCSP.
			Updated Pin Information Summary section. Removed references to UWG20 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 20-ball WLCSP.
			Updated Ordering Part Numbers section. Removed UWG20 part numbers.
		Further Information	Added technical note references.

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.			
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
		Replaced RGB PWM Block section with Embedded PWM IP section.	
DC and Switching Characteristics	Removed RGB PWM Block Timing section.		
April 2014	01.0	All	Initial release.