Lattice Semiconductor Corporation - ICE5LP4K-SWG36ITR Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

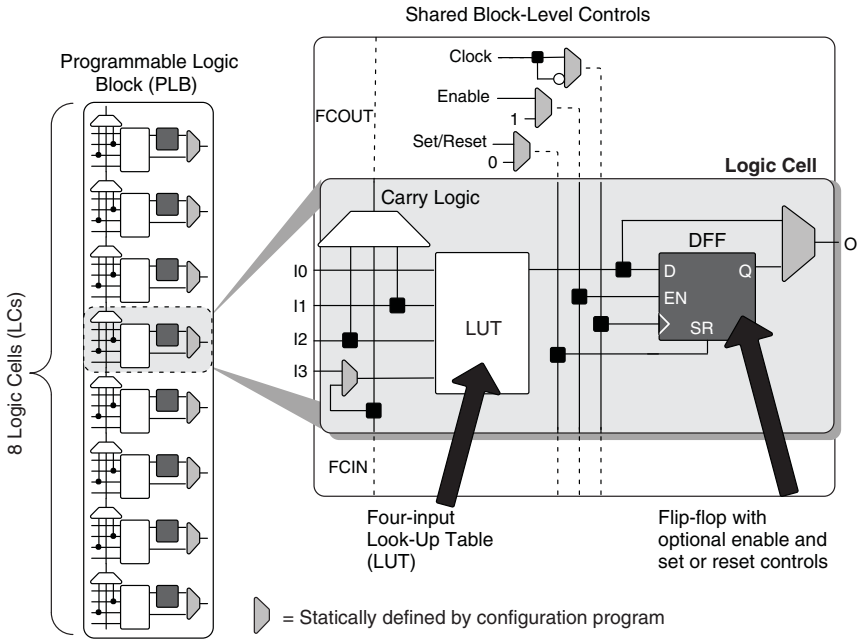
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-XFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.1x2.1)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice5lp4k-swg36itr

PLB Blocks

The core of the iCE40 Ultra device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 Ultra devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 Ultra global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 Ultra PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

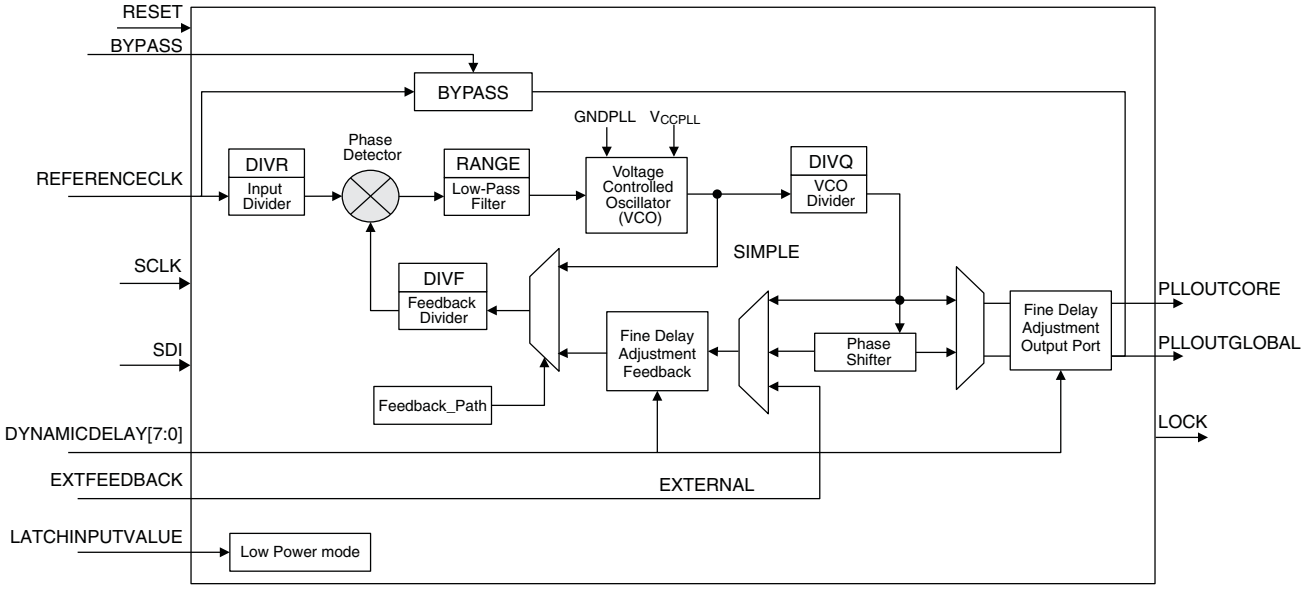


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 Ultra device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

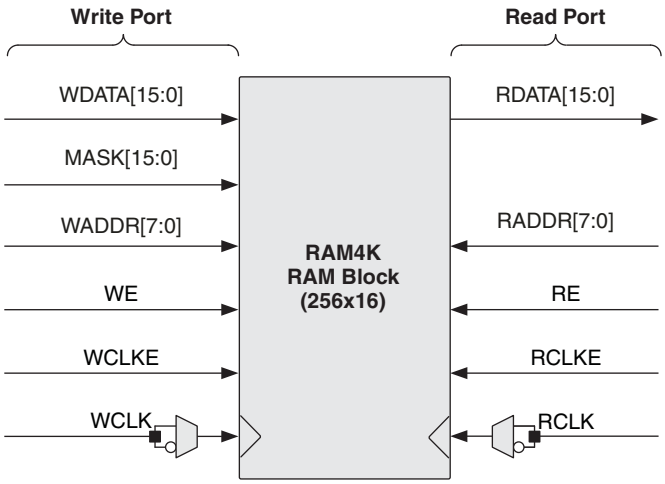


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

sysDSP

The iCE40 Ultra family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 Ultra sysDSP Architecture Features

The iCE40 Ultra sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 2-5 shows the block diagram of the sysDSP block. The block consists Multiplier section, with an bypassable Output register. The Input Register, Intermediate register between Multiplier and AC timing to achieve the highest performance.

Figure 2-5. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

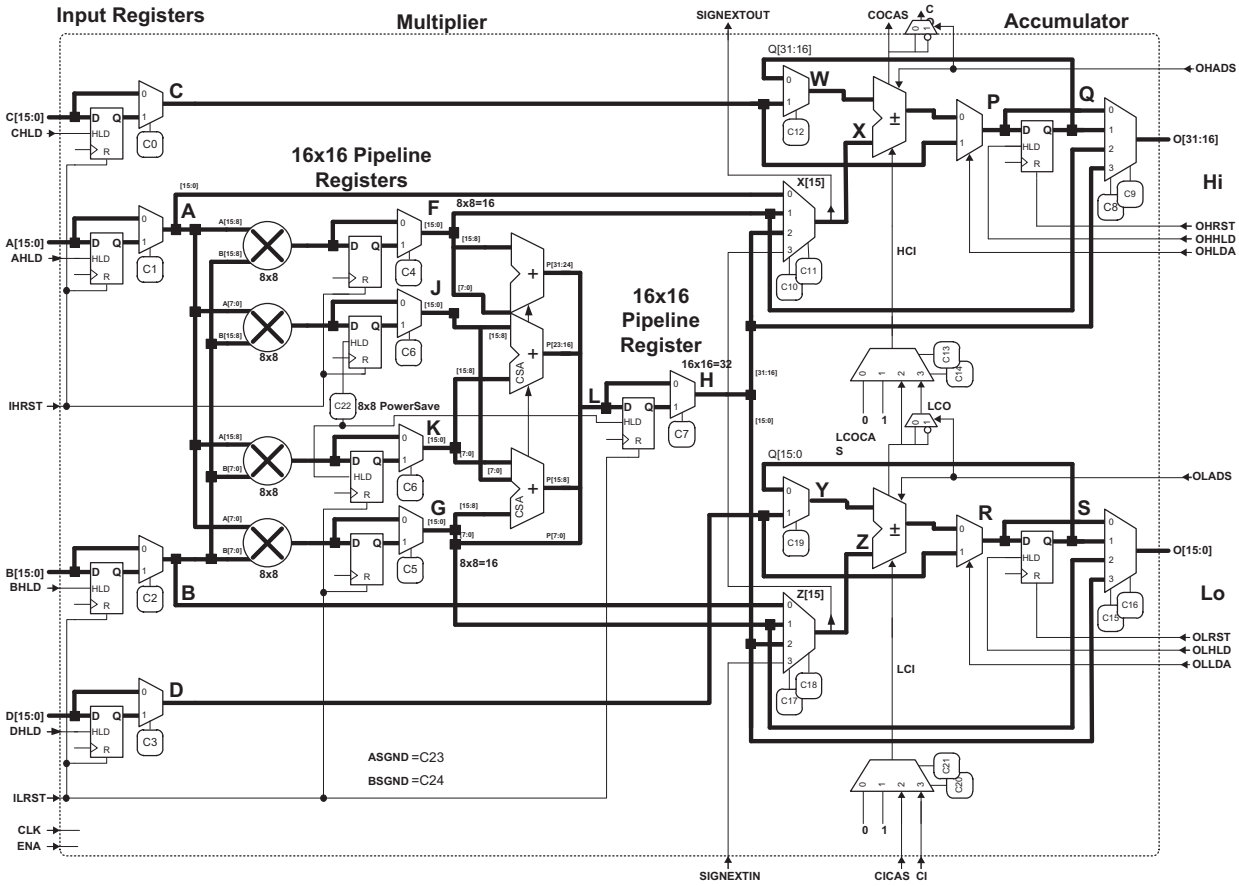


Figure 2-6. sysDSP 8-bit x 8-bit Multiplier

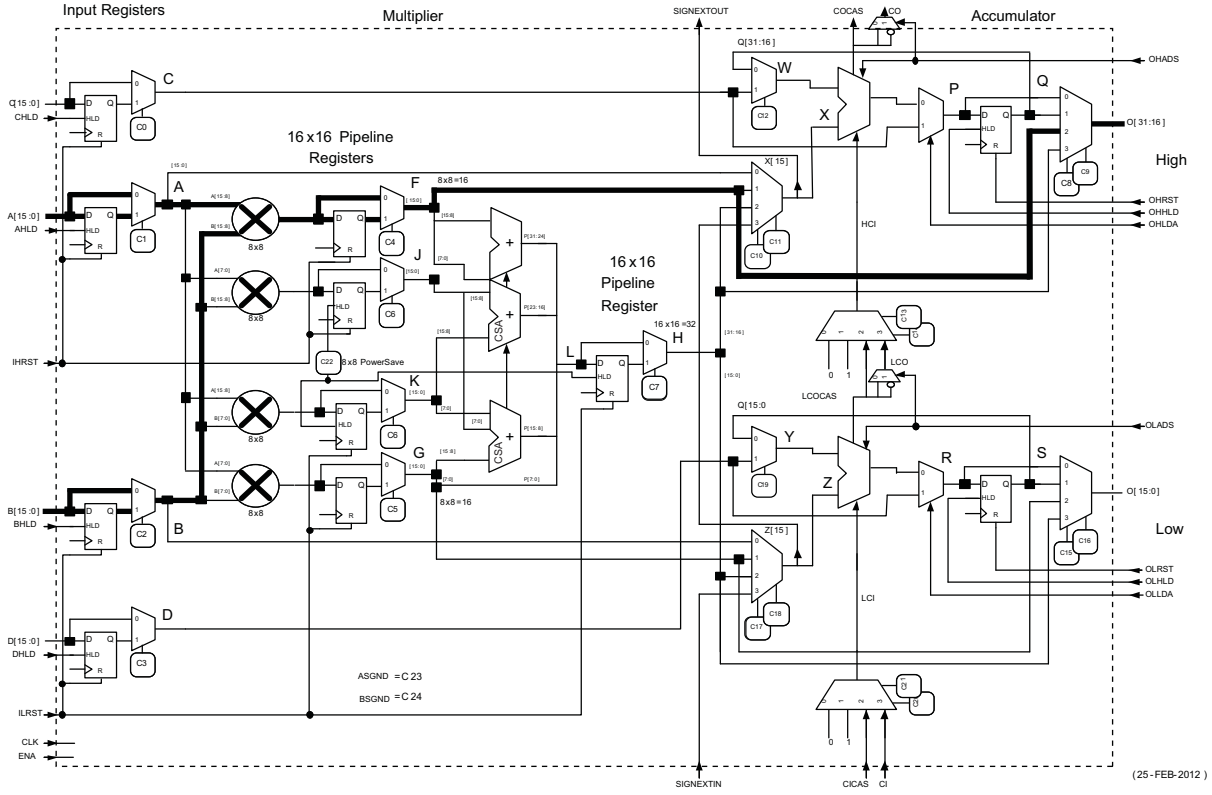


Figure 2-7 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 Ultra sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-8 and Table 2-9 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 Ultra devices.

Differential Comparators

The iCE40 Ultra devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-8. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-9. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

On-Chip Oscillator

The iCE40 Ultra devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

There is one output on each device that can sink up to 500 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 500 mA in increments of 50 mA. This output functions as General Purpose I/O with open-drain when the high current LED drive is not needed.

Embedded PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the embedded PWM IP, please refer to TN1288, iCE40 LED Driver Usage Guide.

Non-Volatile Configuration Memory

All iCE40 Ultra devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration.

iCE40 Ultra Programming and Configuration

This section describes the programming and configuration of the iCE40 Ultra family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 Ultra, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40 Ultra devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 Ultra Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40 Ultra Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.60 V

NVCM Supply Voltage V_{PP_2V5} . . . . . –0.5 V to 3.60 V

PLL Supply Voltage V_{CCPLL} . . . . . –0.5 V to 1.42 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . . –65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Supply Current [1, 2, 3, 4, 5]

Symbol	Parameter	Typ. V_{CC} = 1.2 V[4]	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	71	µA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	0.55	µA
$I_{SPI\_VCCIO1STDBY}$	SPI_V_{CCIO1} Power Supply Static Current	0.5	µA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	0.5	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	8.0	mA
$I_{PP\_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	7.0	mA
$I_{SPI\_VCCIO1PEAK}$	SPI_V_{CCIO1} Power Supply Startup Peak Current	9.0	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	7.5	mA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage, on devices processed in nominal process conditions.
4. Does not include pull-up.
5. Startup Peak Currents are measured with decoupling capacitance of 0.1 uF, 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.

User I^2C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

User SPI Specifications[1, 2]

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software tools. These parameters include the following:
   - — $t_{SUmaster}$ master Setup time (master mode)
   - — $t_{HOLDmaster}$ master Hold time (master mode)
   - — $t_{SUslave}$ slave Setup time (slave mode)
   - — $t_{HOLDslave}$ slave Hold time (slave mode)
   - — $t_{SCK2OUT}$ SCK to out (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI}, t_{LO}) time.

Internal Oscillators (HFOSC, LFOSC)[1]

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	–20%	48	20%	MHz
f_{CLKLF}		LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC clock frequency (t_J = –45 °C–100 °C)	40	50	60	%
DCH_{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

1. Glitchless enabling and disabling OSC clock outputs.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{REF}	Reference Voltage to compare, on V_{INM}	V_{CCIO} = 2.5 V	0.25	V_{CCIO} –0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	—	–250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	V_{CCIO} = 2.5 V	–10	10	µA

Typical Building Block Function Performance[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the Lattice Design Software tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Under worst case operating conditions.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Measured with a toggling pattern

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 Ultra device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time[4]		9.9	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 °C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V Vcc and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1 and 2.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations.
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board.
Configuration				
CRESETB		Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to V_{CCIO_1}.
CDONE		Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kOhm pull-up to SPI_V_{CCIO1}.
PIOB_xx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_32a	SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Signal Name		Function	I/O	Description
PIOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer
PIOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer
PIOT_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer
PIOT_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer
PIOT_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED

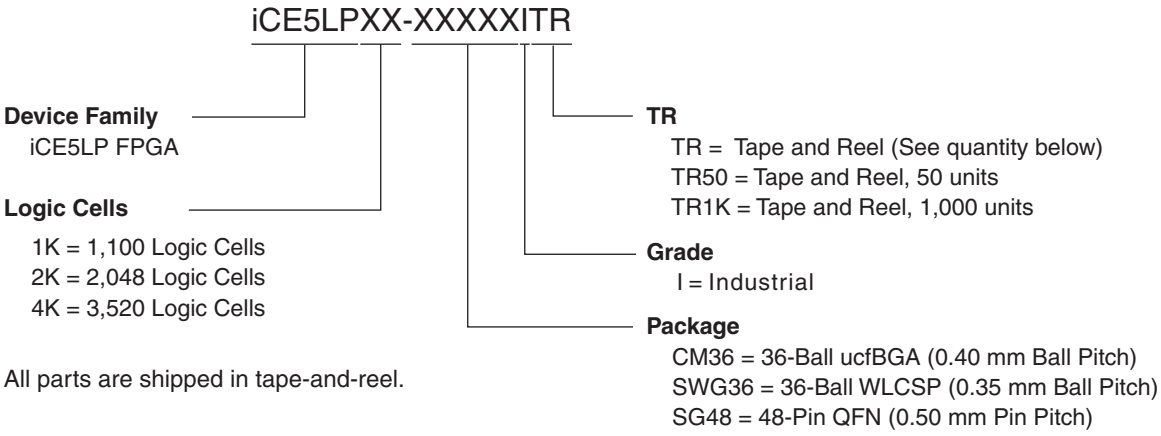
Pin Information Summary

Pin Type		iCE5LP1K			iCE5LP2K			iCE5LP4K		
		CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]	CM36	SWG36	SG48[1]
General Purpose I/O Per Bank	Bank 0	12	5	17	12	5	17	12	5	17
	Bank 1	4	15	14	4	15	14	4	15	14
	Bank 2	10	6	8	10	6	8	10	6	8
Total General Purpose I/Os		26	26	39	26	26	39	26	26	39
V_{CC}		1	1	2	1	1	2	1	1	2
V_{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 1	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V_{CCPLL}		1	1	1	1	1	1	1	1	1
V_{PP_2V5}		1	1	1	1	1	1	1	1	1
Dedicated Config Pins		1	1	2	1	1	2	1	1	2
GND		2	2	0	2	2	0	2	2	0
GND_LED		1	1	0	1	1	0	1	1	0
Total Balls		36	36	48	36	36	48	36	36	48

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

iCE40 Ultra Family Data Sheet Ordering Information

iCE5LP Part Number Description



All parts are shipped in tape-and-reel.

Tape and Reel Quantity

Package	TR Quantity
CM36	4,000
SWG36	5,000
SG48	2,000

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
iCE5LP1K-CM36ITR	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR50	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-CM36ITR1K	1100	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP1K-SWG36ITR	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR50	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SWG36ITR1K	1100	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP1K-SG48ITR	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP1K-SG48ITR50	1100	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-CM36ITR	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR50	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-CM36ITR1K	2048	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP2K-SWG36ITR	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR50	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SWG36ITR1K	2048	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP2K-SG48ITR	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP2K-SG48ITR50	2048	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-CM36ITR	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR50	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-CM36ITR1K	3520	1.2 V	Halogen-Free ucfBGA	36	IND
iCE5LP4K-SWG36ITR	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR50	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SWG36ITR1K	3520	1.2 V	Halogen-Free WLCSP	36	IND
iCE5LP4K-SG48ITR	3520	1.2 V	Halogen-Free QFN	48	IND
iCE5LP4K-SG48ITR50	3520	1.2 V	Halogen-Free QFN	48	IND

Date	Version	Section	Change Summary
April 2015	1.7	Architecture	Updated sysDSP section. Revised the following figures: — Figure 2-5, sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate) — Figure 2-6, sysDSP 8-bit x 8-bit Multiplier — Figure 2-7, DSP 16-bit x 16-bit Multiplier
		Ordering Information	Updated iCE5LP Part Number Description section. Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
March 2015	1.6	Introduction	Updated Features section. — Added BGA and QFN packages in Flexible Logic Architecture. — Added USB 3.1 Type C Cable Detect / Power Delivery Applications in Applications. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Added 36-ball ucfBGA and 48-ball QFN packages. Changed subheading to Total User I/O Count. Changed RBW IP to PWM IP. Deleted footnotes.
		DC and Switching Characteristics	Updated Power-up Sequence section. Indicated all devices in second paragraph.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.
			Replaced the Differential Comparator Electrical Characteristics table.
		Pinout Information	Updated Pin Information Summary section. — Added CM36 and SG48 values. — Changed CRESET_B to Dedicated Config Pins.
		Ordering Information	Updated iCE5LP Part Number Description section. — Added CM36 and SG48 package. — Added TR items.
			Updated Ordering Part Numbers section. Added CM36, SW36 and SG48 part numbers.
October 2014	1.5	Introduction	Updated Features section. — Removed 26 I/O pins for 36-pin WLCSP under Flexible Logic Architecture. — Changed form factor to 2.078 mm x 2.078 mm. — Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 20-Ball WLCSP.
			Updated Introduction section. Changed form factor to 2.078 mm x 2.078 mm.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) section. Removed note in heading regarding sysCLOCK PLL support.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Removed footnote on sysCLOCK PLL support.
			Updated Power-up Sequence section. Removed information on 20-pin WLCSP.
		Pinout Information	Updated Signal Descriptions section. Removed references 20-pin WLCSP.
			Updated Pin Information Summary section. Removed references to UWG20 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 20-ball WLCSP.
			Updated Ordering Part Numbers section. Removed UWG20 part numbers.
		Further Information	Added technical note references.

Date	Version	Section	Change Summary
June 2014	1.2	All	Product name changed to iCE40 Ultra.
		Introduction	Updated Table 1-1, iCE40 Ultra Family Selection Guide. Removed 30-ball WLCSP.
		DC and Switching Characteristics	Updated values in the following sections: — Supply Current — Internal Oscillators (HFOSC, LFOSC) — Power Supply Ramp Rates — Power-On-Reset Voltage Levels — SPI Master or NVCM Configuration Time
			Indicated TBD for values to be determined.
		Pinout Information	Updated Signal Descriptions section. Removed 30-pin WLCSP.
			Updated Pin Information Summary section. Removed SWG30 values.
		Ordering Information	Updated iCE5LP Part Number Description section. Removed 30-ball WLCSP.
			Updated Ordering Part Numbers section. Removed SWG30 and UWG30 part numbers.
May 2014	01.1	Introduction	Updated General Description, Features, and Introduction sections. Removed hardened RGB PWM IP information.
		Architecture	Updated Architecture Overview section. Removed the RGB IP block in Figure 2-1, iCE5LP-4K Device, Top View, Figure 2-8, I/O Bank and Programmable I/O, and in the text content.
			Updated High Current Drive I/O Pins section. Removed hardened RGB PWM IP information.
			Updated Power On Reset section. Removed content on Vccio_2 power down option.
			Replaced RGB PWM Block section with Embedded PWM IP section.
		DC and Switching Characteristics	Removed RGB PWM Block Timing section.
April 2014	01.0	All	Initial release.