NXP USA Inc. - MCIMX6DP4AVT8AAR Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6dp4avt8aar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU3Dv6	Graphics Processing Unit-3D, ver. 6	Multimedia Peripherals	The GPU2Dv6 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 3.0, including extensions, OpenGL ES 2.0, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

- — At power up, an internal ring oscillator is used. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- — Higher accuracy than ring oscillator.
- — If no external crystal is present, then the ring oscillator is used.

The decision to choose a clock source should be based on real-time clock use and precision timeout.

4.1.5 Maximum Measured Supply Currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use case that requires maximum supply current is not a realistic use case.

To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Description of test conditions:

- The Power Virus data shown in Table 8 represent a use case designed specifically to show the maximum current consumption possible for the ARM core complex. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited, if any, practical use case, and be limited to an extremely low duty cycle unless the intention was to specifically cause the worst case power consumption.
- EEMBC CoreMark: Benchmark designed specifically for the purpose of measuring the performance of a CPU core. More information available at www.eembc.org/coremark. Note that this benchmark is designed as a core performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a computationally-intensive application rather than the Power Virus.
- 3DMark Mobile 2011: Suite of benchmarks designed for the purpose of measuring graphics and overall system performance. More information available at www.rightware.com/benchmarks. Note that this benchmark is designed as a graphics performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a very graphics-intensive application.
- Devices used for the tests were from the high current end of the expected process variation.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 8, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for more details on typical power consumption under various use case definitions.

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (1.05 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (1.05 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

Optionally LDO_SOC/VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1 / NVCC_PLL_OUT

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the 24 MHz oscillator, PLLs, and USB PHY. A programmable brown-out detector is included in the regulator that can be used by the

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

CAUTION

> The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 µA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 µA must be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

> The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

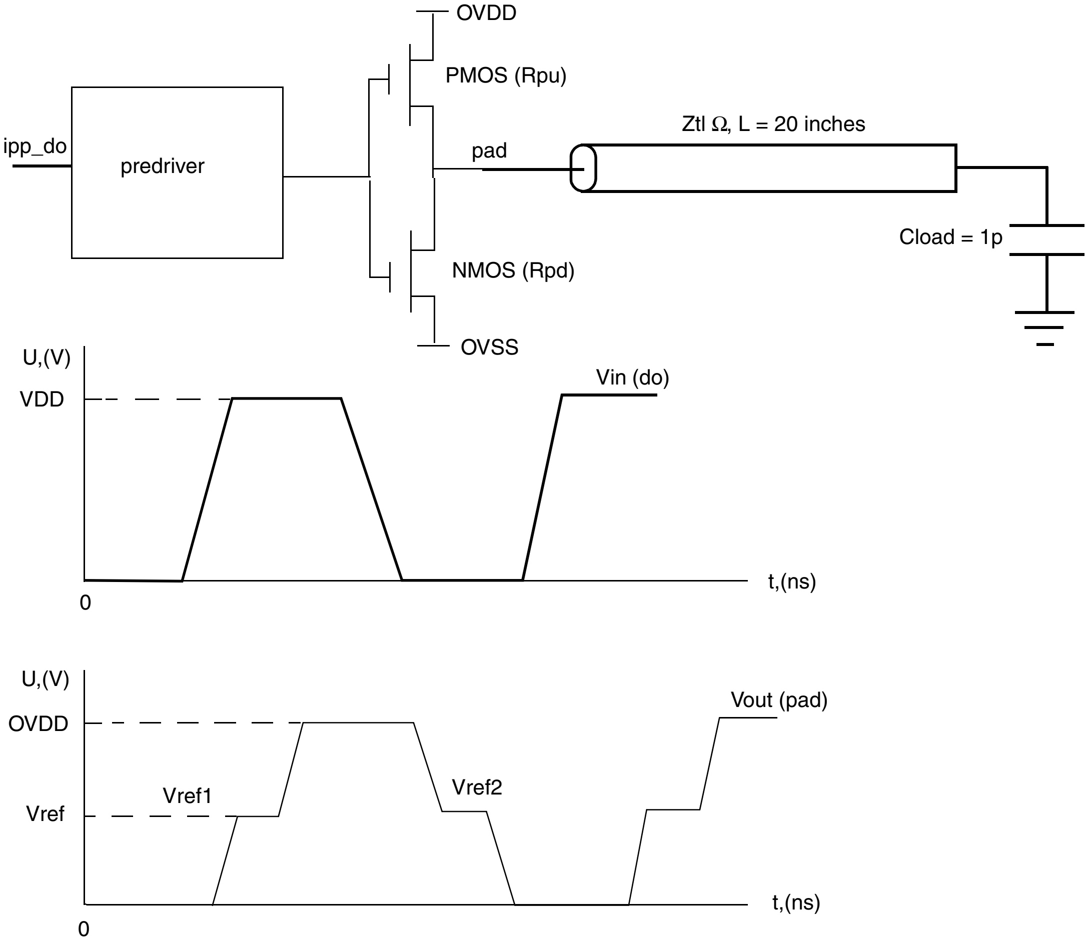
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6DualPlus/6QuadPlus processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).



$$\text{Rpu} = \frac{\text{Vovdd} - \text{Vref1}}{\text{Vref1}} \times \text{Ztl}$$

$$\text{Rpd} = \frac{\text{Vref2}}{\text{Vovdd} - \text{Vref2}} \times \text{Ztl}$$

Figure 9. Impedance Matching Load for Measurement

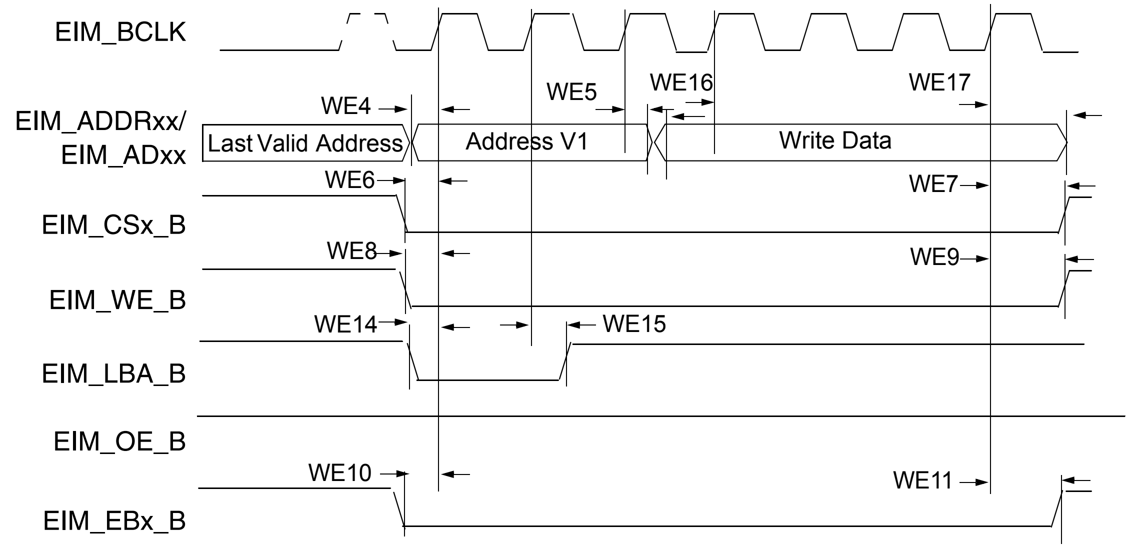


Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

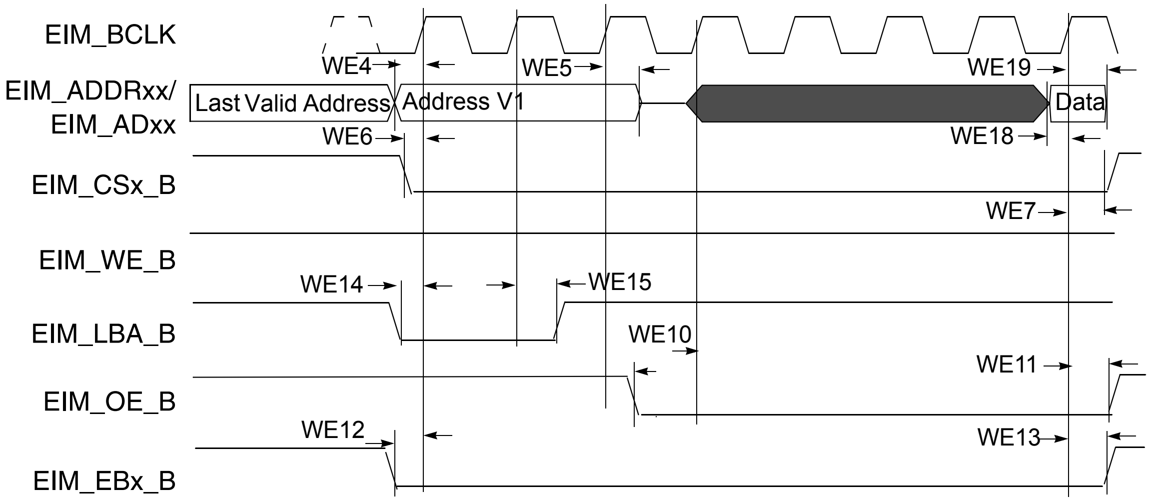


Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

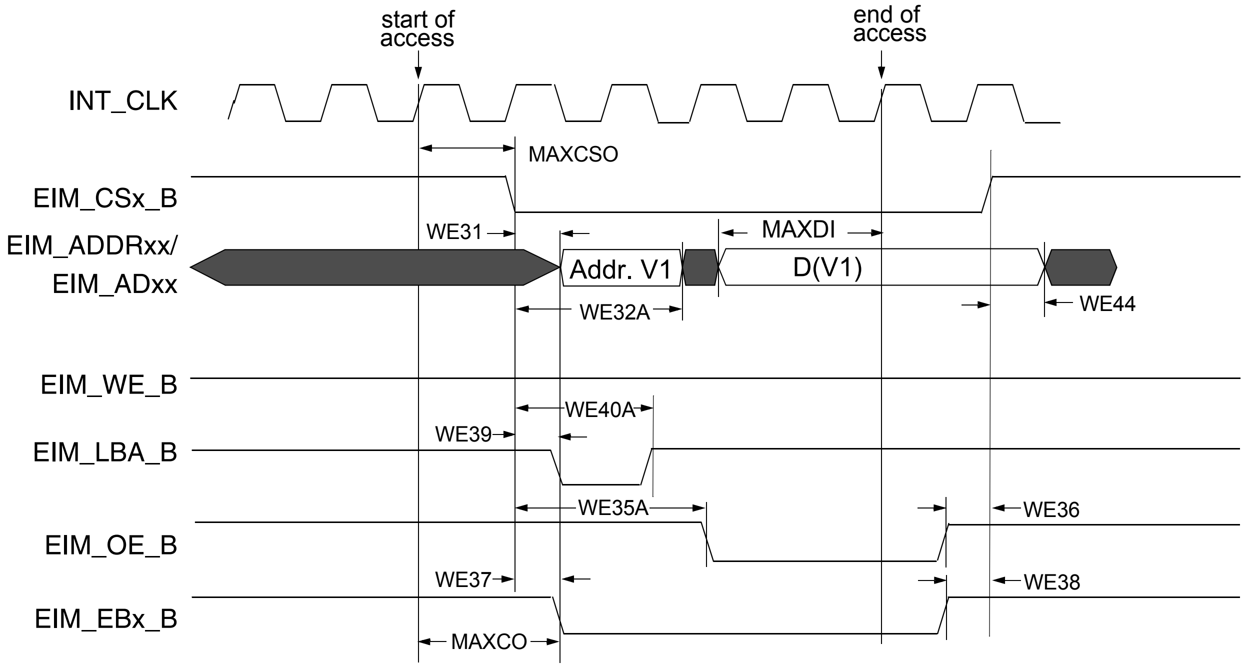


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

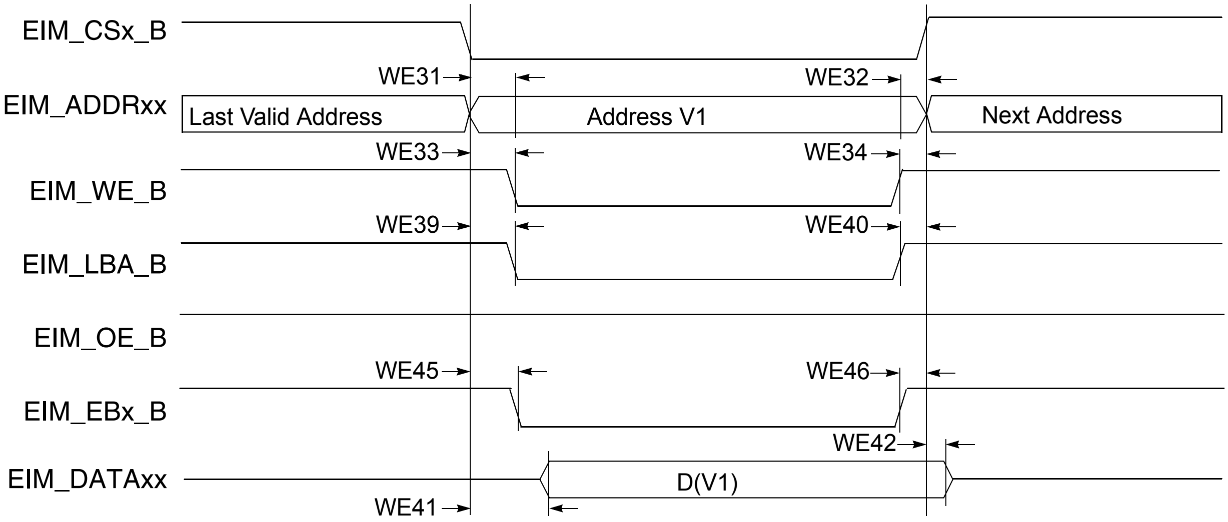


Figure 20. Asynchronous Memory Write Access

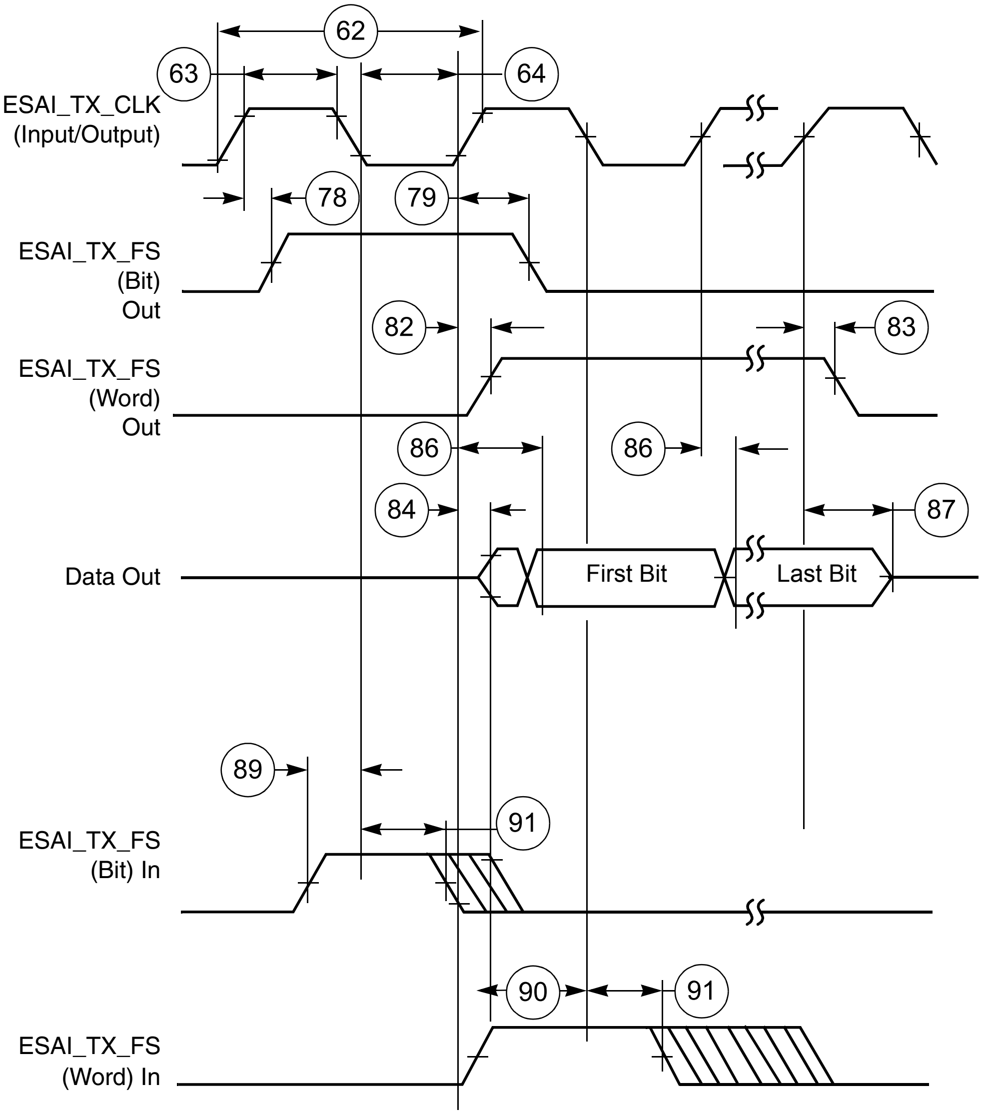


Figure 37. ESAI Transmitter Timing

Table 61. I^2C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

[1] A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

[2] The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

[3] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

[4] C_b = total capacitance of one bus line in pF.

4.12.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

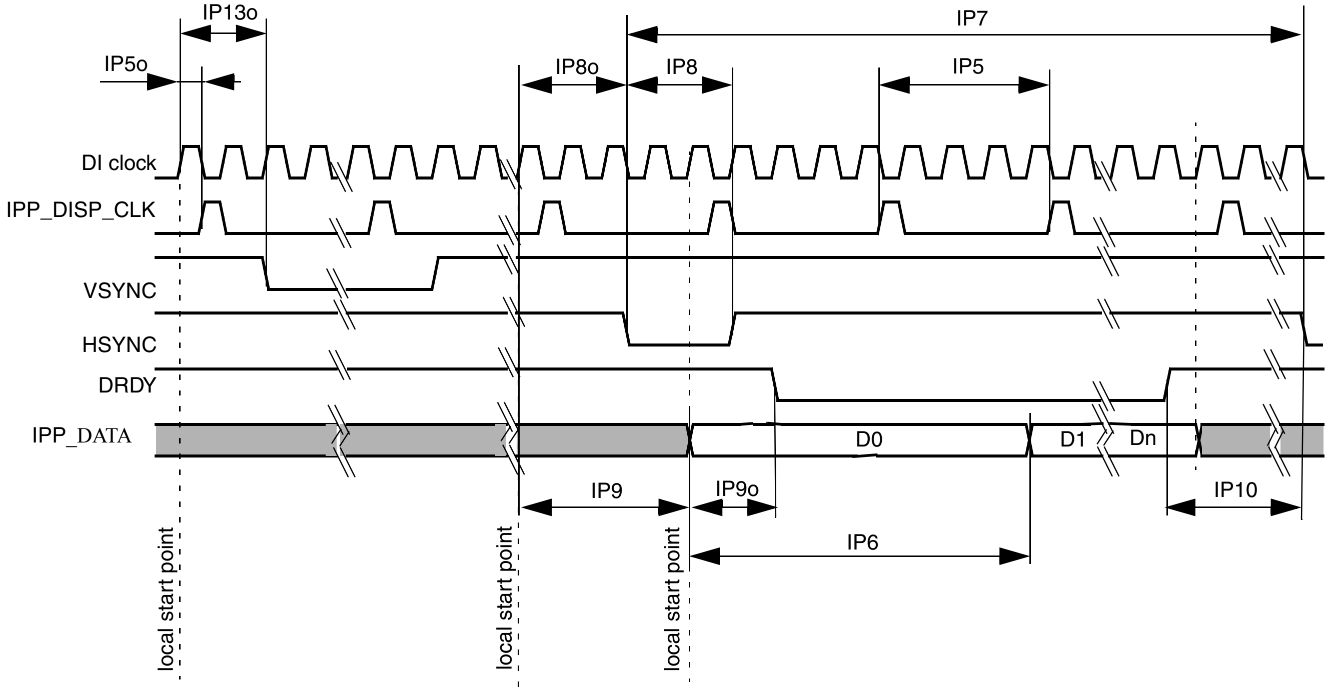


Figure 63. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 64 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

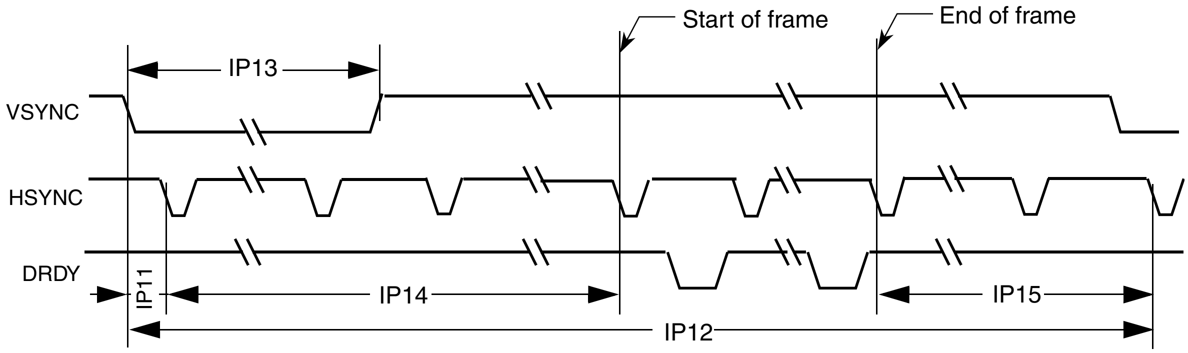


Figure 64. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 65. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

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[1] Display interface clock period immediate value.

$$\mathrm{Tdicp} = \begin{cases} \mathrm{T_{diclk}} \times \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}, & \text{for integer } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \\ \mathrm{T_{diclk}}\left(\mathrm{floor}\left[\dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\bar{\mathrm{T}}\mathrm{dicp} = \mathrm{T_{diclk}} \times \frac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$\mathrm{Accuracy} = (0.5 \times \mathrm{T_{diclk}}) \pm 0.62\mathrm{ns}$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$\mathrm{Accuracy} = \mathrm{T_{diclk}} \pm 0.62\mathrm{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

4.12.13.9 DATA and FLAG Signal Timing

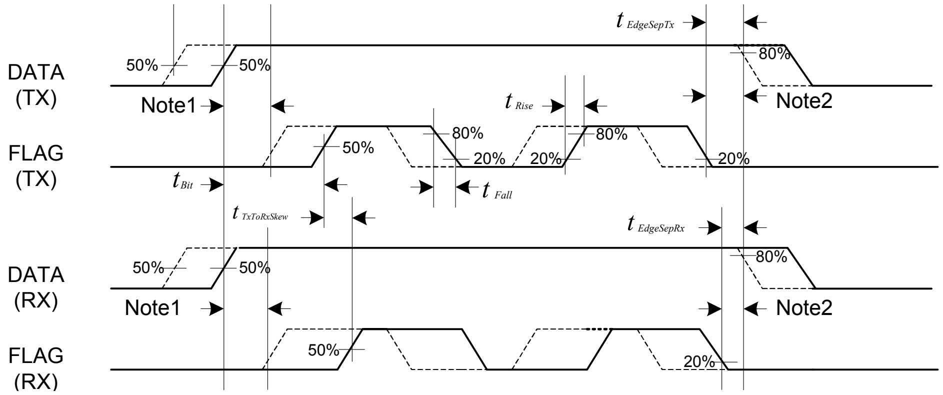

Figure 80. DATA and FLAG Signal Timing

4.12.14 MediaLB (MLB) Characteristics

4.12.14.1 MediaLB (MLB) DC Characteristics

Table 71 lists the MediaLB 3-pin interface electrical characteristics.

Table 71. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	$I_{OL} = 6$ mA	—	0.4	V
High level output threshold	V_{OH}	$I_{OH} = –6$ mA	2.0	—	V
Input leakage current	I_L	$0 < V_{in} <$ VDD	—	±10	µA

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 72 lists the MediaLB 6-pin interface electrical characteristics.

Table 72. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV

Table 72. MediaLB 6-Pin Interface Electrical DC Specifications (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\mid V_{OCM, high} - V_{OCM, low} \mid$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\mid I_{OS} \mid$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					
Differential clock input:		See Note[4]			
• logic low steady-state	V_{ILC}			-50	mV
• logic high steady-state	V_{IHC}		50		mV
• hysteresis	V_{HSC}		-25	25	mV
Differential signal/data input:		—			
• logic low steady-state	V_{ILS}		—	-50	mV
• logic high steady-state	V_{IHS}		50	—	mV
Signal-ended input voltage (steady-state):		—			
• MLB_SIG_P, MLB_DATA_P	V_{IN+}		0.5	2.0	V
• MLB_SIG_N, MLB_DATA_N	V_{IN-}		0.5	2.0	V

[1] The signal-ended output voltage of a driver is defined as V_{O+} on MLB_CLK_P, MLB_SIG_P, and MLB_DATA_P. The signal-ended output voltage of a driver is defined as V_{O-} on MLB_CLK_N, MLB_SIG_N, and MLB_DATA_N.

[2] Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-}.

[3] Short circuit current is applicable when V_{O+} and V_{O-} are shorted together and/or shorted to ground.

[4] The logic state of the receiver is undefined when $-50\ mV < V_{ID} < 50\ mV$.

Table 80. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	 ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	 ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

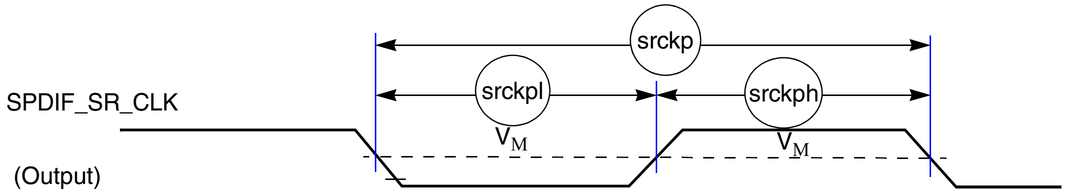

Figure 88. SPDIF_SR_CLK Timing Diagram

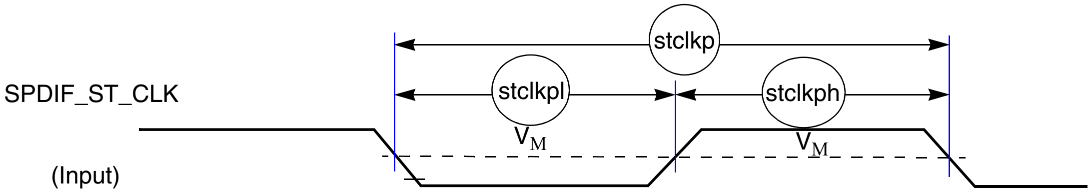

Figure 89. SPDIF_ST_CLK Timing Diagram

4.12.22 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

> HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.12.22.1 Transmit Timing

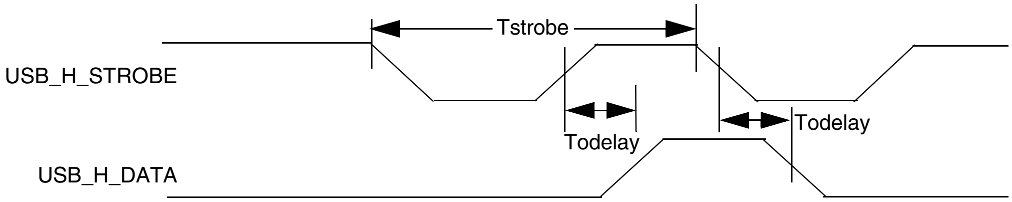

Figure 98. USB HSIC Transmit Waveform

Table 91. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.12.22.2 Receive Timing

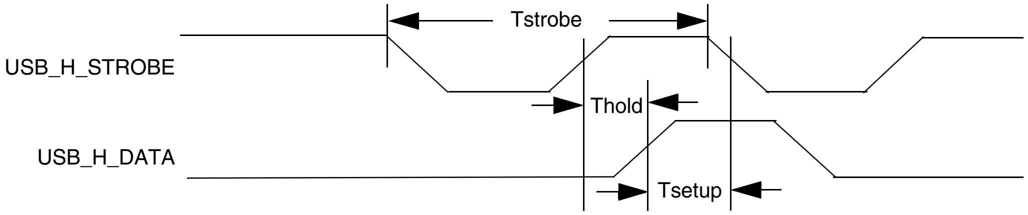

Figure 99. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

Table 94. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	PU (100K)
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	PU (100K)
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	PU (100K)
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	PU (100K)
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	0
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	0