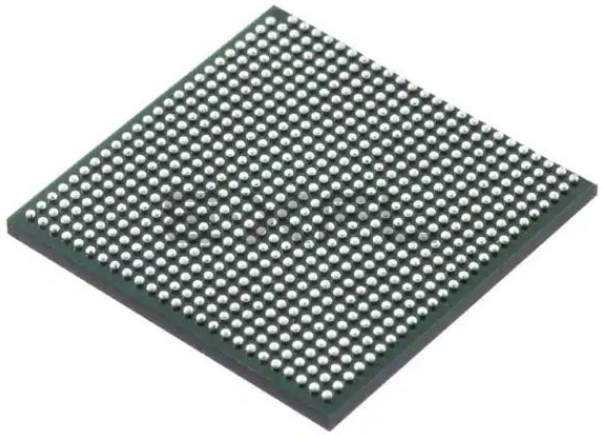

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6dp6avt1ab

- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 170 Mpixels/sec (for example, WUXGA at 60 Hz) or two ports up to 85 MP/sec each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6DualPlus/6QuadPlus processor has four lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated High Speed Inter-Chip (HS-IC) USB PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while the other four support 4-wire. This is due to the SoC IOMUX limitation, because all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI)
  - Three I2C, supporting 400 kbps

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 18. MLB PLL Electrical Parameters

Parameter	Value
Lock time	<1.5 ms

4.4.6 ARM PLL

Table 19. ARM PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA must be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

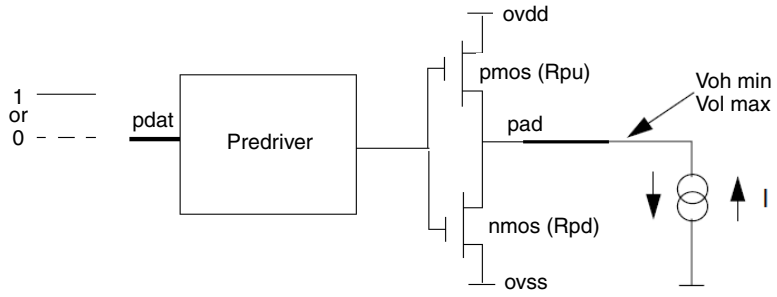


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

Table 21. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 (See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 32 KHz RTC clock @ 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 25. DDR3/DDR3L I/O DC Electrical Parameters (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	See Note[3]	V
Differential input Logic Low	Vil(diff)	—	See Note[3]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49 × OVDD	0.51 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	μA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	105	175	kΩ

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L).

2 Vref – DDR3/DDR3L external reference voltage.

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 31).

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 26 shows the Low Voltage Differential Signalling (LVDS) I/O DC parameters.

Table 26. LVDS I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	Rload=100 Ω between padP and padN	250	450	mV
Output High Voltage	V_{OH}	I_{OH} = 0 mA	1.25	1.6	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	0.9	1.25	
Offset Voltage	V_{OS}	—	1.125	1.375	

4.6.6 MLB 6-Pin I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, "MediaLB 6-pin interface Electrical Characteristics" for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192fs.

Table 27 shows the Media Local Bus (MLB) I/O DC parameters.

4.12.4.3 SDR50/SDR104 AC Timing

Figure 41 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

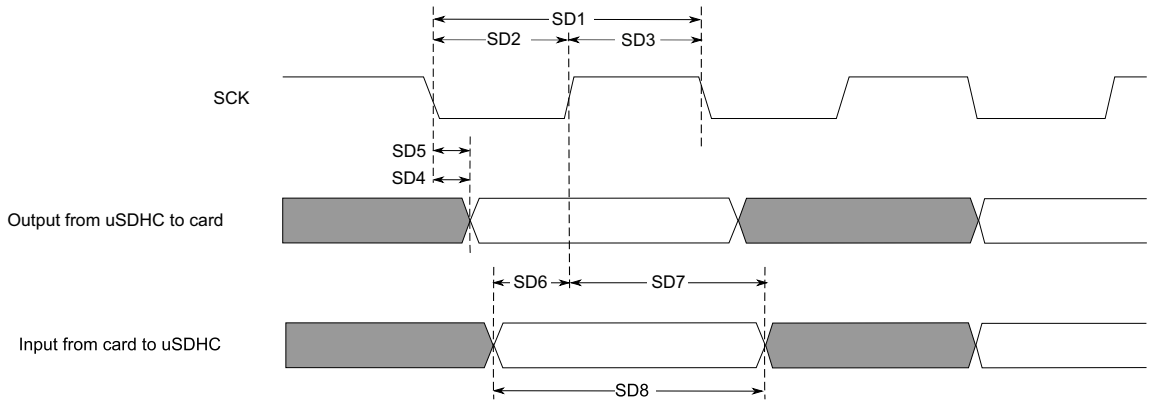


Figure 41. SDR50/SDR104 Timing

Table 52. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

Table 61. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.12.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

stops receiving data from the stream. For the next line, the IPU2_CSIx_HSYNC timing repeats. For the next frame, the IPU2_CSIx_VSYNC timing repeats.

4.12.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.12.10.2.2, "Gated Clock Mode,") except for the IPU2_CSIx_HSYNC signal, which is not used (see Figure 60). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPU2_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

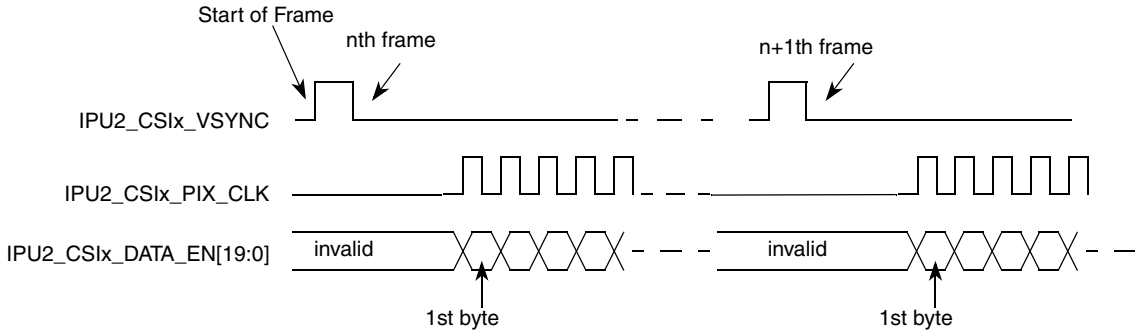


Figure 60. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 60 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPU2_CSIx_VSYNC; active-high/low IPU2_CSIx_HSYNC; and rising/falling-edge triggered IPU2_CSIx_PIX_CLK.

Table 65. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

4.12.13.9 DATA and FLAG Signal Timing

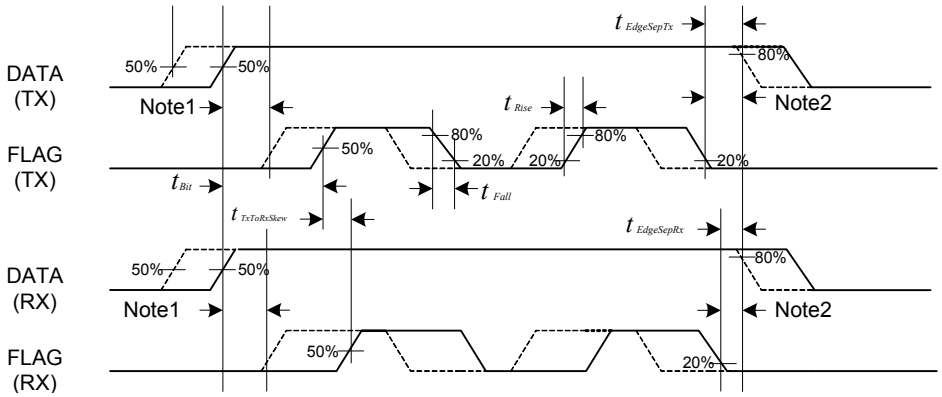


Figure 80. DATA and FLAG Signal Timing

4.12.14 MediaLB (MLB) Characteristics

4.12.14.1 MediaLB (MLB) DC Characteristics

Table 71 lists the MediaLB 3-pin interface electrical characteristics.

Table 71. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_L	0 < V_{in} < VDD	—	±10	µA

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 72 lists the MediaLB 6-pin interface electrical characteristics.

Table 72. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): I V_{O+} - V_{O-} I	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: I $V_{OD, high}$ - $V_{OD, low}$ I	ΔV_{OD}	—	-50	50	mV

4.12.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 81 show the timing of MediaLB 3-pin interface, and Table 73 and Table 74 lists the MediaLB 3-pin interface timing characteristics.

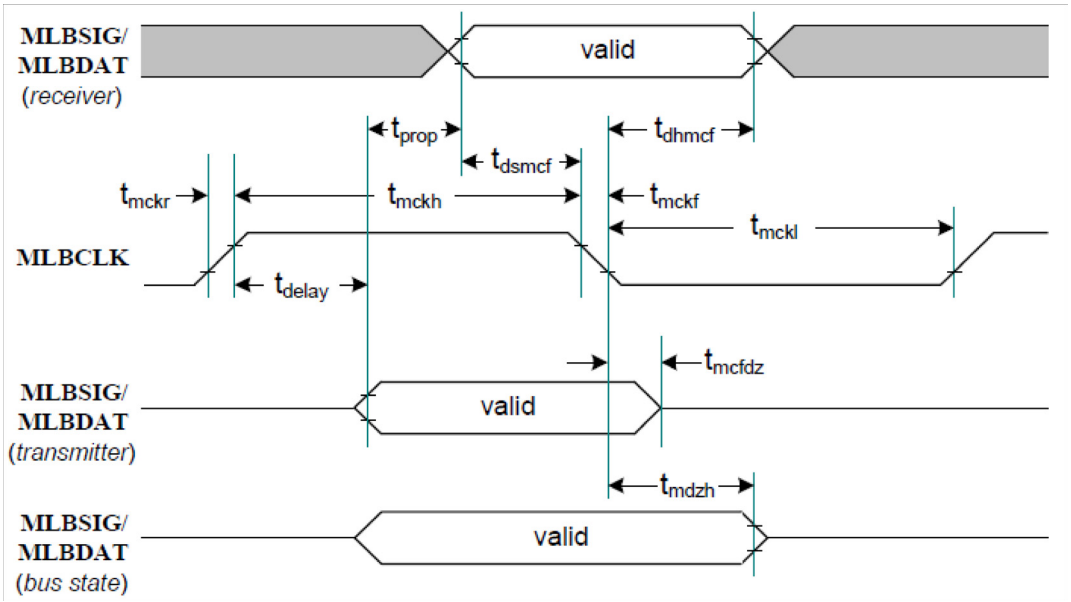


Figure 81. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 73. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK operating frequency[1]	f_{mck}	11.264	 25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLB_CLK low time[2]	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLB_CLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	(see [3])

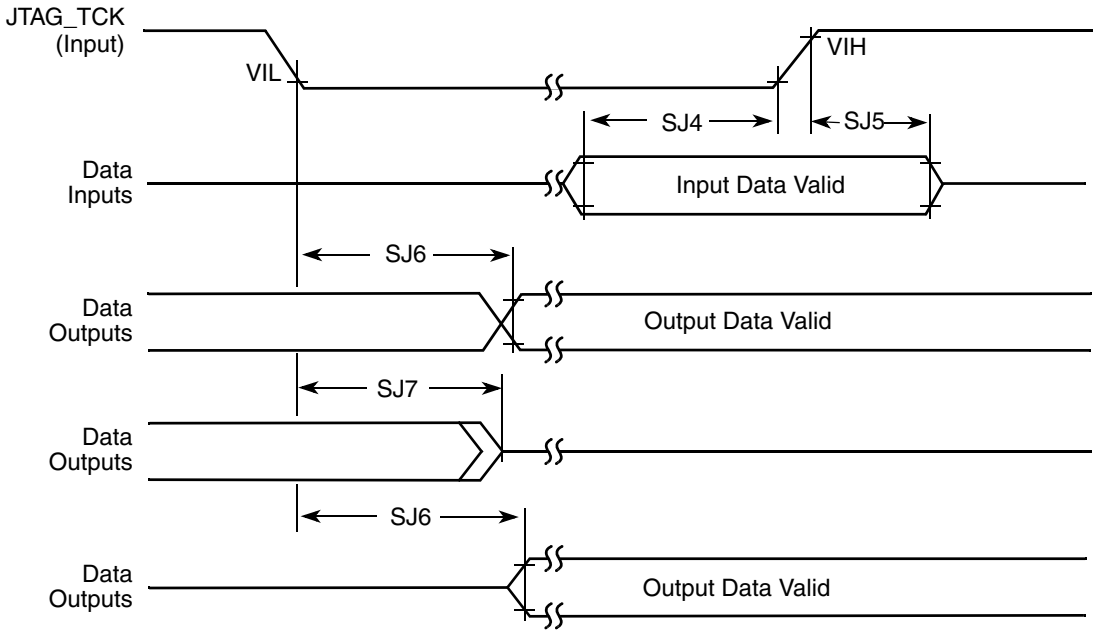


Figure 85. Boundary Scan (JTAG) Timing Diagram

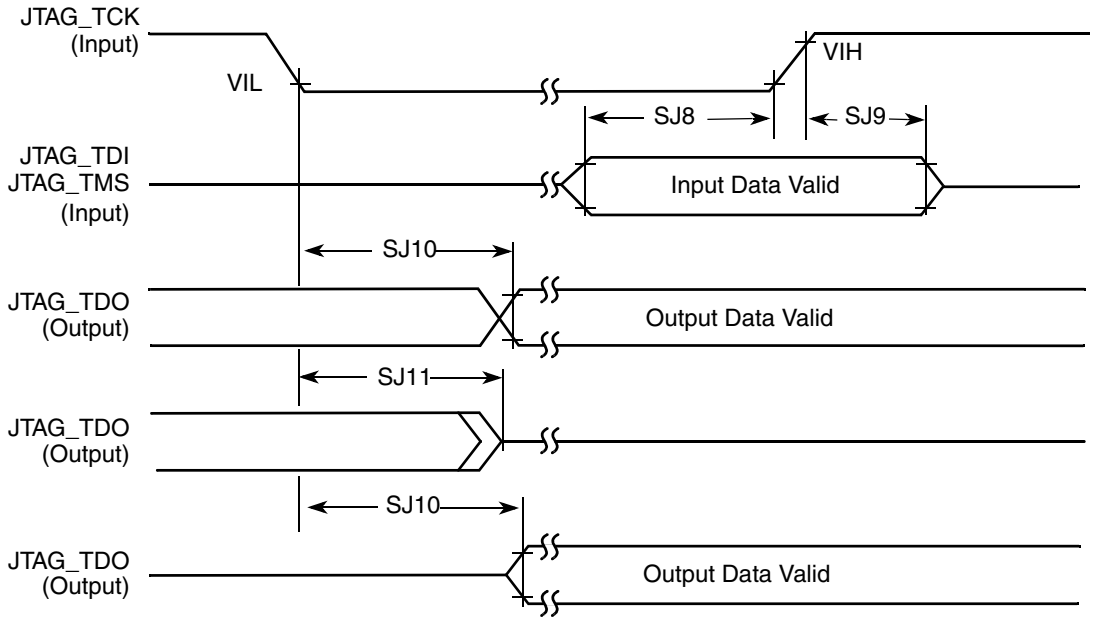


Figure 86. Test Access Port Timing Diagram

4.12.20 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 81.

Table 81. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.12.20.1 SSI Transmitter Timing with Internal Clock

Figure 90 depicts the SSI transmitter internal clock timing and Table 82 lists the timing parameters for the SSI transmitter internal clock.

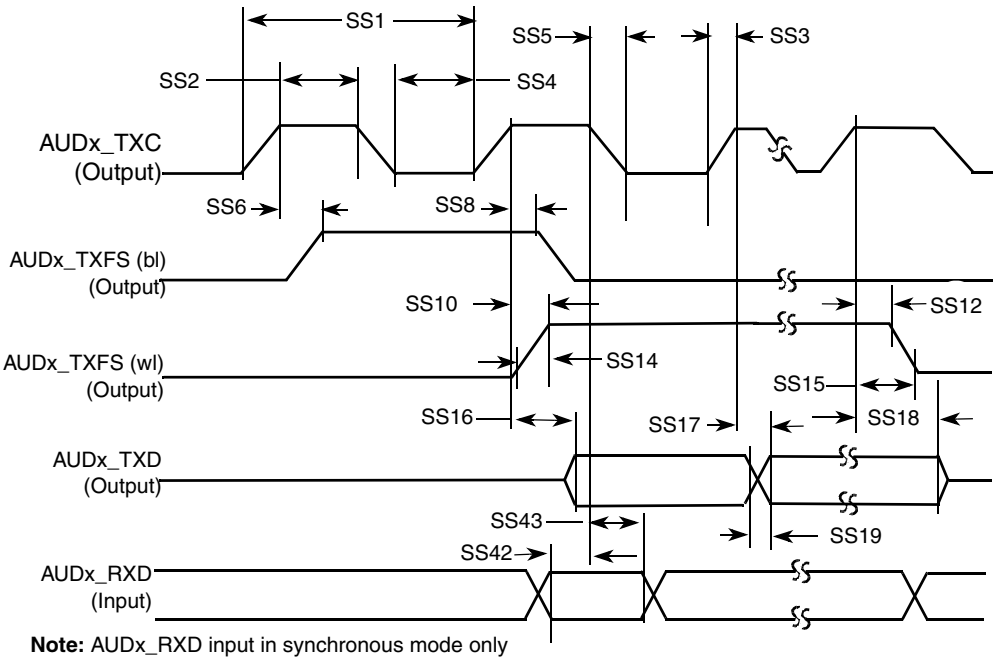


Figure 90. SSI Transmitter Internal Clock Timing Diagram

4.12.20.3 SSI Transmitter Timing with External Clock

Figure 92 depicts the SSI transmitter external clock timing and Table 84 lists the timing parameters for the transmitter timing with the external clock.

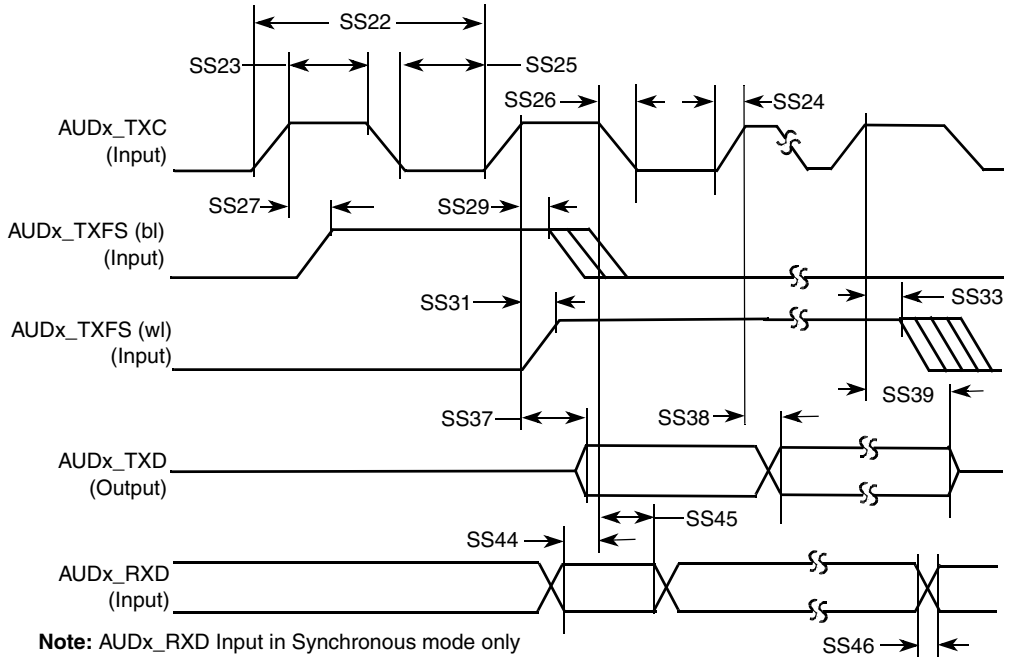


Figure 92. SSI Transmitter External Clock Timing Diagram

Table 84. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

4.12.21 UART I/O Configuration and Timing Parameters

4.12.21.1 UART RS-232 I/O Configuration in Different Modes

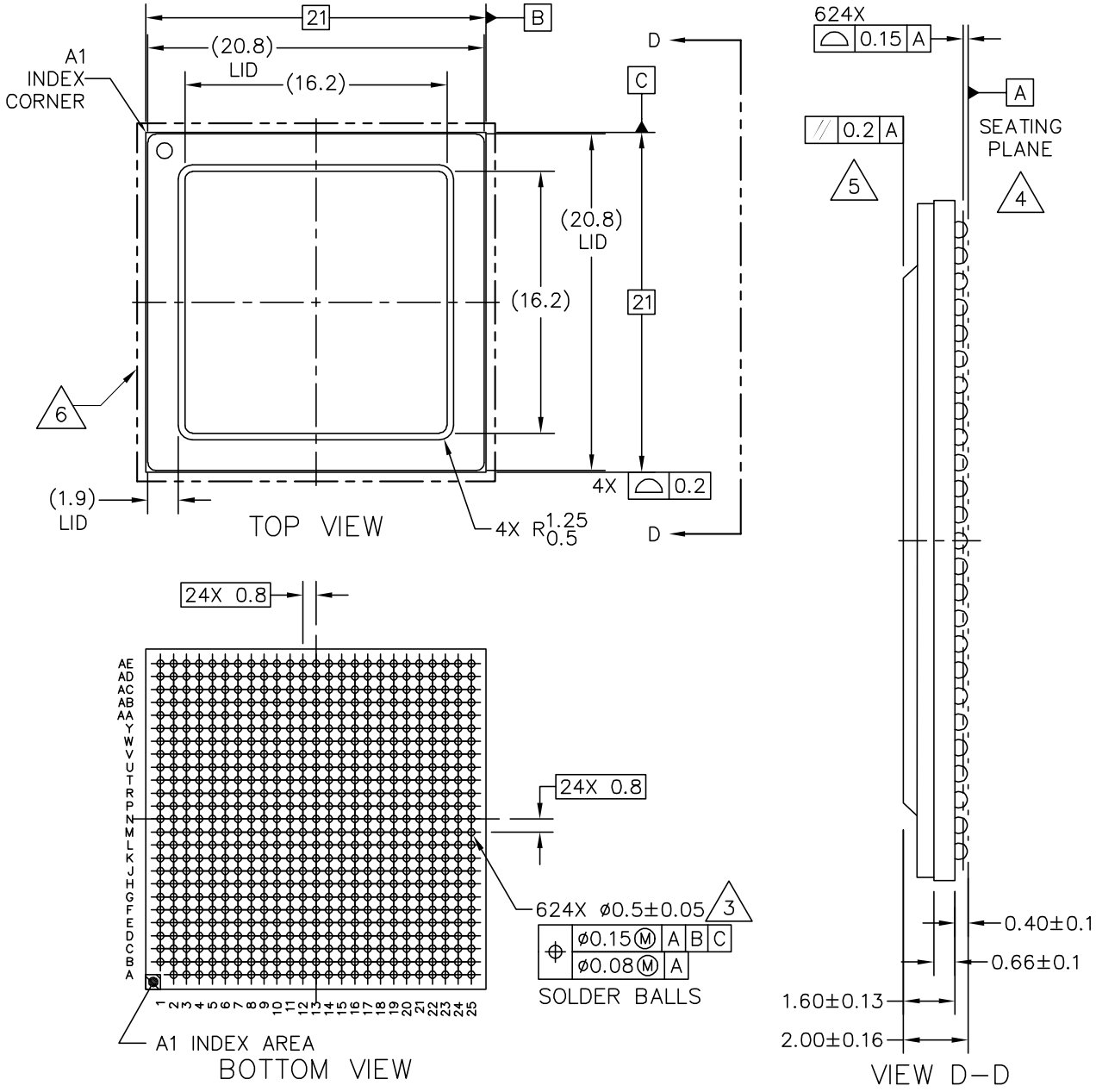
The i.MX 6DualPlus/6QuadPlus UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

6.2.1.1 21 x 21 mm Lidded Package

Figure 100 and Figure 101 show the top, bottom, and side views of the 21 × 21 mm lidded package.



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TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D	REV: E
	STANDARD: NON–JEDEC	
	SOT1643–1	07 JAN 2016

Figure 100. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 1 of 2)

6.2.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 95 shows the device connection list for ground, power, sense, and reference contact signals.

Table 95. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
FA_ANA	A5	—
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	—
GPANAIO	C8	Analog output for NXP use only. This output must remain unconnected
HDMI_DDCCEC	K2	Analog ground reference for the Hot Plug detect signal
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
LVDS0_TX1_P	U3	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX1_P	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX2_P	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX3_N	—	—
LVDS0_TX3_P	W1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS_2P5	LVDS	—	LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX1_P	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_N	—	—
MLB_CP	B11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_P	—	—
MLB_DN	B10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_N	—	—
MLB_DP	A10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_P	—	—
MLB_SN	A9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_N	—	—
MLB_SP	B9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	PU (100K)

6.2.5 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 98 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map

	A	B	C	D	E	F	G
1		PCIE_RXM	GND	CSI_D1M	CSI_D2M	CSI_D3P	DSI_D0P
2	PCIE_REXT	PCIE_RXP	JTAG_TRSTB	CSI_D1P	CSI_D2P	CSI_D3M	DSI_D0M
3	PCIE_TXM	PCIE_TXP	JTAG_TMS	GND	CSI_D0P	CSI_CLK0P	GND
4	GND	GND	GND	CSI_REXT	CSI_D0M	CSI_CLK0M	DSI_REXT
5	FA_ANA	VDD_FA	CLK2_N	CLK2_P	GND	GND	JTAG_TDI
6	USB_OTG_DP	USB_OTG_DN	GND	GND	GND	GND	JTAG_TDO
7	XTALI	XTALO	CLK1_N	CLK1_P	GND	GND	PCIE_VPH
8	GND	USB_OTG_CHD_B	GPANAIO	GND	NVCC_PLL_OUT	GND	PCIE_VPTX
9	MLB_SN	MLB_SP	RTC_XTALO	RTC_XTALI	USB_OTG_VBUS	VDDUSB_CAP	VDD_SNVS_CAP
10	MLB_DP	MLB_DN	GND	USB_H1_VBUS	USB_H1_DP	USB_H1_DN	GND
11	MLB_CN	MLB_CP	POR_B	PMIC_ON_REQ	TAMPER	PMIC_STBY_REQ	VDD_SNVS_IN
12	SATA_TXP	SATA_TXM	BOOT_MODE0	ONOFF	TEST_MODE	BOOT_MODE1	SATA_VPH
13	GND	SD3_CMD	SD3_DAT5	SD3_DAT4	SD3_DAT6	SD3_DAT7	SATA_VP
14	SATA_RXM	SATA_RXP	SATA_REXT	SD3_CLK	SD3_DAT0	SD3_DAT1	NVCC_SD3
15	SD3_DAT2	SD3_DAT3	NANDF_CLE	SD3_RST	NANDF_WP_B	NANDF_CS0	NVCC_NANDF
16	NANDF_ALE	NANDF_RB0	NANDF_CS1	NANDF_CS3	SD4_CLK	NANDF_D2	NVCC_SD1
17	NANDF_CS2	SD4_CMD	NANDF_D1	NANDF_D3	NANDF_D6	SD4_DAT2	NVCC_SD2
18	NANDF_D0	NANDF_D5	NANDF_D7	SD4_DAT0	SD4_DAT4	SD1_DAT3	NVCC_RGMII
19	NANDF_D4	SD4_DAT1	SD4_DAT5	SD4_DAT7	SD1_DAT2	SD2_CMD	GND
20	SD4_DAT3	SD4_DAT6	SD1_DAT1	SD1_CLK	SD2_DAT1	RGMII_TD1	EIM_D20
21	SD1_DAT0	SD1_CMD	SD2_CLK	RGMII_TXC	RGMII_TD2	EIM_D17	EIM_D19
22	SD2_DAT0	SD2_DAT3	RGMII_TD0	RGMII_RX_CTL	EIM_EB2	EIM_D24	EIM_D25
23	SD2_DAT2	RGMII_RD1	RGMII_TX_CTL	RGMII_RD3	EIM_D22	EIM_EB3	EIM_D28
24	RGMII_TD3	RGMII_RD2	RGMII_RD0	EIM_D18	EIM_D26	EIM_A22	EIM_A17
25	GND	RGMII_RXC	EIM_D16	EIM_D23	EIM_D27	EIM_A24	EIM_A19

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
AC	DRAM_D4	DRAM_VREF	DRAM_DQM0	DRAM_D2	DRAM_D13	DRAM_DQM1	DRAM_D15	DRAM_D22	DRAM_D28	DRAM_SDQS3	DRAM_D31	DRAM_A11	DRAM_A6	DRAM_A0	DRAM_SDBA0	DRAM_SDODT0	DRAM_A13	DRAM_D34	DRAM_D39	DRAM_DQM5	DRAM_D47	DRAM_D48	DRAM_D53	DRAM_D51	DRAM_D55
AD	DRAM_D5	DRAM_D0	DRAM_SDQS0_B	GND	DRAM_D8	DRAM_SDQS1	GND	DRAM_SDQS2	DRAM_D29	GND	DRAM_D30	DRAM_A12	GND	DRAM_SDCLK_1	DRAM_SDCLK_0	GND	DRAM_CS1	DRAM_SDQS4	GND	DRAM_SDQS5	DRAM_D43	GND	DRAM_SDQS6	DRAM_DQM6	DRAM_D54
AE	GND	DRAM_D1	DRAM_SDQS0	DRAM_D7	DRAM_D9	DRAM_SDQS1_B	DRAM_D11	DRAM_SDQS2_B	DRAM_D24	DRAM_DQM3	DRAM_D26	DRAM_A9	DRAM_A5	DRAM_SDCLK_1_B	DRAM_SDCLK_0_B	DRAM_CAS	ZQPAD	DRAM_SDQS4_B	DRAM_D35	DRAM_SDQS5_B	DRAM_D46	DRAM_D49	DRAM_SDQS6_B	DRAM_D50	GND