E·XFL



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6qp4avt1ab

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.2 Features

The i.MX 6DualPlus/6QuadPlus processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone[®])
- The core configuration is symmetric, where each core includes:
 - 32 KByte L1 Instruction Cache
 - 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 6.
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 512 KB)
- Secure/non-secure RAM (16 KB)
- External memory interfaces:
 - 16-bit, 32-bit, and 64-bit DDR3-1066, DDR3L-1066, and 1/2 LPDDR2-800 channels, supporting DDR interleaving mode, for dual x32 LPDDR2
 - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNANDTM and others. BCH ECC up to 40 bit.
 - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
 - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6DualPlus/6QuadPlus processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

• Hard Disk Drives—SATA II, 3.0 Gbps

Introduction

- Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000¹ Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)
- MLB (MediaLB) provides interface to MOST Networks (150 Mbps)

The i.MX 6DualPlus/6QuadPlus processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6DualPlus/6QuadPlus processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6DualPlus/6QuadPlus processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv6—3D Graphics Processing Unit (OpenGL ES 3.0) version 6
- GPU2Dv3—2D Graphics Processing Unit (BitBlt) version 3
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- 4 x PRE—Prefetch and Resolve Engine
- 2 x PRG—Prefetch and Resolve Gasket
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	 LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: One clock pair Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST [®] data network, using the standardized MediaLB protocol (up to 150 Mbps). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	 DDR Controller has the following features: Supports 16/32/64-bit DDR3 / DDR3L or LPDDR2 Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) Supports LPDDR2 up to 400 MHz and DDR3 up to 532 MHz Supports up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6DualPlus/6QuadPlus processors, the OCRAM is used for controlling the 512 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCle	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	 The EIM NOR-FLASH / PSRAM provides: Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 FCPBGA Package Thermal Resistance

Table 5 provides the FCPBGA package thermal resistance data for the *lidded* package type.

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient ¹	Single-layer board (1s); natural convection ²	R _{θJA}	24	°C/W
	Four-layer board (2s2p); natural convection ²	R _{θJA}	15	°C/W
Junction to Ambient ¹	Single-layer board (1s); air flow 200 ft/min ³	R _{θJMA}	17	°C/W
	Four-layer board (2s2p); air flow 200 ft/min ⁴	R _{θJMA}	12	°C/W
Junction to Board ^{1,4}	_	$R_{\theta JB}$	5	°C/W
Junction to Case (top) ^{1,5}	—	R _{0JCtop}	1	°C/W

 Table 5. FCPBGA Package Thermal Resistance Data (Lidded)

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per JEDEC JESD51-3 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

- ³ Per JEDEC JESD51-6 with the board horizontal.
- ⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.6.4 RGMII I/O 2.5V I/O DC Electrical Parameters

The RGMII interface complies with the RGMII standard version 1.3. The parameters in Table 23 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage ¹	V _{OH}	loh= -0.1 mA (DSE=001,010) loh= -1.0 mA (DSE=011,100,101,110,111)	OVDD-0.15	—	V
Low-level output voltage ¹	V _{OL}	lol= 0.1 mA (DSE=001,010) lol= 1.0 mA (DSE=011,100,101,110,111)	_	0.15	V
Input Reference Voltage	V _{ref}	_	0.49xOVDD	0.51xOVDD	V
High-Level input voltage 2, 3	V _{IH}	_	0.7xOVDD	OVDD	V
Low-Level input voltage 2, 3	V _{IL}	_	0	0.3xOVDD	V
Input Hysteresis(OVDD=1.8V)	V _{HYS_HighVDD}	OVDD=1.8V	250	—	mV
Input Hysteresis(OVDD=2.5V)	$V_{HYS_HighVDD}$	OVDD=2.5V	250	—	mV
Schmitt trigger VT+ 3, 4	V _{TH+}	_	0.5xOVDD	—	mV
Schmitt trigger VT- 3, 4	V _{TH-}	_	—	0.5xOVDD	mV
Pull-up resistor (22 k Ω PU)	R _{PU_22K}	V _{in} =0V	_	212	μA
Pull-up resistor (22 k Ω PU)	R _{PU_22K}	V _{in} =OVDD	—	1	μA
Pull-up resistor (47 k Ω PU)	R _{PU_47K}	V _{in} =0V	—	100	μA
Pull-up resistor (47 k Ω PU)	R _{PU_47K}	V _{in} =OVDD	—	1	μA
Pull-up resistor (100 k Ω PU)	R _{PU_100K}	V _{in} =0V	_	48	μA
Pull-up resistor (100 k Ω PU)	R _{PU_100K}	V _{in} =OVDD	—	1	μA
Pull-down resistor (100 k Ω PD)	R _{PD_100K}	V _{in} =OVDD	—	48	μA
Pull-down resistor (100 k Ω PD)	R _{PD_100K}	V _{in} =0V	_	1	μA
Keeper Circuit Resistance	R _{keep}		105	165	kΩ
Input current (no pull-up/down)	l _{in}	$V_{I} = 0, VI = OVDD$	-2.9	2.9	μA

Table 23. RGMII I/O 2.5V I/O DC Electrical Parameters¹

Input Mode Selection: SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 10 (1.8V Mode) SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 11 (2.5V Mode)

² Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled (register IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC[HYS]= 0).

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 28 and Table 29, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	2.72/2.79 1.51/1.54	
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	3.20/3.36 1.96/2.07	ne
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	3.64/3.88 2.27/2.53	115
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	4.32/4.50 3.16/3.17	
Input Transition Times ¹	trm	_		_	25	ns

Table 28. General Purpose I/O AC Parameters 1.8 V Mode

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 29. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	1.70/1.79 1.06/1.15	
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	2.35/2.43 1.74/1.77	ns
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	_	_	5.14/5.57 4.77/5.15	
Input Transition Times ¹	trm	_	_		25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Electrical Characteristics



Figure 9. Impedance Matching Load for Measurement

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported DDR3/DDR3L/LPDDR2 Configurations."

Table 36 shows DDR I/O output buffer impedance of i.MX 6DualPlus/6QuadPlus processors.

			Тур	ical	
Parameter	Symbol	Test Conditions	NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	Unit
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Table 36. DDR I/O Output Buffer Impedance

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

2. Calibration is done against 240 W external reference resistor.

3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

4.8.4 MLB 6-Pin I/O Differential Output Impedance

Table 37 shows MLB 6-pin I/O differential output impedance of i.MX 6DualPlus/6QuadPlus processors.

Table 37. MLB 6-Pin I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Тур	Мах	Unit
Differential Output Impedance	ZO	—	1.6	_	—	kΩ

ID	Parameter	Min ¹	Max ¹	Unit
WE4	Clock rise to address valid	-0.5×t×(k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5×t×(k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5×t×(k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE9	Clock rise to EIM_WE_B invalid	0.5×t×(k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE11	Clock rise to EIM_OE_B invalid	0.5×t×(k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	$-0.5 \times t \times (k+1) + 2.25$	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	$0.5 \times t \times (k+1) + 2.25$	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

Table 41. EIM Bus	Timing	Parameters	(continued)
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k represents register setting BCD value.
 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.



Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

Figure 14. Synchronous Memory Read Access, WSC=1



Figure 15. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

Table 42. EIM Asynchronou	Timing Parameters Relative to	Chip Select ^{1, 2} (continued)
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Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Мах	Unit
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7-WE15-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14-WE6+(ADVN+ADVA+1- CSA)×t	-3.5+(ADVN+AD VA+1-CSA)×t	3.5+(ADVN+ADVA +1-CSA)×t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16-WE6-WCSA×t	-3.5-WCSA×t	3.5-WCSA×t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16-WE6+(WADVN+WADVA +ADH+1-WCSA)×t	-3.5+(WADVN+ WADVA +ADH+1-WCSA) ×t	3.5+(WADVN+WADVA +ADH+1-WCSA)×t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17-WE7-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	_	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	_	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	_	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCS O+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	_	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WC SA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WC SN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	_	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCS O+MAXDTI		ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	_	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 24 through Figure 27 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 44 describes the timing parameters (NF1–NF17) that are shown in the figures.



Figure 24. Command Latch Cycle Timing Diagram



Figure 25. Address Latch Cycle Timing Diagram











Figure 28. Read Data Latch Cycle Timing Diagram (EDO Mode)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Мах	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T -	· 0.12 [see ^{2,3}]	ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.	72 [see ²]	ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1)	×T [see ^{3,2}]	ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T	- 1 [see ²]	ns
NF5	NAND_WE_B pulse width	tWP	$DS \times T$ [see ²]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see ^{3,2}]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see ²]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see ²]		ns
NF9	Data hold time	tDH	DH × T - 1.	37 [see ²]	ns
NF10	Write cycle time	tWC	(DS + DH) :	× T [see ²]	ns
NF11	NAND_WE_B hold time	tWH	DH × T [see ²]		ns
NF12	Ready to NAND_RE_B low	tRR ⁴	$(AS + 2) \times T [see ^{3,2}]$	_	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see ²]		ns
NF14	READ cycle time	tRC	$(DS + DH) \times T [see 2]$		ns
NF15	NAND_RE_B high hold time	tREH	DH imes T	[see ²]	ns

Table 44.	Asynchronous	Mode	Timing	Parameters ¹
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4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 39 depicts the timing of SD/eMMC4.3, and Table 50 lists the SD/eMMC4.3 timing characteristics.



Figure 39. SD/eMMC4.3 Timing

ID	Parameter	Symbols	Min	Max	Unit				
	Card Input Clock								
SD1	Clock Frequency (Low Speed)	f _{PP} ¹	0	400	kHz				
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f _{PP} ²	0	25/50	MHz				
	Clock Frequency (MMC Full Speed/High Speed)	f _{PP} ³	0	20/52	MHz				
	Clock Frequency (Identification Mode)	f _{OD}	100	400	kHz				
SD2	Clock Low Time	t _{WL}	7	—	ns				
SD3	Clock High Time	t _{WH}	7	—	ns				
SD4	Clock Rise Time	t _{TLH}	—	3	ns				
SD5	Clock Fall Time	t _{THL}	—	3	ns				
	eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)								
SD6	eSDHC Output Delay	t _{OD}	-6.6	3.6	ns				



Figure 53. TMDS Clock Signal Definitions



Figure 54. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1



Figure 55. Intra-Pair Skew Definition

п	Parameter	Standa	ard Mode	Fast Mode		Unit
	Falameter	Min	Мах	Min	Max	Onne
IC9	Bus free time between a STOP and START condition	4.7	—	1.3		μs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	_	1000	$20 + 0.1 C_b^4$	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1 C_b^4$	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

Table 61. I²C Module Timing Parameters (continued)

¹ A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

³ A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

⁴ $C_b = total capacitance of one bus line in pF.$

4.12.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

Figure 65 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 66 lists the synchronous display interface timing characteristics.



Figure 65. Synchronous Display Interface Timing Diagram—Access Level

ID	Parameter	Symbol	Min	Typ ¹	Мах	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd ² -Tdicu ³	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	_	ns

Table 66. Synchronou	s Display Interface	Timing Characteristics	(Access Level)
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¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

² Display interface clock down time

$$Tdicd = \frac{1}{2} \left(T_{diclk} \times ceil \left[\frac{2 \times DISP_{CLK} DOWN}{DI_{CLK} PERIOD} \right] \right)$$

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$\Gamma \text{dicu} = \frac{1}{2} \left(T_{\text{diclk}} \times \text{ceil} \left[\frac{2 \times \text{DISP} \text{-} \text{CLK} \text{-} \text{UP}}{\text{DI} \text{-} \text{CLK} \text{-} \text{PERIOD}} \right] \right)$$



Figure 86. Test Access Port Timing Diagram

Output Data Valid

i.MX 6DualPlus/6QuadPlus Automotive Applications Processors, Rev. 2, 09/2017

(Output)

Package Information and Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output— requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

6.2.3 21 x 21 mm Functional Contact Assignments

Table 96 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

					Out of Reset Con	dition ¹	
Ball Name	Ball	Power Group	Ball Type	Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—		CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	_		CLK1_P		_
CLK2_N	C5	VDD_HIGH_CAP	—		CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—		CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—		CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—		CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—		CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	_	CSI_DATA0_P	—	
CSI_D1M	D1	NVCC_MIPI	_	_	CSI_DATA1_N		_

Table 96. 21 x 21 mm Functional Contact Assignments