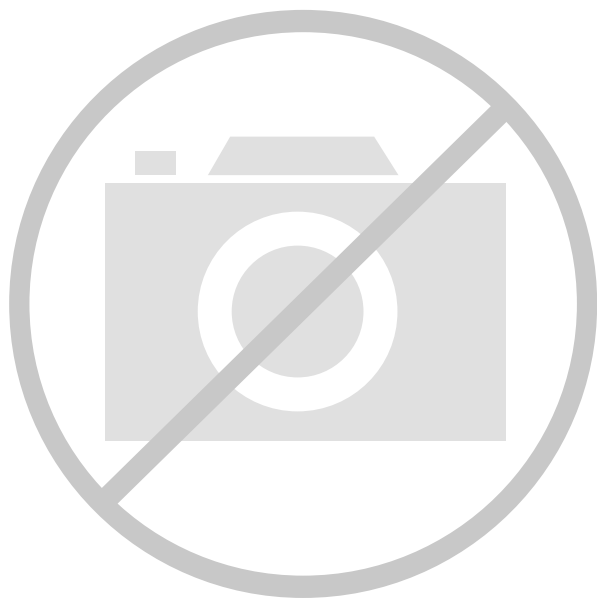




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

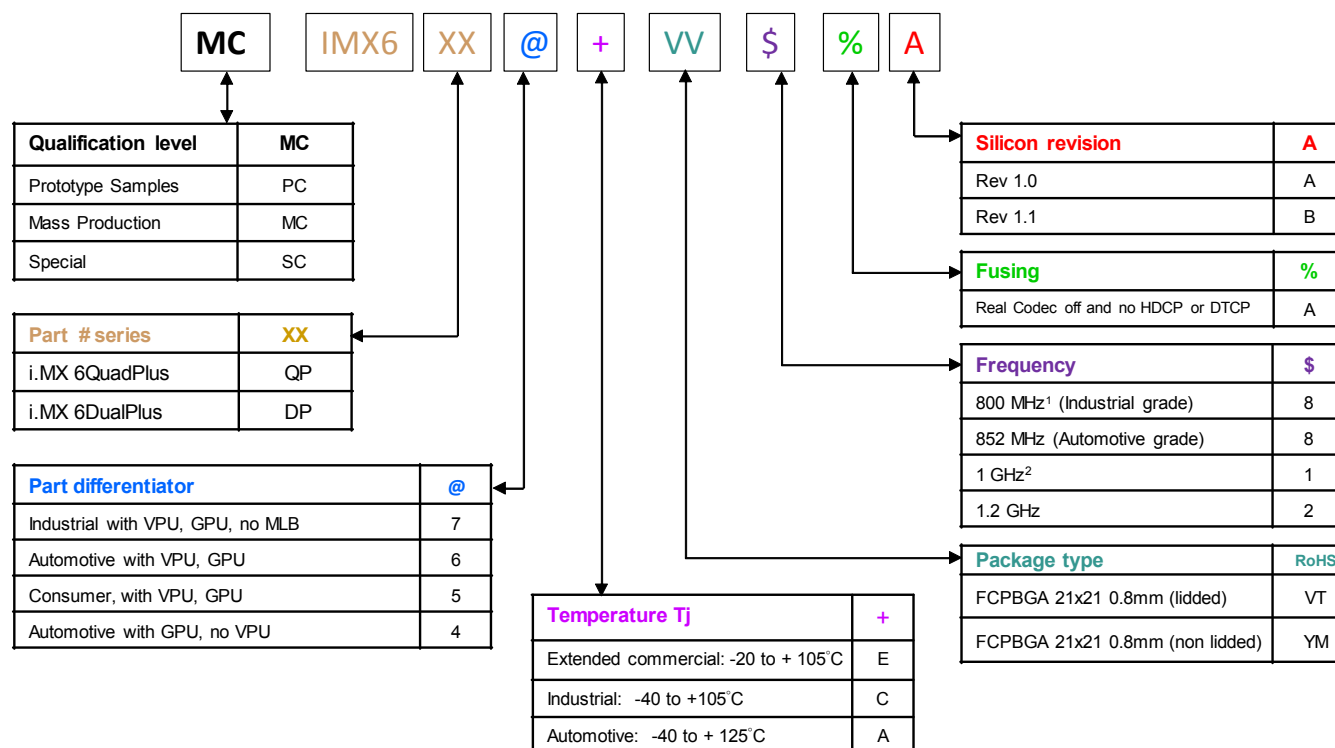
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6qp6avt1aar

Introduction

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6DualPlus/6QuadPlus Automotive Applications Processors data sheet (IMX6DQPAEC) covers parts listed for the “Plus” series and with “A” indicating automotive temperature.
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Consumer Products data sheet (IMX6DQPCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Industrial Products data sheet (IMX6DQPIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the fields: Part # Series (DP/QP), temperature grade (junction) (A), and Frequency (8).



1. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.

2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualPlus and i.MX 6QuadPlus

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6DualPlus/6QuadPlus processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6DualPlus/6QuadPlus processor system.

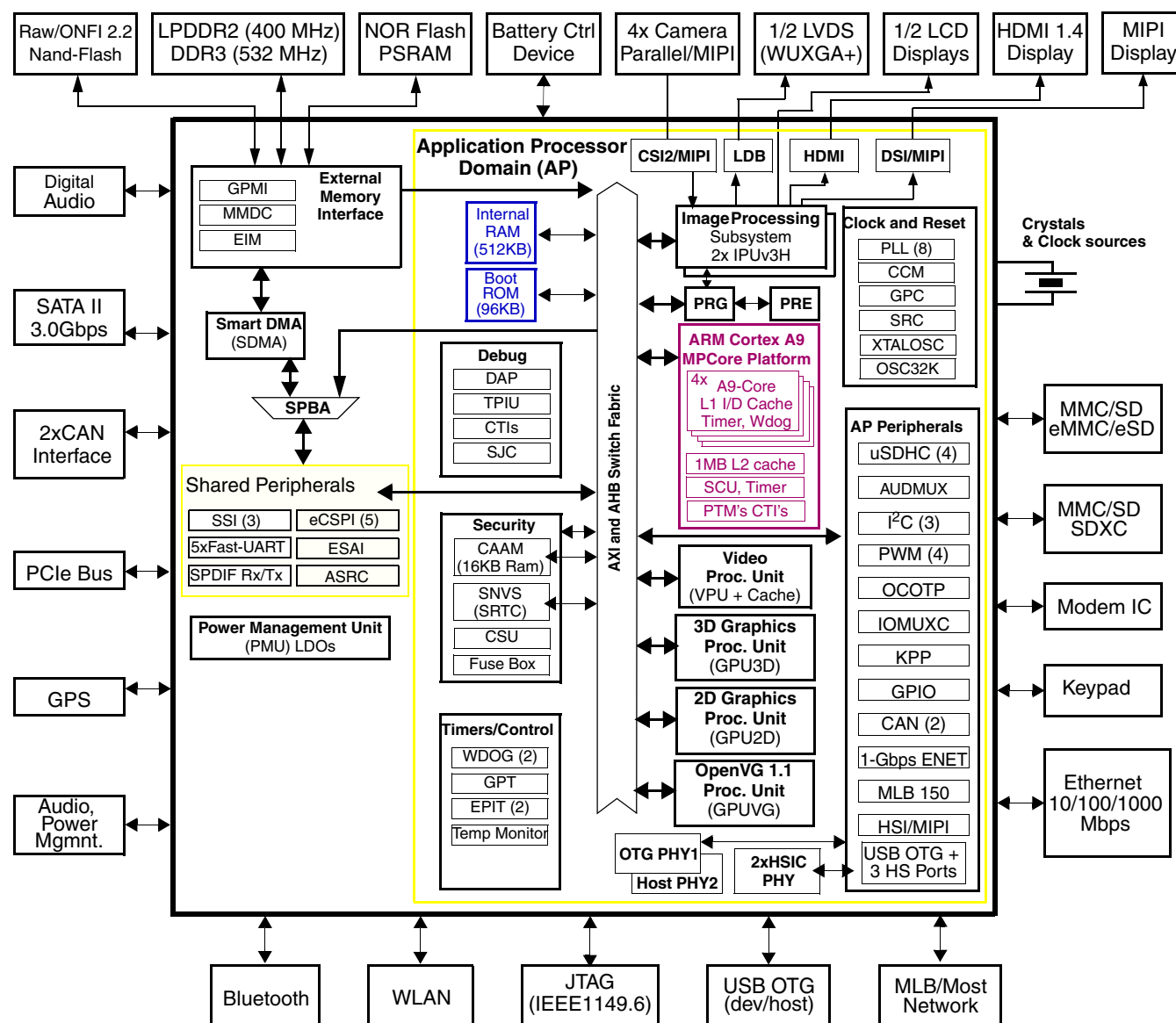


Figure 2. i.MX 6DualPlus/6QuadPlus Automotive Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6DualPlus/6QuadPlus processors contain a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX 6DualPlus/6QuadPlus Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512 x 8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6DualPlus/6QuadPlus processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPIM2 operation.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC error correction for NAND Flash controller (GPMI).
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6DualPlus/6QuadPlus processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in [Section 6, “Package Information and Contact Assignments.”](#) Signal descriptions are defined in the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, “Unused analog interfaces,” of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment ²
GPIO supplies ¹⁰	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5 ¹¹ NVCC_MIP1	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature	T _J	-40	95	125	°C	See <i>i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note</i> , AN4724, for information on product lifetime (power-on years) for this processor.

¹ Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

² See the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

³ For Quad core system, connect to VDD_ARM_IN. For Dual core system, may be shorted to GND together with VDD_ARM23_CAP to reduce leakage.

⁴ VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation

⁵ VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

⁶ VDD_SOC_CAP and VDD_PU_CAP must be equal.

⁷ In LDO enabled mode, the internal LDO output set points must be configured such that the:

VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.

VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

⁸ In LDO bypassed mode, the external power supply must ensure that VDD_ARM_IN does not exceed VDD_SOC_IN by more than 100 mV. The VDD_ARM_IN supply voltage can be lower than the VDD_SOC_IN supply voltage. The minimum voltages shown in this table must be maintained.

⁹ To set VDD_SNVS_IN voltage with respect to Charging Currents and RTC, see the *Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors* (IMX6DQ6SDLHDG).

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

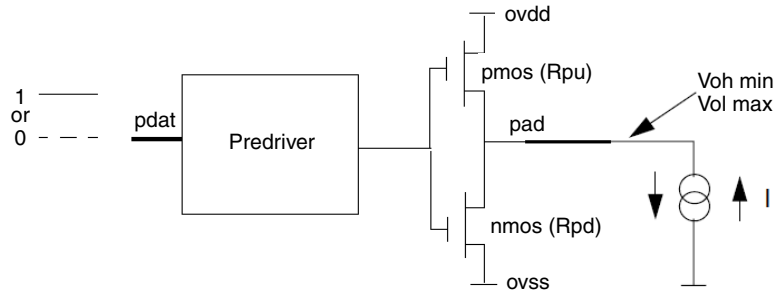


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

Table 21. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 ^(See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C _{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	I _{XTALI_STARTUP}	Power-on startup for 0.15 msec with a driven 32 KHz RTC clock @ 1.1 V. ²	—	—	600	μA
DC input current	I _{XTALI_DC}	—	—	—	2.5	μA

¹ This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

² This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

4.6.4 RGMII I/O 2.5V I/O DC Electrical Parameters

The RGMII interface complies with the RGMII standard version 1.3. The parameters in Table 23 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 23. RGMII I/O 2.5V I/O DC Electrical Parameters¹

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage ¹	V _{OH}	I _{oh} = -0.1 mA (DSE=001,010) I _{oh} = -1.0 mA (DSE=011,100,101,110,111)	OVDD-0.15	—	V
Low-level output voltage ¹	V _{OL}	I _{ol} = 0.1 mA (DSE=001,010) I _{ol} = 1.0 mA (DSE=011,100,101,110,111)	—	0.15	V
Input Reference Voltage	V _{ref}	—	0.49xOVDD	0.51xOVDD	V
High-Level input voltage ^{2, 3}	V _{IH}	—	0.7xOVDD	OVDD	V
Low-Level input voltage ^{2, 3}	V _{IL}	—	0	0.3xOVDD	V
Input Hysteresis(OVDD=1.8V)	V _{HYS_HighVDD}	OVDD=1.8V	250	—	mV
Input Hysteresis(OVDD=2.5V)	V _{HYS_HighVDD}	OVDD=2.5V	250	—	mV
Schmitt trigger VT+ ^{3, 4}	V _{TH+}	—	0.5xOVDD	—	mV
Schmitt trigger VT- ^{3, 4}	V _{TH-}	—	—	0.5xOVDD	mV
Pull-up resistor (22 kΩ PU)	R _{PU_22K}	V _{in} =0V	—	212	μA
Pull-up resistor (22 kΩ PU)	R _{PU_22K}	V _{in} =OVDD	—	1	μA
Pull-up resistor (47 kΩ PU)	R _{PU_47K}	V _{in} =0V	—	100	μA
Pull-up resistor (47 kΩ PU)	R _{PU_47K}	V _{in} =OVDD	—	1	μA
Pull-up resistor (100 kΩ PU)	R _{PU_100K}	V _{in} =0V	—	48	μA
Pull-up resistor (100 kΩ PU)	R _{PU_100K}	V _{in} =OVDD	—	1	μA
Pull-down resistor (100 kΩ PD)	R _{PD_100K}	V _{in} =OVDD	—	48	μA
Pull-down resistor (100 kΩ PD)	R _{PD_100K}	V _{in} =0V	—	1	μA
Keeper Circuit Resistance	R _{keep}	—	105	165	kΩ
Input current (no pull-up/down)	I _{in}	V _I = 0, V _I = OVDD	-2.9	2.9	μA

¹ Input Mode Selection: SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 10 (1.8V Mode)
SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 11 (2.5V Mode)

² Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{il} or V_{ih}. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled (register IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC[HYS]= 0).

Table 27. MLB I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	$R_{load} = 50\ \Omega$ between padP and padN	300	500	mV
Output High Voltage	V_{OH}		1.15	1.75	V
Output Low Voltage	V_{OL}		0.75	1.35	V
Common-mode Output Voltage ((Vpad_P + Vpad_N) / 2))	V_{OCM}		1	1.5	V
Differential Output Impedance	Z_O	—	1.6	—	k Ω

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in [Figure 4](#) and [Figure 5](#).

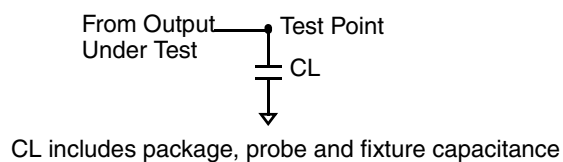


Figure 4. Load Circuit for Output

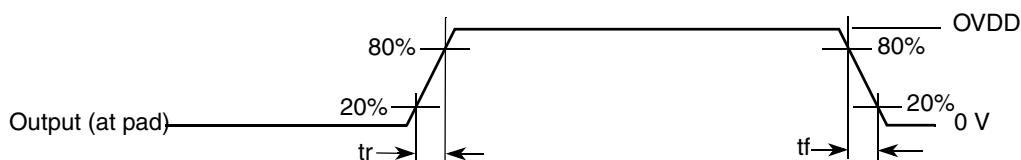


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the [Table 28](#) and [Table 29](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 28. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 29. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive, DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

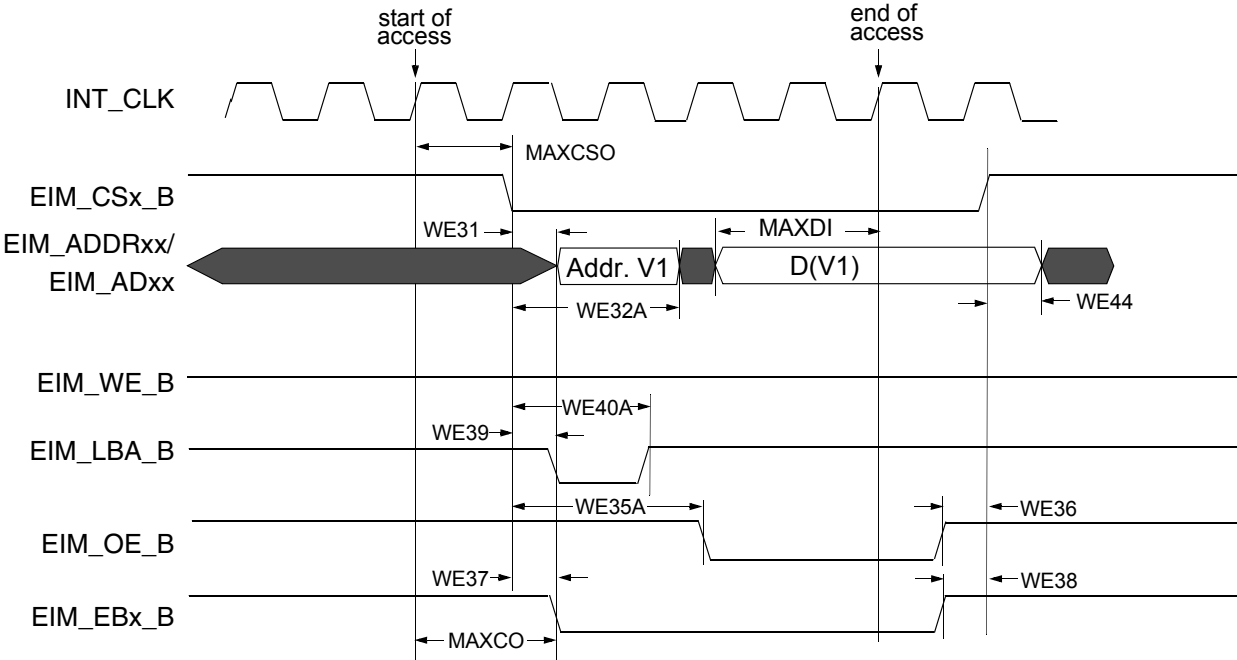


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

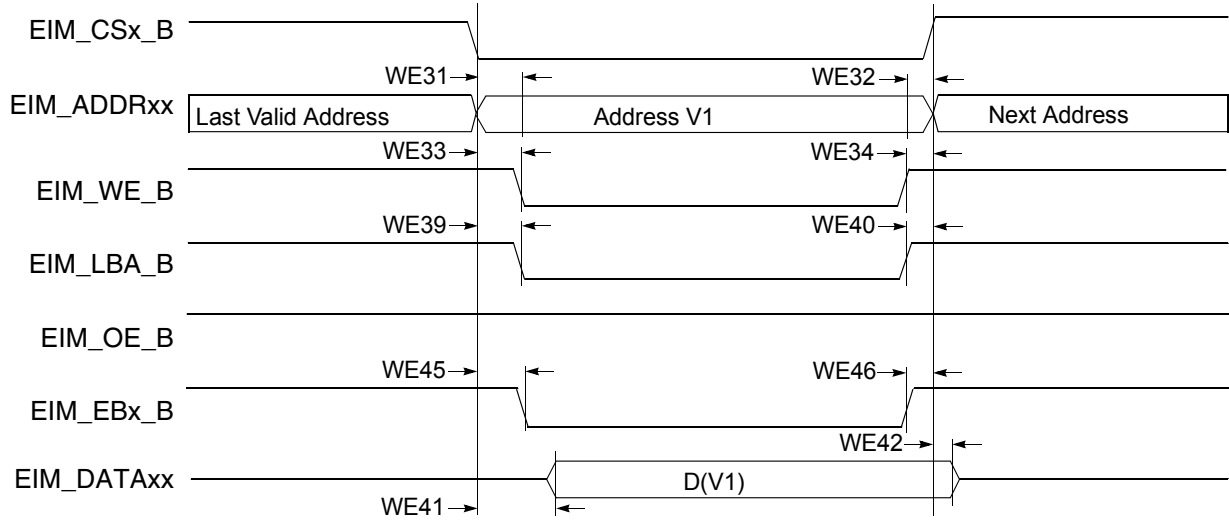


Figure 20. Asynchronous Memory Write Access

4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 24 through Figure 27 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 44 describes the timing parameters (NF1–NF17) that are shown in the figures.

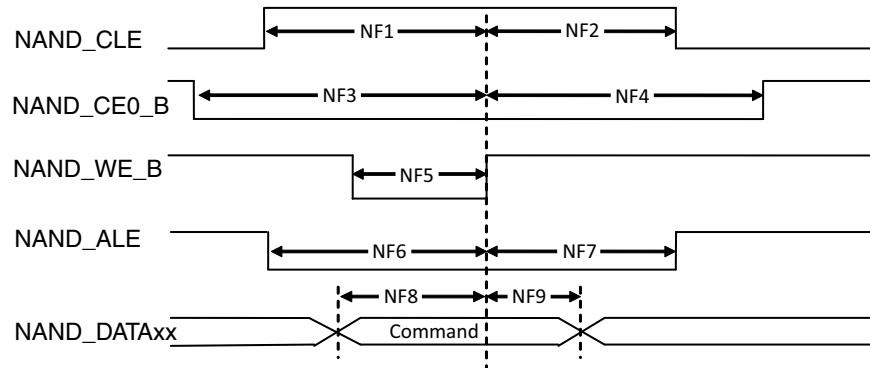


Figure 24. Command Latch Cycle Timing Diagram

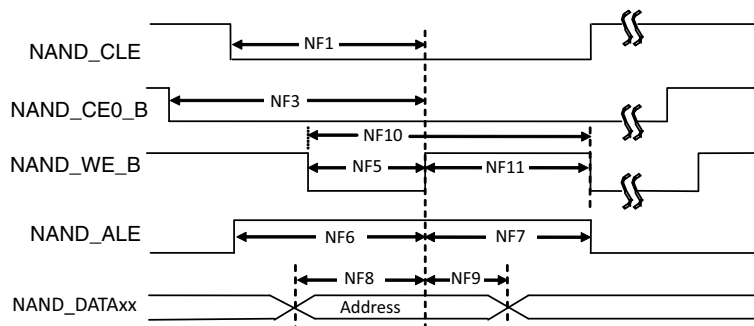


Figure 25. Address Latch Cycle Timing Diagram

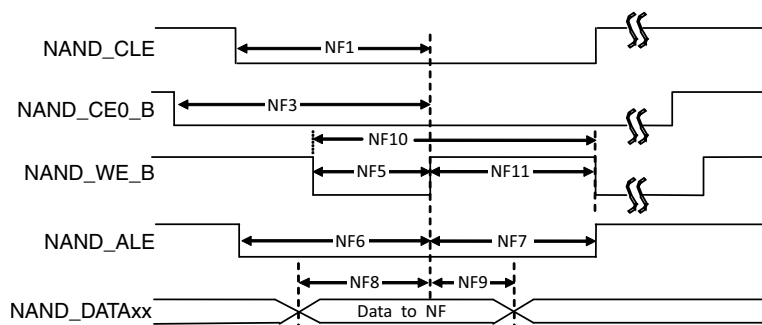


Figure 26. Write Data Latch Cycle Timing Diagram

Table 44. Asynchronous Mode Timing Parameters¹ (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	$(DS \times T - 0.67)/18.38$ [see ^{5,6}]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see ^{5,6}]	—	ns

¹ The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

² AS minimum value can be 0, while DS/DH minimum value is 1.

³ T = GPMI clock period -0.075ns (half of maximum p-p jitter).

⁴ NF12 is met automatically by the design.

⁵ Non-EDO mode.

⁶ EDO mode, GPMI clock $\approx$ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 28), NF16/NF17 are different from the definition in non-EDO mode (Figure 27). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM)). The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

Table 60. Switching Characteristics (continued)

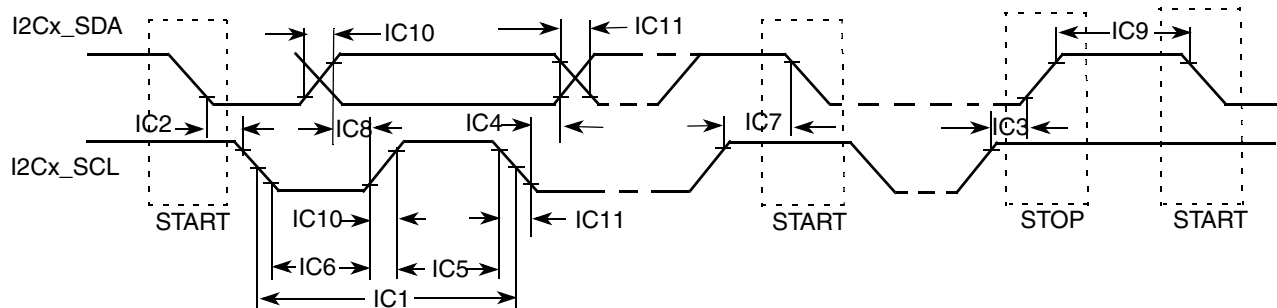
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	Differential output signal fall time	20–80% RL = 50 Ω See Figure 57.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to $2 \times V_{SWING}$	—	—	15	%
—	Differential signal undershoot	Referred to $2 \times V_{SWING}$	—	—	25	%
Data and Control Interface Specifications						
$t_{Power-up}^2$	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	—	—	3.35	ms

¹ Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

² For information about latencies and associated timings, see Section 4.12.7.1, “Latencies and Timing Information.”

4.12.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 58 depicts the timing of I²C module, and Table 61 lists the I²C module timing characteristics.

Figure 58. I²C Bus TimingTable 61. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	μ s
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μ s
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μ s
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μ s
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	μ s
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	μ s
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μ s
IC8	Data set-up time	250	—	100 ³	—	ns

Table 64. Video Signal Cross-Reference (continued)

i.MX 6DualPlus/6QuadPlus	LCD							Comment ^{1,2}
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ³	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_Dlx_DISP_CLK	PixCLK							—
IPUx_Dlx_PIN01	—							May be required for anti-tearing
IPUx_Dlx_PIN02	HSYNC							—
IPUx_Dlx_PIN03	VSYNC							VSYNC out

Table 75. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLB_SIG_P/_N (MLB_DATA_P/_N) output valid from transition of MLB_CLK_P/_N (low-to-high) ¹	t_{delay}	0.6	1.3	ns	—
Disable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{phz}	0.6	3.5	ns	—
Enable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{plz}	0.6	5.6	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) valid to transition of MLB_CLK_P/_N (low-to-high)	t_{su}	0.05	—	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) hold from transition of MLB_CLK_P/_N (low-to-high) ²	t_{hd}	0.6	—	ns	—

¹ t_{delay} , t_{phz} , t_{plz} , t_{su} , and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

² The transmitting device must ensure valid data on MLB_SIG_P/_N (MLB_DATA_P/_N) for at least $t_{\text{hd}(\text{min})}$ following the rising edge of MLBCLKP/N; receivers must latch MLB_SIG_P/_N (MLB_DATA_P/_N) data within $t_{\text{hd}(\text{min})}$ of the rising edge of MLBCLKP/_N.

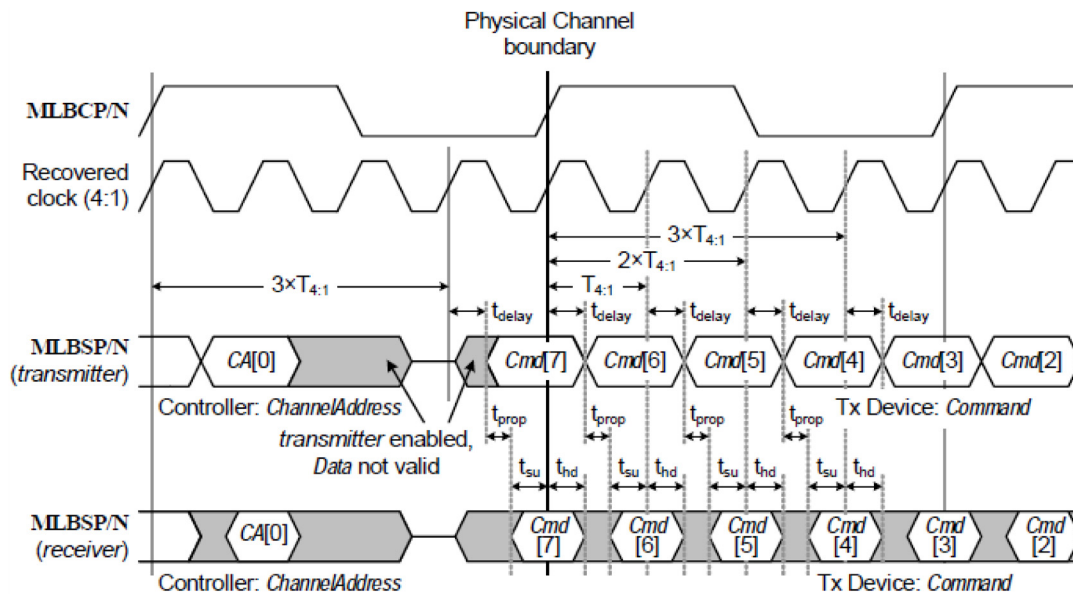


Figure 82. MLB 6-Pin Delay, Setup, and Hold Times

4.12.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	PU (100K)
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	PU (100K)
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	PU (100K)
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	PU (100K)
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	PU (100K)
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	PU (100K)
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100K)
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	PU (100K)
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	PU (100K)
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	PU (100K)
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	PU (100K)
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	PU (100K)
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	PU (100K)
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	PU (100K)
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	PU (100K)
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	PU (100K)
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	PU (100K)
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100K)
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	PU (100K)
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	PU (100K)
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	PU (100K)
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	PU (100K)
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100K)
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100K)
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100K)
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	0
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	0
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	0

6.2.5 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 98 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map

G	F	E	D	C	B	A	
DSI_D0P	CSI_D3P	CSI_D2M	CSI_D1M	GND	PCIE_RXM		1
DSI_D0M	CSI_D3M	CSI_D2P	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND	GND	4
JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN	USB_OTG_DP	6
PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO	XTALI	7
PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B	GND	8
VDD_SNV5_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
VDD_SNV5_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
SATA_VPH	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	SATA_TXM	SATA_TXP	12
SATA_VP	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	SATA_REXT	SATA_RXP	SATA_RXM	14
NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC	GND	25

7 Revision History

Table 99 provides a revision history for this i.MX 6DualPlus/6QuadPlus data sheet.

Table 99. i.MX 6DualPlus/6QuadPlus Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
2	09/2017	Rev. 2 changes include the following: • Changed throughout: terminology from “floating” to “not connected”. • Figure 1, “Part Number Nomenclature—i.MX 6DualPlus and i.MX 6QuadPlus,” on page 4: Corrected Automotive grade frequency from 850 to 852 MHz. • Section 1.2, “Features” on page 5: Changed Internal/external peripheral item from “LVDS serial ports—One port up to 165 MPixels/sec...” to: “...—One port up to 170 MPixels/sec...”. • Table 4, “Absolute Maximum Ratings,” on page 21: Multiple changes: – Core supply voltages: Separated rows by LDO enabled and LDO bypass. – Renamed Internal supply voltages to Core supply output voltage (LDO enabled) and changed maximum value from 1.3 to 1.4V. Added symbol NVCC_PLL_OUT. – Reordered VDD_HIGH_IN row and changed maximum value from 3.6 to 3.7V. – DDR I/O supply voltage: added symbol, NVCC_DRAM, and footnote. – GPIO I/O supply voltage: Added symbols. Changed maximum value from 3.6 to 3.7V. – Added HDMI, PCIe, and SATA PHY (VPH and VP) supply voltage rows and values. – Consolidated LVDS, MLB, and MIPI I/O supply voltage rows. Added symbols. – Added rows: PCIe PHY, RGMII I/O, and SMVS IN supply voltages, symbols, and values. – USB I/O supply voltage: moved symbols from parameters to symbol column. Changed maximum value from 3.63 to 3.73V. Added symbol USB_OTG_CHD_B – USB VBUS supply voltage: Changed maximum value from 5.25 to 5.35V. – Separated V_{in}/V_{out} input/output voltage range distinguishing between non-DDR and DDR pins. Changed maximum value for V_{in}/V_{out} input/output voltage range DDR pins to OVDD+0.4. Added footnotes to both maximum values. – Separated ESD immunity by HBM and CDM. Expanded symbols for each. • Section 4.1.2, “Thermal Resistance” on page 22: Added NOTE: “Per JEDEC JESD51-2, the intent of thermal resistance measurements...”. • Table 5, “FCPBGA Package Thermal Resistance Data (Lidded),” on page 22: Added Lidded Table. • Section 4.2.1, “Power-Up Sequence” on page 33: – Removed inference to internal POR. • Section 4.5.2, “OSC32K” on page 37: Removed content about calculating the proper current limiting resistor for a coin cell. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” on page 39: Added “NOTE: The V_{il} and V_{ih} specifications only apply when an external clock source is used...”. • Table 21, “XTALI and RTC_XTALI DC Parameters,” on page 39: Added footnote to RTC_XTALI high level DC input voltage row: “This voltage specification must not be exceeded and ...”. <i>(Revision History table continued on next page.)</i>

Table 99. i.MX 6DualPlus/6QuadPlus Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2 (Cont.)	09/2017	• Section 4.6.4, “RGMII I/O 2.5V I/O DC Electrical Parameters” on page 41: Added section and table. • Section 4.10, “Multi-Mode DDR Controller (MMDC)” on page 64: Replaced section with new content. Was 4.9.4 “<i>DDR SDRAM Specific Parameters (DDR3/DDR3L/LPDDR2)</i>” with timing diagrams and parameter tables for DDR. • Table 51, “eMMC4.4/4.41 Interface Timing Specification,” on page 81: – Corrected SD3, uSDHC Input Setup Time, minimum value from 2.6ns to 1.7ns. – Added footnote to Card Input Clock regarding duty cycle range. • Table 52, “SDR50/SDR104 Interface Timing Specification,” on page 82: Changes to Min/Max values: – SD2 min from: 0.3 x tCLK; to: 0.46 x tCLK – SD2 max from: 0.7 x tCLK to: 0.54 x tCLK – SD3 min from: 0.3 x tCLK; to: 0.46 x tCLK. Also corrected ID from duplicate SD2 to SD3. – SD3 max from: 0.7 x tCLK; to: 0.54 x tCLK – SD5 max from: 1 ns; to: 0.74 ns • Table 62, “Camera Input Signal Cross Reference, Format, and Bits Per Cycle,” on page 95: Changed RGB565, 16 bits column heading from 2 cycles to 1 cycle. • Table 95, “21 x 21 mm Supplies Contact Assignment,” on page 144: – Added description to ZQPAD. – Added description to GPANAIO row: “...output for NXP use only...” • Table 96, “21 x 21 mm Functional Contact Assignments,” on page 146: – Changed DRAM_SDCLK_0, DRAM_SDCLK_1 from “<i>Input–Hi-Z</i>” to “<i>Output–0</i>”. • Section 6.2.1.1, “21 x 21 mm Lidded Package” on page 142: Added section.
1	3/2016	Revision 1 changes are within Table 20, “Maximum Supply Currents” on page 48 Changed: • VDD-ARM_IN with condition 996 MHz, CoreMark maximum current value from 1500 to 1200 • VDD-ARM_IN with condition 852 MHz, CoreMark maximum current value from 1360 to 1090 • Added footnote regarding values are assumed when VDD_ARM23_IN and VDD_ARM23_CAP are connected to ground.