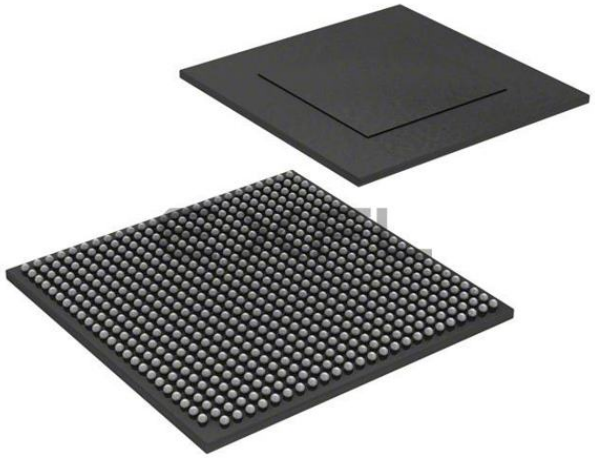

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6qp6avt1ab

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6DualPlus/6QuadPlus platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6DualPlus/6QuadPlus processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6DualPlus/6QuadPlus processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM). **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP NVCC_PLL_OUT	-0.3	1.4	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI, PCIe, and SATA PHY high (VPH) supply voltage	HDMI_VPH PCIE_VPH SATA_VPH	-0.3	2.85	V
HDMI, PCIe, and SATA PHY low (VP) supply voltage	HDMI_VP PCIE_VP SATA_VP	-0.3	1.4	V
LVDS, MLB, and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMII I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V
V_{in}/V_{out} input/output voltage range (non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.3 (See note 2)	V
V_{in}/V_{out} input/output voltage range (DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.4 (See notes1&2)	V
ESD immunity (HBM)	V_{esd_HBM}	—	2000	V
ESD immunity (CDM)	V_{esd_CDM}	—	500	V
Storage temperature range	$T_{storage}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 FCPBGA Package Thermal Resistance

Table 5 provides the FCPBGA package thermal resistance data for the *lidded* package type.

Table 5. FCPBGA Package Thermal Resistance Data (Lidded)

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2]	$R_{\theta JA}$	24	°C/W
	Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$	15	°C/W
Junction to Ambient[1]	Single-layer board (1s); air flow 200 ft/min[3]	$R_{\theta JMA}$	17	°C/W
	Four-layer board (2s2p); air flow 200 ft/min[4]	$R_{\theta JMA}$	12	°C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	5	°C/W
Junction to Case (top)[1,5]	—	$R_{\theta JCtop}$	1	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-3 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 8. Maximum Supply Currents (continued)

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
NVCC_LVDS2P5	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.		
MISC				
DRAM_VREF	—	1		mA

1 i.MX 6DualPlus numbers assume VDD_ARM23_IN and VDD_ARM23_CAP are connected to ground.

2 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

3 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

4 This is the maximum current per active USB physical interface.

5 The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

6 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6DualPlus/6QuadPlus processors in selected low power modes.

Table 9. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.4 V)	6	mA
		VDD_SOC_IN (1.4 V)	23	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW

Table 12. PCIe PHY Current Drain (continued)

Mode	Test Conditions	Supply	Max Current	Unit
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.10 HDMI Maximum Power Consumption

Table 13 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 13. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported DDR3/DDR3L/LPDDR2 Configurations."

Table 36 shows DDR I/O output buffer impedance of i.MX 6DualPlus/6QuadPlus processors.

Table 36. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

4.8.4 MLB 6-Pin I/O Differential Output Impedance

Table 37 shows MLB 6-pin I/O differential output impedance of i.MX 6DualPlus/6QuadPlus processors.

Table 37. MLB 6-Pin I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Z_O	—	1.6	—	—	kΩ

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 41 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

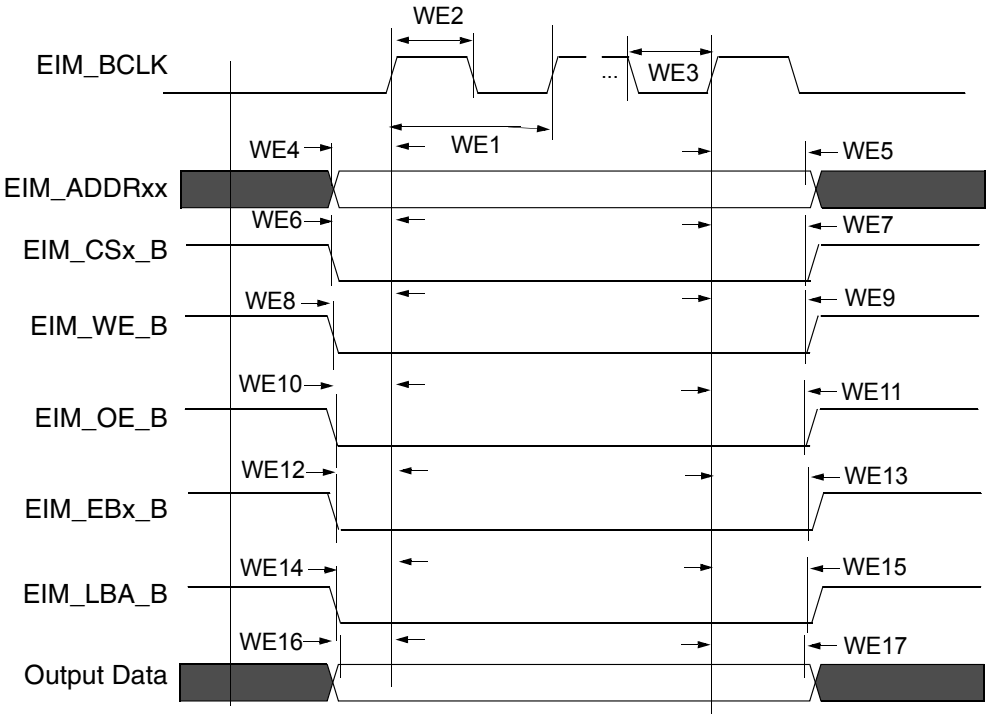


Figure 12. EIM Output Timing Diagram

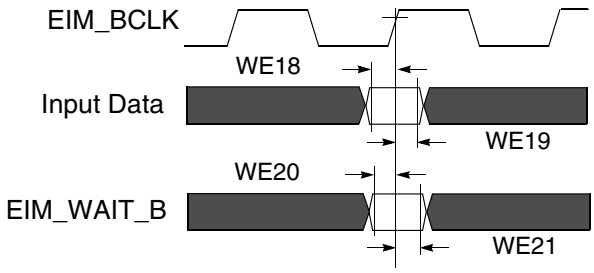


Figure 13. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 41. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns

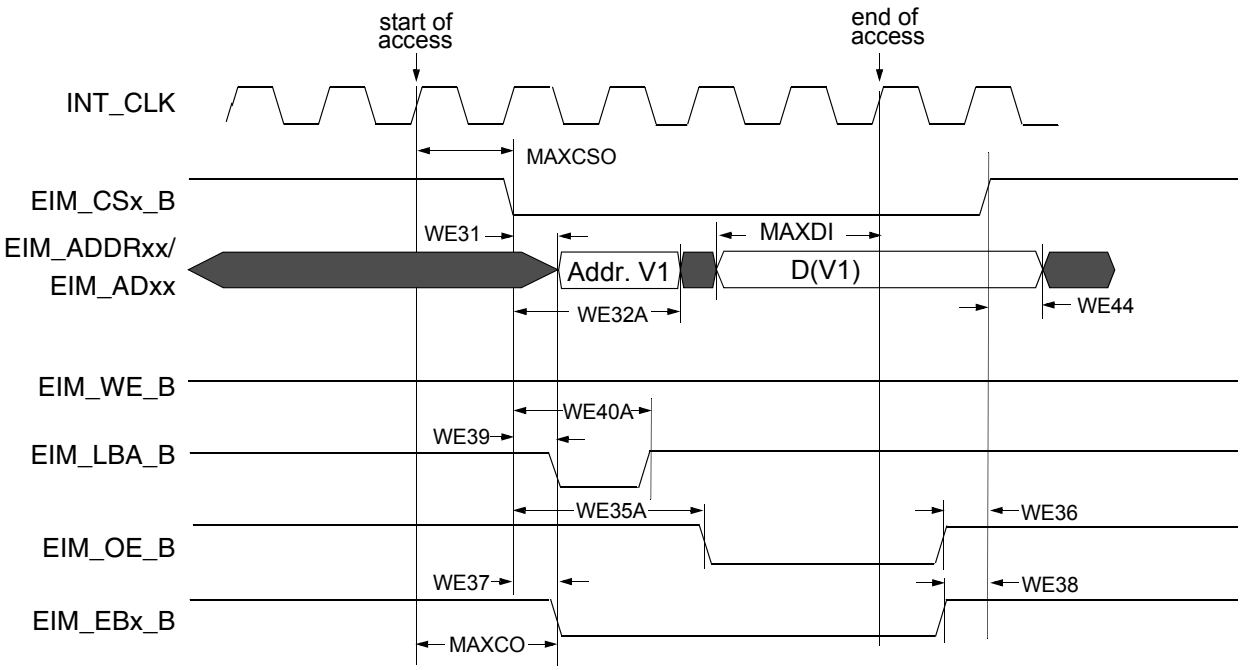


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

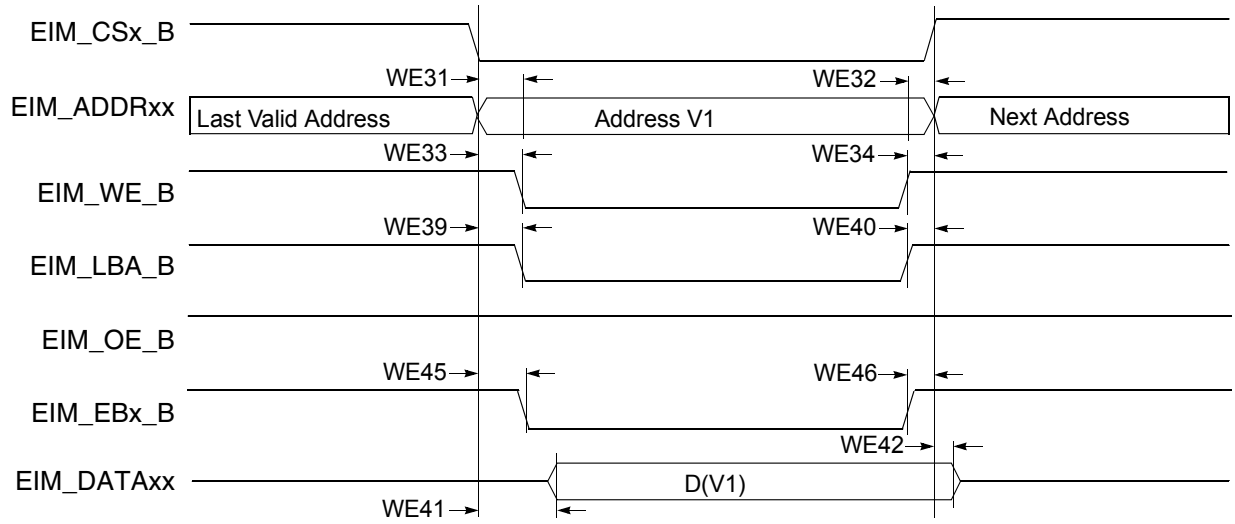


Figure 20. Asynchronous Memory Write Access

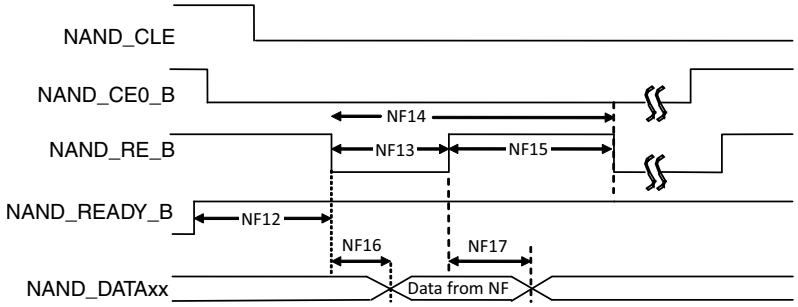


Figure 27. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

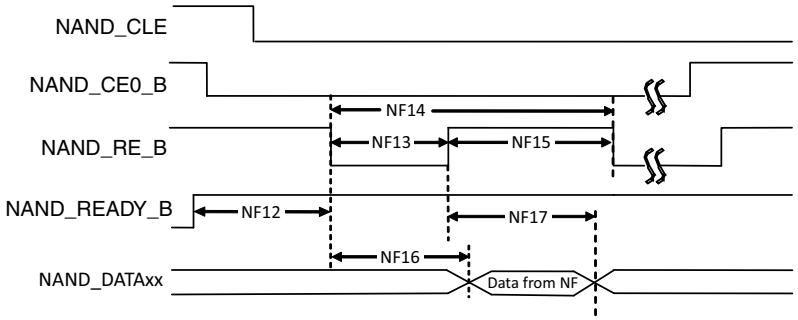


Figure 28. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 44. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see [3,2]]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see [2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see [2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see [2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see [2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see [2]]		ns

Table 46. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is met automatically by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 30.

7 Shown in Figure 31.

Figure 32 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For DDR Toggle mode, the typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM)). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 AUDMUX Timing Parameters

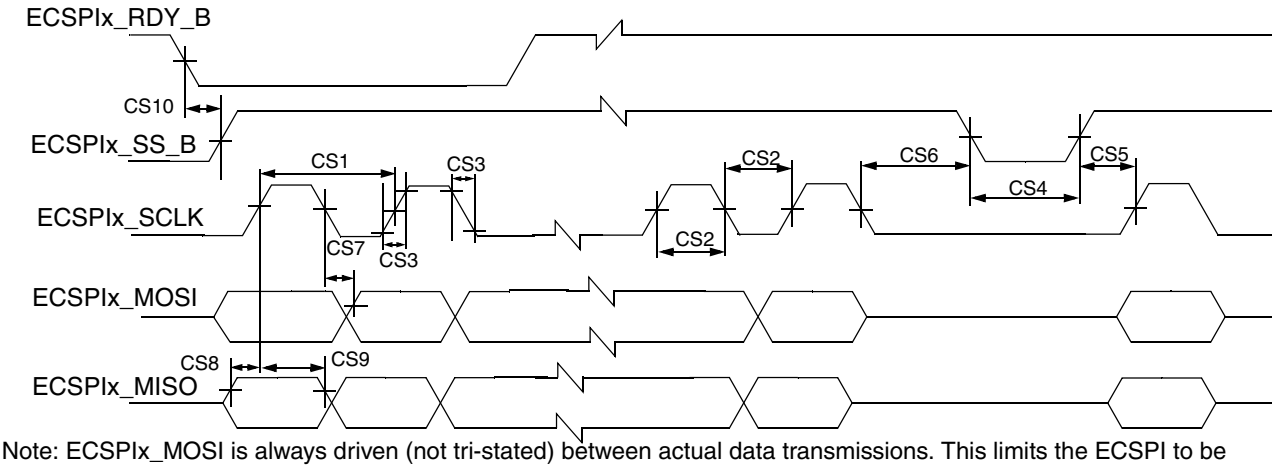
The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 35 depicts the timing of ECSPI in master mode and Table 47 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 35. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	 21.5 16	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow includes:

ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/ ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

2 ECSPI fast includes:

ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signalling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signalling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 22, “GPIO I/O DC Parameters,” on page 40.

4.12.5 Ethernet Controller (ENET) AC Electrical Specifications

4.12.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.12.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 42 shows MII receive signal timings. Table 53 describes the timing parameters (M1–M4) shown in the figure.

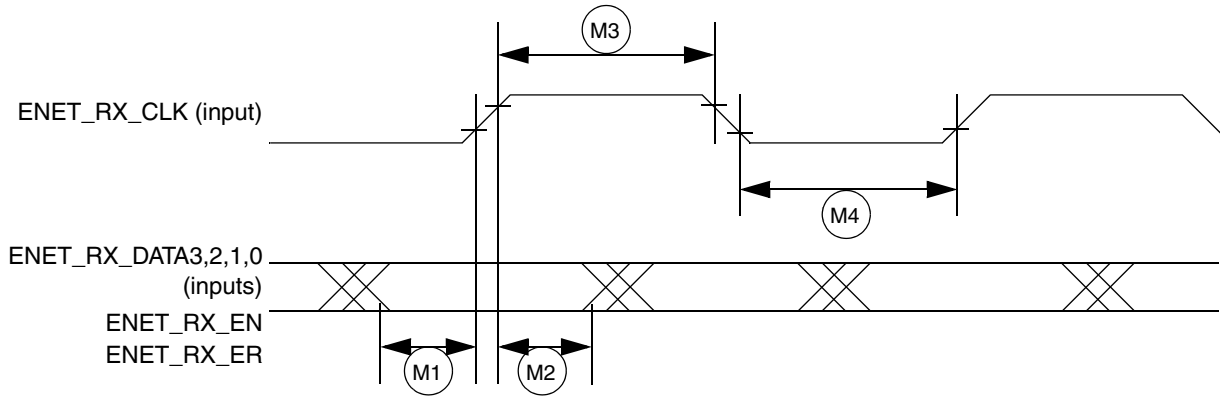


Figure 42. MII Receive Signal Timing Diagram

Table 53. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.12.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 62 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 62. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_ DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_ DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_ DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_ DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPU2_CSIx_ DATA_05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_ DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_ DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_ DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_ DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_ DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_ DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_ DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
IPUx_CSIx_ DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_ DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_ DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_ DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_ DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_ DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_ DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] IPU2_CSIx stands for IPU2_CSI1 or IPU2_CSI2.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

4.12.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.12.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.12.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

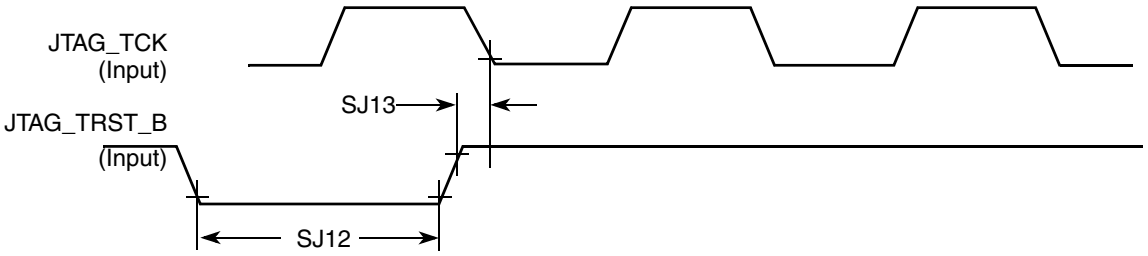


Figure 87. JTAG_TRST_B Timing Diagram

Table 79. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.12.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figure 88 and Figure 89 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.20.4 SSI Receiver Timing with External Clock

Figure 93 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

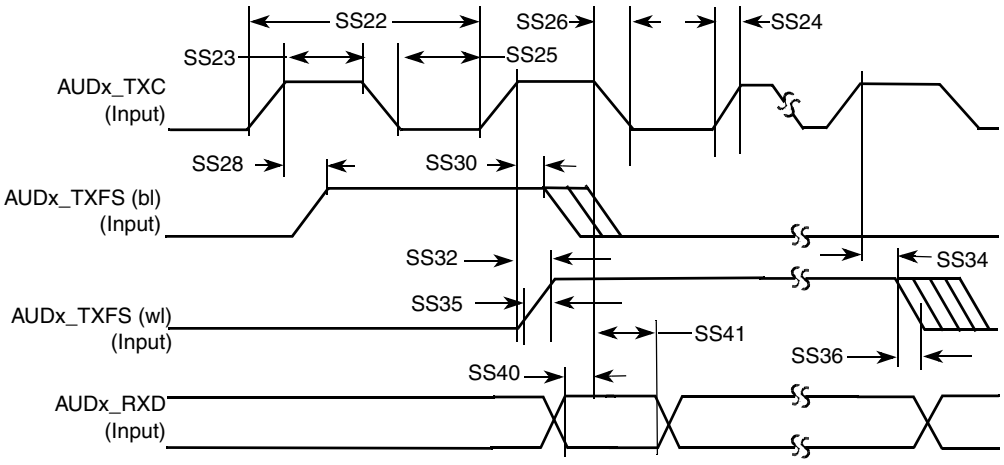


Figure 93. SSI Receiver External Clock Timing Diagram

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 21 x 21 mm Functional Contact Assignments

Table 96 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 96. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	—	—	CSI_DATA1_N	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	PU (100K)
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	PU (100K)
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	PU (100K)
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	PU (100K)
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	PU (100K)
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	PU (100K)
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100K)
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	PU (100K)
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	PU (100K)
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	PU (100K)
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	PU (100K)
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	PU (100K)
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	PU (100K)
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	PU (100K)
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	PU (100K)
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	PU (100K)
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	PU (100K)
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100K)
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	PU (100K)
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	PU (100K)
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	PU (100K)
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	PU (100K)
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100K)
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100K)
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100K)
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	0
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	0
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	0

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DSI_D1P	H1	NVCC_MIPI	—	—	DSI_DATA1_P	—	—
EIM_A16	H25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR16	Output	0
EIM_A17	G24	NVCC_EIM1	GPIO	ALT0	EIM_ADDR17	Output	0
EIM_A18	J22	NVCC_EIM1	GPIO	ALT0	EIM_ADDR18	Output	0
EIM_A19	G25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	H22	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	H23	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	F24	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	J21	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	F25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H19	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	N22	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	H24	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	J23	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	C25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100K)
EIM_D17	F21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100K)
EIM_D18	D24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100K)
EIM_D19	G21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100K)
EIM_D20	G20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100K)
EIM_D21	H20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100K)
EIM_D22	E23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PD (100K)
EIM_D23	D25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100K)
EIM_D24	F22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO24	Input	PU (100K)
EIM_D25	G22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO25	Input	PU (100K)
EIM_D26	E24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO26	Input	PU (100K)
EIM_D27	E25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO27	Input	PU (100K)
EIM_D28	G23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO28	Input	PU (100K)
EIM_D29	J19	NVCC_EIM0	GPIO	ALT5	GPIO3_IO29	Input	PU (100K)
EIM_D30	J20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO30	Input	PU (100K)
EIM_D31	H21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO31	Input	PD (100K)
EIM_DA0	L20	NVCC_EIM2	GPIO	ALT0	EIM_AD00	Input	PU (100K)
EIM_DA1	J25	NVCC_EIM2	GPIO	ALT0	EIM_AD01	Input	PU (100K)
EIM_DA2	L21	NVCC_EIM2	GPIO	ALT0	EIM_AD02	Input	PU (100K)
EIM_DA3	K24	NVCC_EIM2	GPIO	ALT0	EIM_AD03	Input	PU (100K)
EIM_DA4	L22	NVCC_EIM2	GPIO	ALT0	EIM_AD04	Input	PU (100K)
EIM_DA5	L23	NVCC_EIM2	GPIO	ALT0	EIM_AD05	Input	PU (100K)

Table 99. i.MX 6DualPlus/6QuadPlus Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2 *(Cont.)*	09/2017	• Section 4.6.4, "RGMII I/O 2.5V I/O DC Electrical Parameters" on page 41: Added section and table. • Section 4.10, "Multi-Mode DDR Controller (MMDC)" on page 64: Replaced section with new content. Was 4.9.4 "*DDR SDRAM Specific Parameters (DDR3/DDR3L/LPDDR2)*" with timing diagrams and parameter tables for DDR. • Table 51, "eMMC4.4/4.41 Interface Timing Specification," on page 81: – Corrected SD3, uSDHC Input Setup Time, minimum value from 2.6ns to 1.7ns. – Added footnote to Card Input Clock regarding duty cycle range. • Table 52, "SDR50/SDR104 Interface Timing Specification," on page 82: Changes to Min/Max values: – SD2 min from: 0.3 x tCLK; to: 0.46 x tCLK – SD2 max from: 0.7 x tCLK to: 0.54 x tCLK – SD3 min from: 0.3 x tCLK; to: 0.46 x tCLK. Also corrected ID from duplicate SD2 to SD3. – SD3 max from: 0.7 x tCLK; to: 0.54 x tCLK – SD5 max from: 1 ns; to: 0.74 ns • Table 62, "Camera Input Signal Cross Reference, Format, and Bits Per Cycle," on page 95: Changed RGB565, 16 bits column heading from 2 cycles to 1 cycle. • Table 95, "21 x 21 mm Supplies Contact Assignment," on page 144: – Added description to ZQPAD. – Added description to GPANAIO row: "…output for NXP use only…" • Table 96, "21 x 21 mm Functional Contact Assignments," on page 146: – Changed DRAM_SDCLK_0,DRAM_SDCLK_1 from *"Input–Hi-Z"* to *"Output–*0". • Section 6.2.1.1, "21 x 21 mm Lidded Package" on page 142: Added section.
1	3/2016	Revision 1 changes are within Table 20, "Maximum Supply Currents" on page 48 Changed: • VDD-ARM_IN with condition 996 MHz, CoreMark maximum current value from 1500 to 1200 VDD-ARM_IN with condition 852 MHz, CoreMark maximum current value from 1360 to 1090 • Added footnote regarding values are assumed when VDD_ARM23_IN and VDD_ARM23_CAP are connected to ground.