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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z51f0811rfx

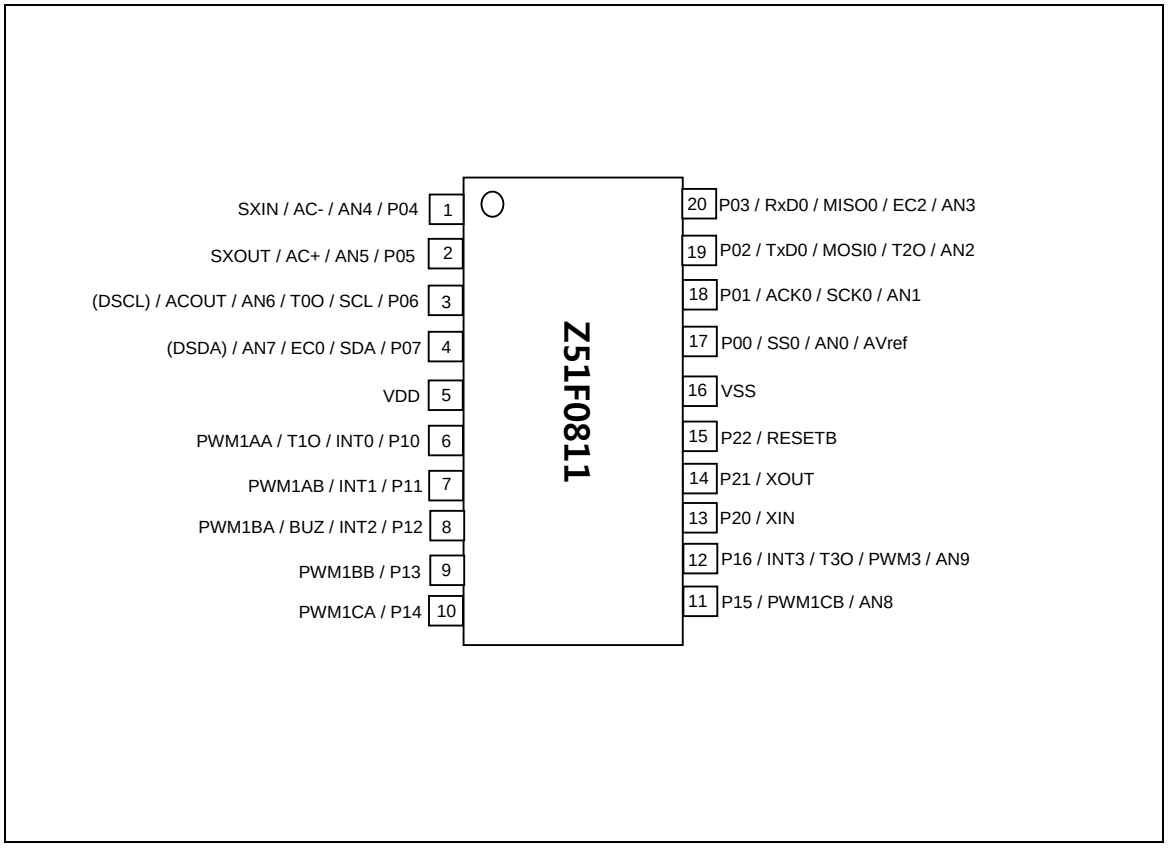

Figure 3-3 Z51F0811 20 TSSOP Pin assignment

7.11 DC Characteristics

Table 7-11 DC Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Low Voltage	VIL1	P2[2]	-0.5	-	0.2VDD	V
	VIL2	All others PAD	-0.5	-	0.2VDD	V
Input High Voltage	VIH1	P2[2]	0.8VDD	-	VDD	V
	VIH2	All others PAD	0.7VDD	-	VDD	V
Output Low Voltage	VOL1	ALL I/O (IOL=20mA, VDD=4.5V)	-	-	1	V
Output High Voltage	VOH1	ALL I/O (IOH=-8.57mA, VDD=4.5V)	3.5	-	-	V
Input High Leakage Current	IIH	ALL PAD	-	-	1	uA
Input Low Leakage Current	IIL	ALL PAD	-1	-	-	uA
Pull-Up Resister	RPU	ALL PAD	20	-	50	kΩ
Power Supply Current	IDD1	Run Mode, fXIN=12MHz @5V	-	*2.6	10	mA
	IDD2	Sleep Mode, fXIN=12MHz @5V	-	*1.5	5	mA
	IDD3	Sub Active Mode, fSUBXIN=32.768KHz @5V	-	*71	500	uA
	IDD4	STOP1 Mode, WDT Active @5V (BOD enable)	-	*45	200	uA
	IDD5	STOP1 Mode, WDT Active @5V (BOD disable)	-	*20	100	uA
	IDD6	STOP2 Mode, WDT Disable @5V (BOD enable)	-	*27	100	uA
	IDD7	STOP2 Mode, WDT Disable @5V (BOD disable)	-	*1	7 (room temp)	uA

(VDD =2.7~5.5V, VSS =0V, fXIN=10.0MHz, TA=-40~+85℃)

Note) - STOP1: WDT running, STOP2: WDT disable.

- (*) typical test condition : VDD=5V, Internal RC-OSC=8MHz, ROOM TEMP, all PORT output LOW, Timer0 Active, 1PORT toggling.

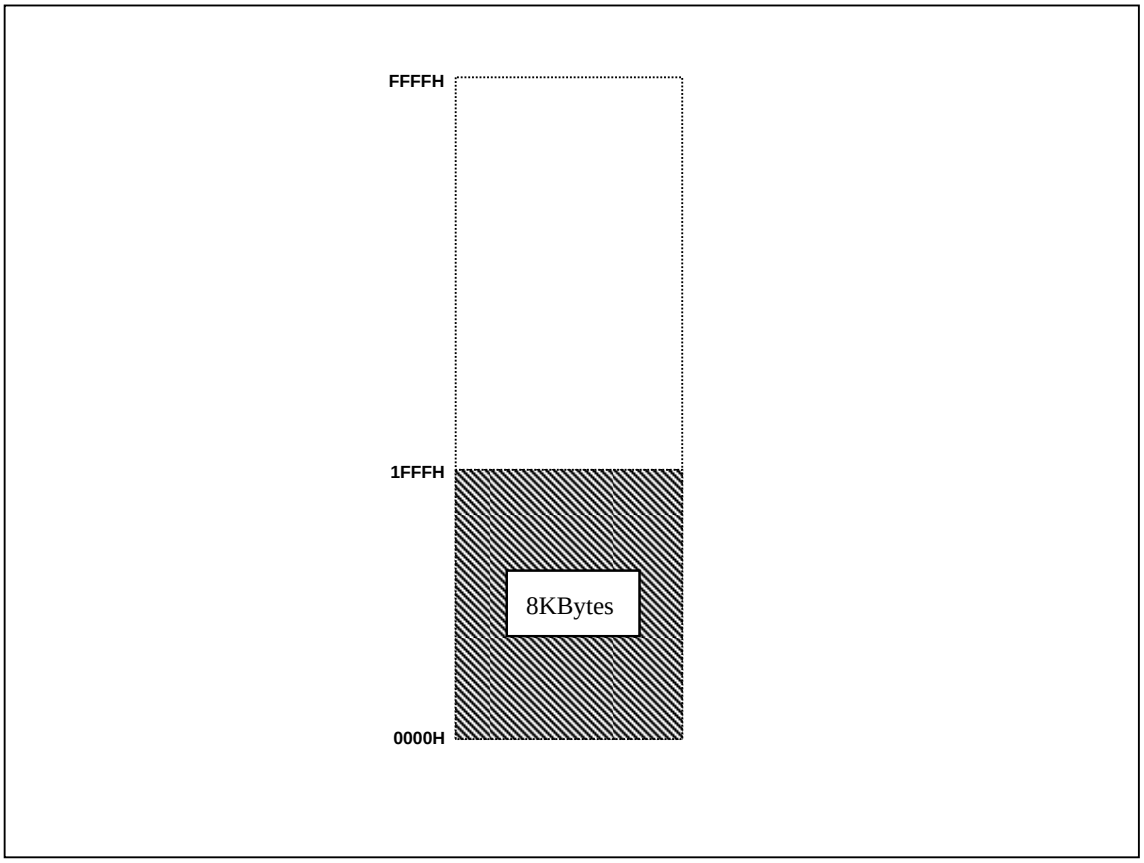

Figure 8-1 Program memory

- User Function Mode: 8KBytes Included Interrupt Vector Region
- Non-volatile and reprogramming memory: Flash memory based on EEPROM cell

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ACC Accumulator

B (B Register) : F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

B B Register

SP (Stack Pointer) : 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 07H

SP Stack Pointer

DPL (Data Pointer Low Byte) : 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL Data Pointer Low Byte

DPH (Data Pointer High Byte) : 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH Data Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

Px[7:0] I/O Data

PxIO (Px Direction Register) : 89H, 91H, 99H, A1H

7	6	5	4	3	2	1	0
Px7IO	Px6IO	Px5IO	Px4IO	Px3IO	Px2IO	Px1IO	Px0IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PxIO[7:0] Px data I/O direction.

0 Input

1 Output

PxPU (Px Pull-up Resistor Selection Register) : 2F00H ~ 2F03H

7	6	5	4	3	2	1	0
Px7PU	Px6PU	Px5PU	Px4PU	Px3PU	Px2PU	Px1PU	Px0PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PxPU[7:0] Configure pull-up resistor of Px port

0 Disable

1 Enable

PxOD (Px Open-drain Selection Register) : 2F0CH ~ 2F0FH

7	6	5	4	3	2	1	0
Px7OD	Px6OD	Px5OD	Px4OD	Px3OD	Px2OD	Px1OD	Px0OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PxOD[7:0] Configure open-drain of Px port

0 Disable

1 Enable

PxDB (Px Debounce Enable Register) : 2F18H ~ 2F1BH

7	6	5	4	3	2	1	0
Px7DB	Px6DB	Px5DB	Px4DB	Px3DB	Px2DB	Px1DB	Px0DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PxDB[7:0] Configure debounce of Px port

0 Disable

1 Enable

PCI0 (P0 Pin Change Interrupt Enable Register) : AEH

7	6	5	4	3	2	1	0
PCI07	PCI06	PCI05	PCI04	PCI03	PCI02	PCI01	PCI00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

10.12.8 Register Map

Table 10-3 Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IE4	ACH	R/W	00H	Interrupt Enable Register 4
IE5	ADH	R/W	00H	Interrupt Enable Register 5
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIENAB	A3H	R/W	00H	External Interrupt Enable Register
EIFLAG	A4H	R/W	00H	External Interrupt Flag Register
EIEDGE	A5H	R/W	00H	External Interrupt Edge Register
EIPOLA	A6H	R/W	00H	External Interrupt Polarity Register
EIBOTH	A7H	R/W	00H	External Interrupt Both Edge Enable Register

10.13 Interrupt Register Description

The Interrupt Register is used for controlling interrupt functions. Also it has External interrupt control registers. The interrupt register consists of Interrupt Enable Register (IE), Interrupt Enable Register 1 (IE1), Interrupt Enable Register 2 (IE2), Interrupt Enable Register 3 (IE3), Interrupt Enable Register 4 (IE4) and Interrupt Enable Register 5 (IE5). For external interrupt, it consists of External Interrupt Flag Register (EIFLAG), External Interrupt Edge Register (EIEDGE), External Interrupt Polarity Register (EIPOLA), External Interrupt Enable Register (EIENAB) and External Interrupt Both Edge Enable Register(EIBOTH).

10.13.1 Register description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	-	INT5E	INT4E	INT3E	INT2E	INT1E	INT0E
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

EA Enable or disable all interrupt bits
- 0 All Interrupt disable
- 1 All Interrupt enable

INT5E Reserved
- 0 Disable
- 1 Enable

INT4E Enable or disable Pin Change Interrupt 0 (Port 0)
- 0 Disable
- 1 Enable

INT3E Enable or disable External Interrupt 3
- 0 Disable

Level case:

0 When High level, Interrupt occurred (default)

1 When Low level, Interrupt occurred

Edge case:

0 When Rising edge, Interrupt occurred (default)

1 When Falling edge, Interrupt occurred

EIENAB (External Interrupt Enable Register) : A3H

7	6	5	4	3	2	1	0
ENAB7	ENAB6	ENAB5	ENAB4	ENAB3	ENAB2	ENAB1	ENAB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ENAB[7:0] Control External Interrupt

0 Disable (default)

1 Enable

EIBOTH (External Interrupt Both Edge Enable Register) : A7H

7	6	5	4	3	2	1	0
BOTH7	BOTH6	BOTH5	BOTH4	BOTH3	BOTH2	BOTH1	BOTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

BOTH[7:0] Determines which type of interrupt may occur, EIBOTH or EIEDGE+EIPOLA. if EIBOTH is enable, EIEDGE and EIPOLA register value don't matter.

0 Disable (default)

1 Enable

11.5 Timer/PWM

11.5.1 8-bit Timer/Event Counter 0, 1

11.5.1.1 Overview

Timer 0 and timer 1 can be used either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, 8-bit timer data register, 8-bit counter register, mode register, input capture register, comparator. For PWM, it has PWM register (T1PPR, T1ADR, T1BDR, T1CDR, T1PCR, T1PCR2, T1PCR3, T1PHR, T1DLYA, T1DLYB, T1DLYC, T1ISR, T1IMSK).

It has seven operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 8-bit compare output mode
- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit compare output mode
- PWM mode

Note> TxDR must be set to higher than 0x03 for guaranteeing operation.

The timer/counter can be clocked by an internal or an external clock source (external EC0). The clock source is selected by clock select logic which is controlled by the clock select (T0CK[2:0], T1CK[3:0]). Also the timer/PWM/event counter 1 can use more clock sources than timer/event counter 0.

- TIMER0 clock source: fX/2, 4, 8, 32, 128, 512, 2048, EC0
- TIMER1 clock source: fX/1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, T0CK

In the capture mode, by INT0, INT1, the data is captured into Input Capture Register. The timer 0 outputs the compare result to T0 port in 8/16-bit mode. Also the timer 1 outputs the result to T1 port in the timer mode and the PWM wave form to PWMA, PWMAB(bar), PWMB, PWMBB, PWMC, PWMCB Port(6-channel) in the PWM mode.

Table 11-5 Timer 0,1 operating modes

16 Bit	CAP0	CAP1	PWM1E	T0CK[2:0]	T1CK[3:0]	T0/1_PE	Timer 0	Timer 1
0	0	0	0	XXX	XXXX	00	8 Bit Timer	8 Bit Timer
0	0	1	0	111	XXXX	00	8 Bit Event Counter	8 Bit Capture
0	1	0	0	XXX	XXXX	01	8 Bit Capture	8 Bit Compare Output
0	0	0	1	XXX	XXXX	11	8 Bit Timer/Counter	10 Bit PWM
1	0	0	0	XXX	1111	00	16 Bit Timer	
1	0	0	0	111	1111	00	16 Bit Event Counter	
1	1	1	0	XXX	1111	00	16 Bit Capture	
1	0	0	0	XXX	1111	01	16 Bit Compare Output	

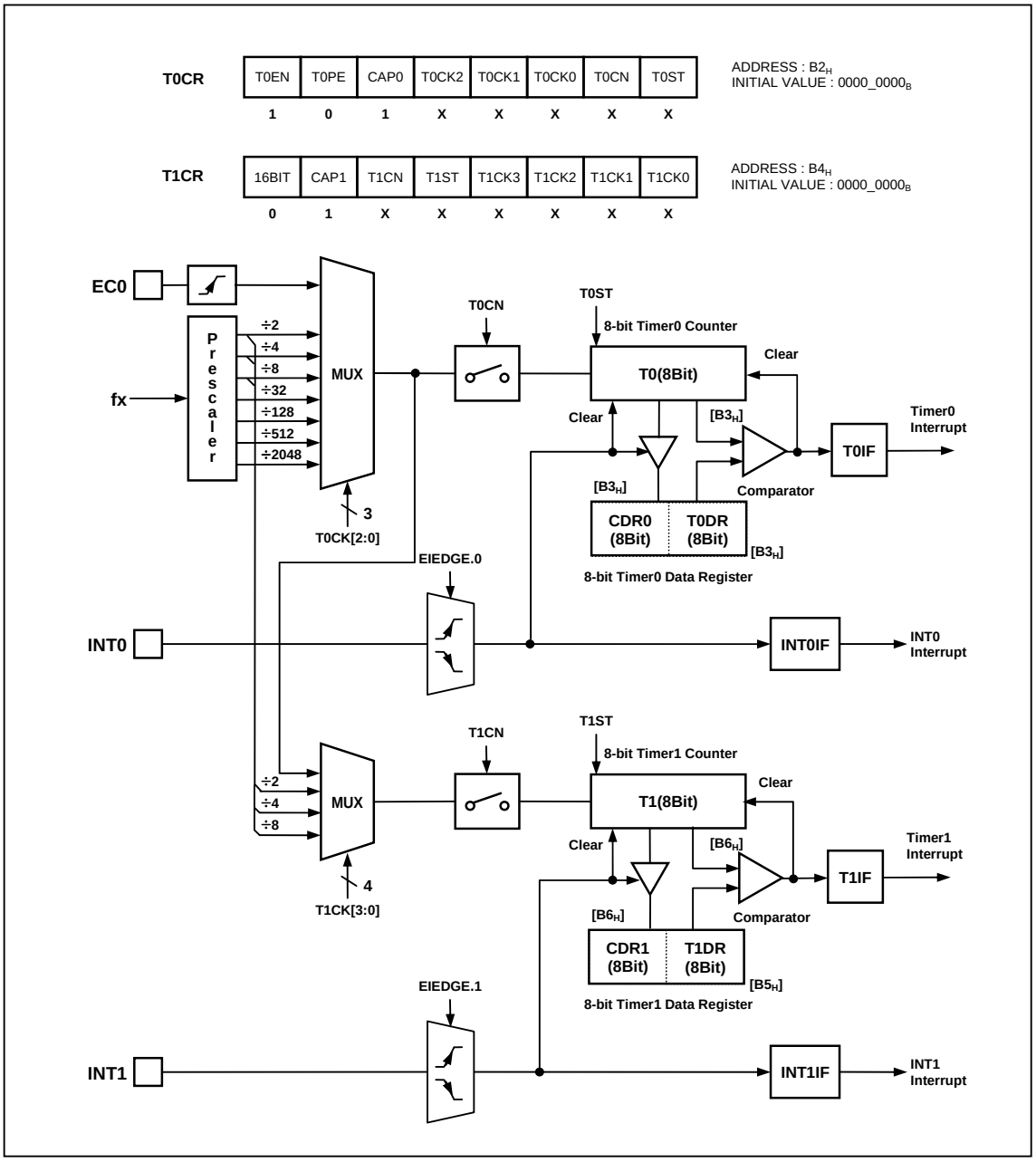

Figure 11-10 8-bit Capture Mode for Timer 0, 1

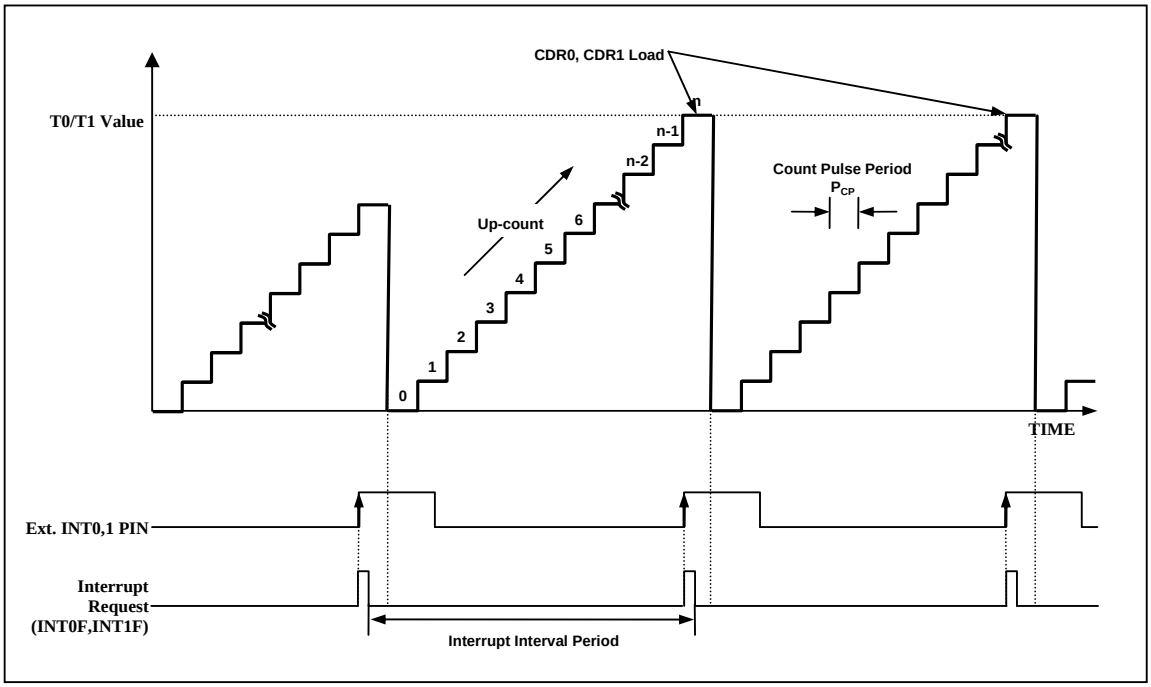

Figure 11-11 Input Capture Mode Operation of Timer 0, 1

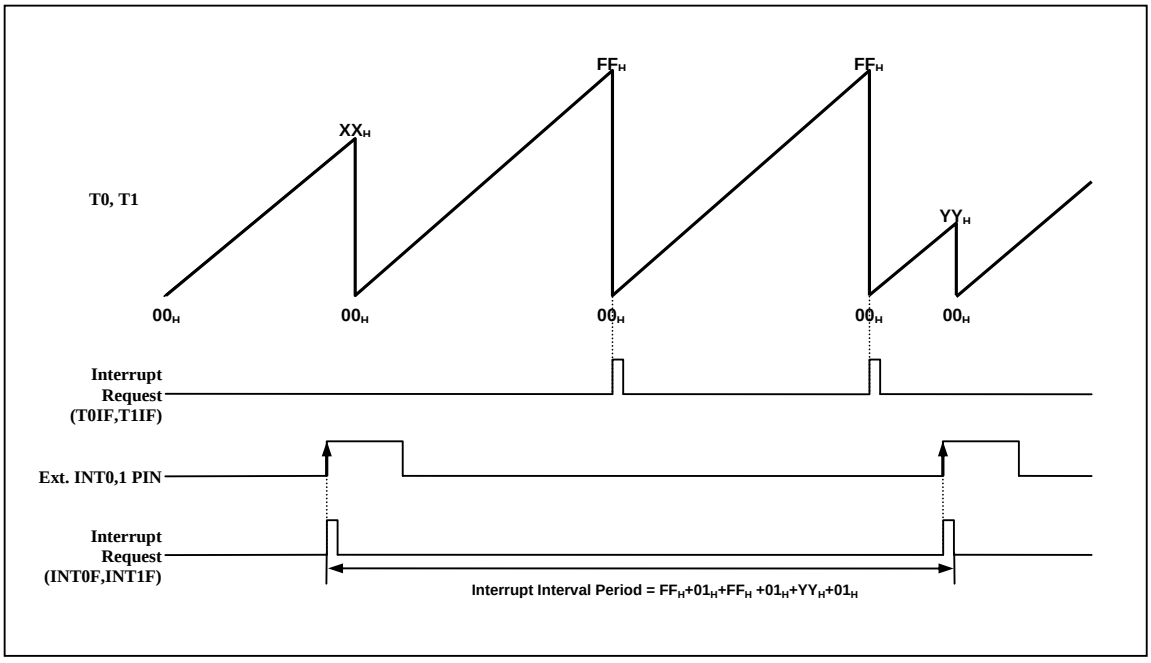

Figure 11-12 Express Timer Overflow in Capture Mode

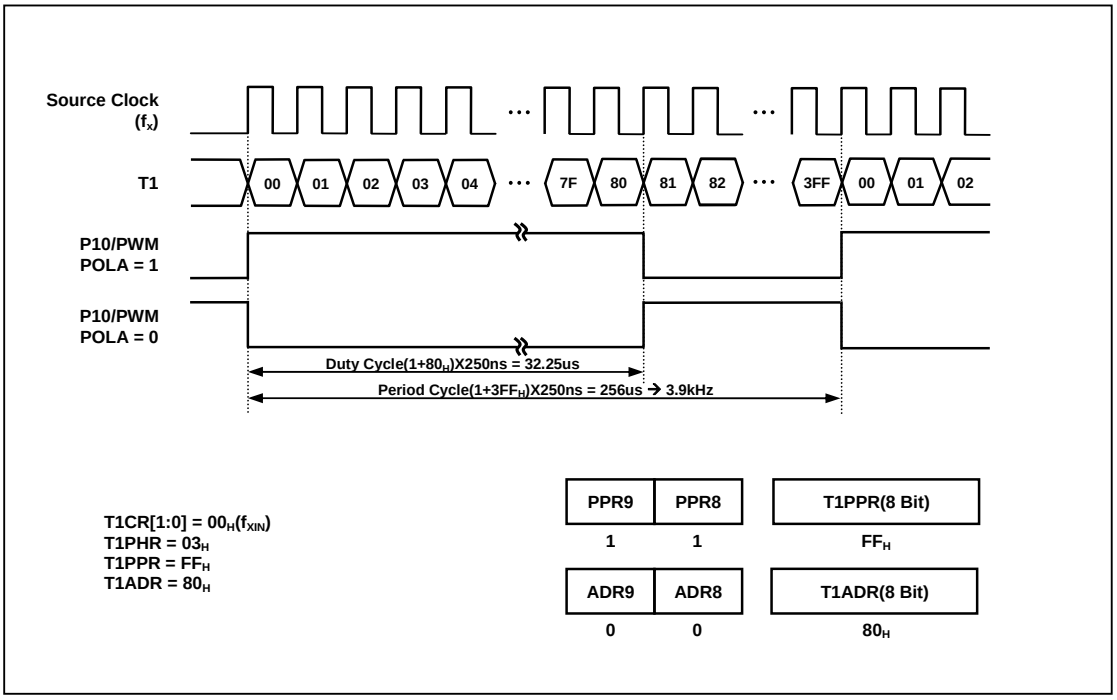

Figure 11-16 Example of PWM at 4MHz

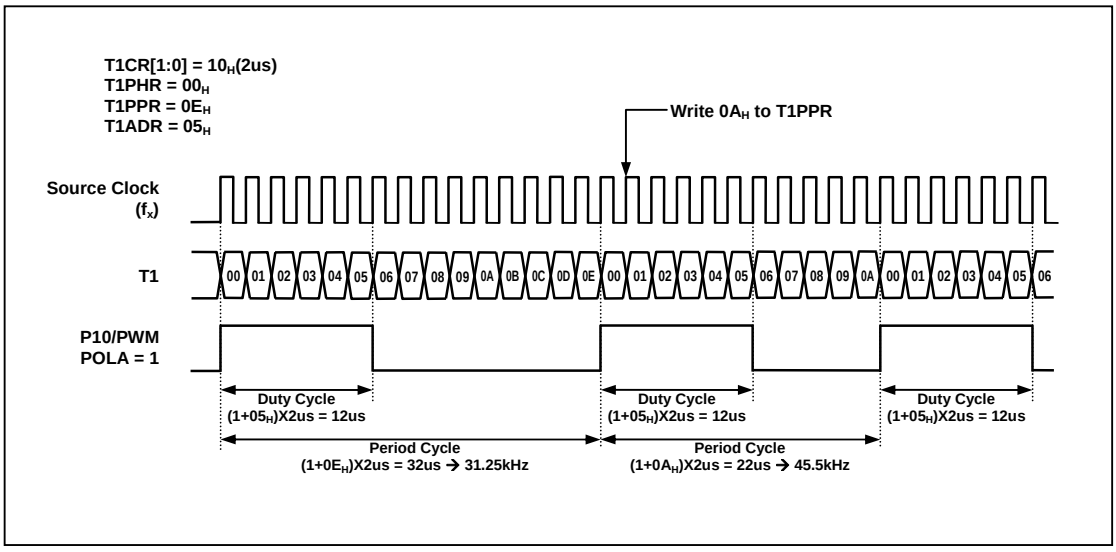

Figure 11-17 Example of Changing the Period in Absolute Duty Cycle at 4Mhz

Update period & duty register value at once

The period and duty of PWM comes to move from temporary registers to PPR (PWM Period Register) and PDR (PWM Duty Register) when always period match occurs. If you want that the period and duty is immediately changed, the UPDT bit in the T1PCR register must set to '1'. It should be noted that it needs the 3 cycle of timer clock for data transfer in the internal clock synchronization circuit. So the update data is written before 3 cycle of timer clock to get the right output waveform.

Phase correction & Frequency correction

T0DR (Timer 0 Data Register: Write Case) : B3H

7	6	5	4	3	2	1	0
T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
W	W	W	W	W	W	W	W

Initial value : FFH

T0D[7:0] T0 Compare

CDR0 (Capture 0 Data Register: Read Case, Capture mode only) : B3H

7	6	5	4	3	2	1	0
CDR07	CDR06	CDR05	CDR04	CDR03	CDR02	CDR01	CDR00
R	R	R	R	R	R	R	R

Initial value : 00H

CDR0[7:0] T0 Capture

T1CR (Timer 1 Mode Count Register) : B4H

7	6	5	4	3	2	1	0
16BIT	CAP1	T1CN	T1ST	T1CK3	T1CK2	T1CK1	T1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

16BIT Select Timer 1 8/16Bit
- 0 8 Bit
- 1 16 Bit

CAP1 Control Timer 1 operation mode
- 0 Timer/Counter mode
- 1 Capture mode

T1CN Control Timer 1 Count pause/continue
- 0 Temporary count stop
- 1 Continue count

T1ST Control Timer 1 start/stop
- 0 Counter stop
- 1 Clear counter and start

T1CK[3:0] Select Timer 1 clock source. Fx is main system clock frequency

T1CK3	T1CK2	T1CK1	T1CK0	description
0	0	0	0	fx
0	0	0	1	fx/2
0	0	1	0	fx/4
0	0	1	1	fx/8
0	1	0	0	fx/16
0	1	0	1	fx/32
0	1	1	0	fx/64
0	1	1	1	fx/128
1	0	0	0	fx/256
1	0	0	1	fx/512
1	0	1	0	fx/1024
1	0	1	1	fx/2048
1	1	0	0	fx/4096

T1BDR (Timer 1 PWM 1B Duty Register) : BAH

7	6	5	4	3	2	1	0
PBD7	PBD6	PBD5	PBD4	PBD3	PBD2	PBD1	PBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 7FH

T1BDR[7:0] PWM 1B ch Duty
Note) only write, when PWM1E '1'

T1CDR (Timer 1 PWM 1C Duty Register) : BBH

7	6	5	4	3	2	1	0
PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 7FH

T1CDR[7:0] PWM 1C ch Duty
Note) only write, when PWM1E '1'

T1PHR (Timer 1 PWM High Register) : BCH

7	6	5	4	3	2	1	0
ADR9	ADR8	BDR9	BDR8	CDR9	CDR8	PPR9	PPR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ADR[9:8] PWM 1A High (Bit [9:8])
BDR[9:8] PWM 1B High (Bit [9:8])
CDR[9:8] PWM 1C High (Bit [9:8])
PPR[9:8] PERIOD High (Bit [9:8])

PERIOD:	PPR9	PPR8	T1PPR[7:0]
DUTY A:	ADR9	ADR8	P1ADR[7:0]
DUTY B:	BDR9	BDR8	P1BDR[7:0]
DUTY C:	CDR9	CDR8	P1CDR[7:0]

T1PCR2 (Timer 1 PWM Control Register 2) : BDH

7	6	5	4	3	2	1	0
FORCA	FORC6	PAOE	PABOE	PBOE	PBBOE	PCOE	PCBOE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

FORCA Control Force Drive A Channel mode
0 Force Drive A Channel mode disable
1 Force Drive A Channel mode enable

FORC6 Control Force 6 Channel mode
Note) PAOE~PCBOE is effective when FORC6 sets to '1'
0 Force 6 Channel mode disable
1 Force 6 Channel mode enable

PAOE/ PABOE Select Channel A/AB operation
0 P1A (or P1AB) output disable
1 P1A (or P1AB) output enable

PBOE/ PBBOE Select Channel B/BB operation
0 P1B (or P1BB) output disable
1 P1B (or P1BB) output enable

T2DR (Timer 2 Data Register: Write Case) : C7H

7	6	5	4	3	2	1	0
T2D7	T2D6	T2D5	T2D4	T2D3	T2D2	T2D1	T2D0
W	W	W	W	W	W	W	W

Initial value : FFH

T2D[7:0] T2 Compare data

CDR2 (Capture 2 Data Register: Read Case) : C7H

7	6	5	4	3	2	1	0
CDR27	CDR26	CDR25	CDR24	CDR23	CDR22	CDR21	CDR20
R	R	R	R	R	R	R	R

Initial value : 00H

CDR2[7:0] T2 Capture data

T3CR (Timer 3 Mode Count Register) : CAH

7	6	5	4	3	2	1	0
POL	16BIT	PWM3E	CAP3	T3CK1	T3CK0	T3CN	T3ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

POL Configure PWM polarity
- 0 Negative (Duty Match: Clear)
- 1 Positive (Duty Match: Set)

16BIT Select Timer 1 8/16Bit
- 0 8 Bit
- 1 16 Bit

PWM3E Control PWM enable
- 0 PWM disable
- 1 PWM enable

CAP3 Control Timer 3 mode
- 0 Timer/Counter mode
- 1 Capture mode

T3CK[1:0] Select clock source of Timer 3. Fx is the frequency of main system.

T3CK1	T3CK0	Description
0	0	fx
0	1	fx/2
1	0	fx/16
1	1	Use Timer 2 Clock

Note) If you want to use “Using Timer 2 Clock”, you can set T2EN bit in T2CR

T3CN Control Timer 3 Count pause/continue
- 0 Temporary count stop
- 1 Continue count

T3ST Control Timer 3 start/stop
- 0 Counter stop
- 1 Clear counter and start

T3DR (Timer 3 Data Register: Write Case) : CBH

11.5.3.3 Register Map

Table 11-11 Register Map

Name	Address	Dir	Default	Description
T4CR	0xCE	R/W	00H	Timer 4 Mode Control Register
T4L	0xCF	R	00H	Timer 4 Low Register
T4LDR	0xCF	W	FFH	Timer 4 Low Data Register
LCDR4	0xCF	R	00H	Low Capture 4 Data Register
T4H	0xD5	R	00H	Timer 4 High Register
T4HDR	0xD5	R/W	00H	Timer 4 High Data Register
HCDR4	0xD5	R	00H	High Capture 4 Data Register

11.5.3.4 Timer 4 Register description

The timer 4 register consists of Timer 4 Mode Control Register (T4CR), Timer 4 Low Register (T4L), Timer 4 Low Data Register (T4LDR), Low Capture 4 Data Register (LCDR4), Timer 4 High Register (T4H), Timer 4 High Data Register (T4HDR), High Capture 4 Data Register (HCDR4).

11.5.3.5 Register description for Timer 4

T4CR (Timer 4 Mode Control Register) : CEH

7	6	5	4	3	2	1	0
T4EN	-	CAP4	T4CK2	T4CK1	T4CK0	T4CN	T4ST
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T4EN Control Timer 4 operation
- 0 Timer 4 disable
- 1 Timer 4 enable

CAP4 Control Timer 4 mode
- 0 Timer/Counter mode
- 1 Capture mode

T4CK[2:0] Select Timer 4 clock source. fx is main system clock frequency

T4CK2	T4CK1	T4CK0	Description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/16
1	0	0	fx/64
1	0	1	fx/256
1	1	0	fx/1024
1	1	1	fx/2048

T4CN Control Timer 4 Count pause/continue
- 0 Temporary count stop
- 1 Continue count

T4ST Control Timer 4 start/stop

SPIDR (SPI Data Register) : D3H

7	6	5	4	3	2	1	0
SPIDR7	SPIDR6	SPIDR5	SPIDR4	SPIDR3	SPIDR2	SPIDR1	SPIDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

SPIDR [7:0] SPI data register.
Although you only use reception, user must write any data in here to start the SPI operation.

SPISR (SPI Status Register) : D4H

7	6	5	4	3	2	1	0
TCIR	WCOL	SS_HIGH	-	TWOPIN	SSENA	TXENA	RXENA
R	R	R/W	-	R/W	R/W	R/W	R/W

Initial value : 00H

TCIR When a serial data transmission is complete, the TCIR bit is set. If the SPI interrupt is enabled, an interrupt is requested. And TCIR bit is cleared by hardware when executing the corresponding interrupt. If SPI interrupt is disable, TCIR bit is cleared when user read the status register SPISR, and then access (read/write) the data register SPIDR.

0 Interrupt cleared

1 Transmission Complete and Interrupt Requested

WCOL This bit is set if the data register SPIDR is written during a data transfer. This bit is cleared when user read the status register SPISR, and then access (read/write) the data register SPIDR.

0 No collision

1 Write Collision

SS_HIGH When SS pin is configured as input(master or slave), if ‘HIGH’ signal come into SS pin, this flag bit will be set at the SS rising time. And you can clear it by writing ‘0’.
You can write only zero.

0 Flag is cleared

1 Flag is set

TWOPIN This bit controls the 2 pin operation.
In master mode,

0 Disable

1 Enable

SSENA This bit controls the SS pin operation

0 Disable

1 Enable

TXENA This bit controls a data transfer operation

0 Disable

1 Enable

RXENA This bit controls a data reception operation

0 Disable

1 Enable

Note that if the MS is set to ‘0’, when TWOPIN is set to ‘0’, port 03 is set to MISO and if the MS is set to ‘0’, when TWOPIN is set to ‘1’, port 02 is set to MOSI. But if the MS is set to ‘1’, when TWOPIN is set to ‘0’, port 03 is set to MOSI and if the MS is set to ‘1’, when TWOPIN is set to ‘1’, port 02 is set to MISO.

the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

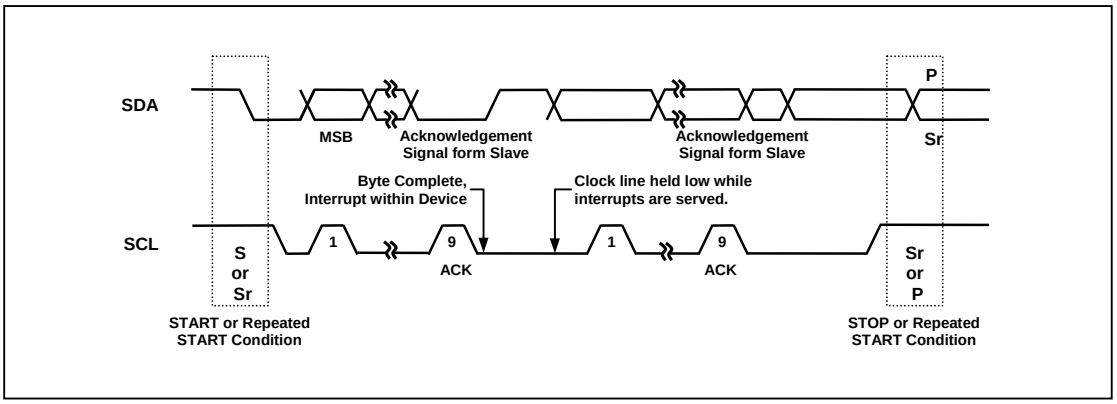

Figure 11-54 STOP or Repeated START Condition

11.9.6 Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

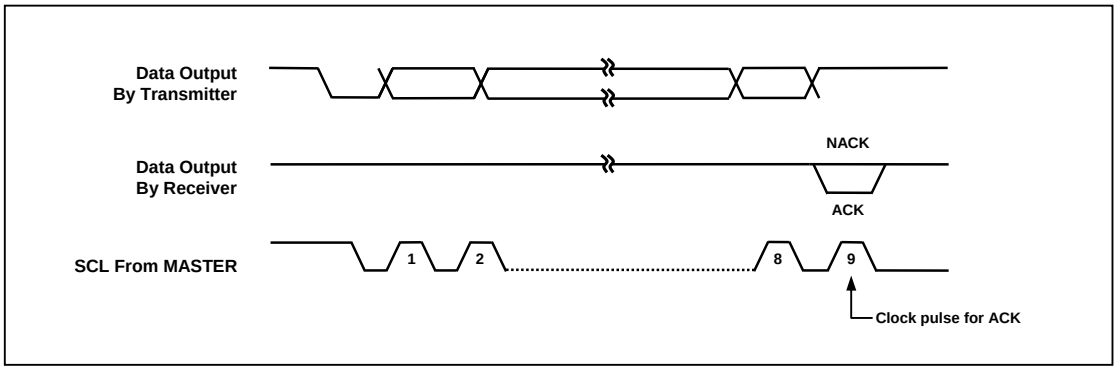

Figure 11-55 Acknowledge on the I^2C-Bus

load SLA+R/W into the I2CDR and set the START bit in I2CMR.

After doing one of the actions above, write arbitrary value to I2CSR to release SCL line. In case of 1) and 2), move to step 7. In case of 3), move to step 9 to handle STOP interrupt. In case of 4), move to step 6 after transmitting the data in I2CDR, and if transfer direction bit is '0' go to master transmitter section.

9. This is the final step for master receiver function of I^2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2CSR, write arbitrary value to I2CSR. After this, I^2C enters idle state.

The processes described above for master receiver operation of I^2C can be depicted as the following figure.

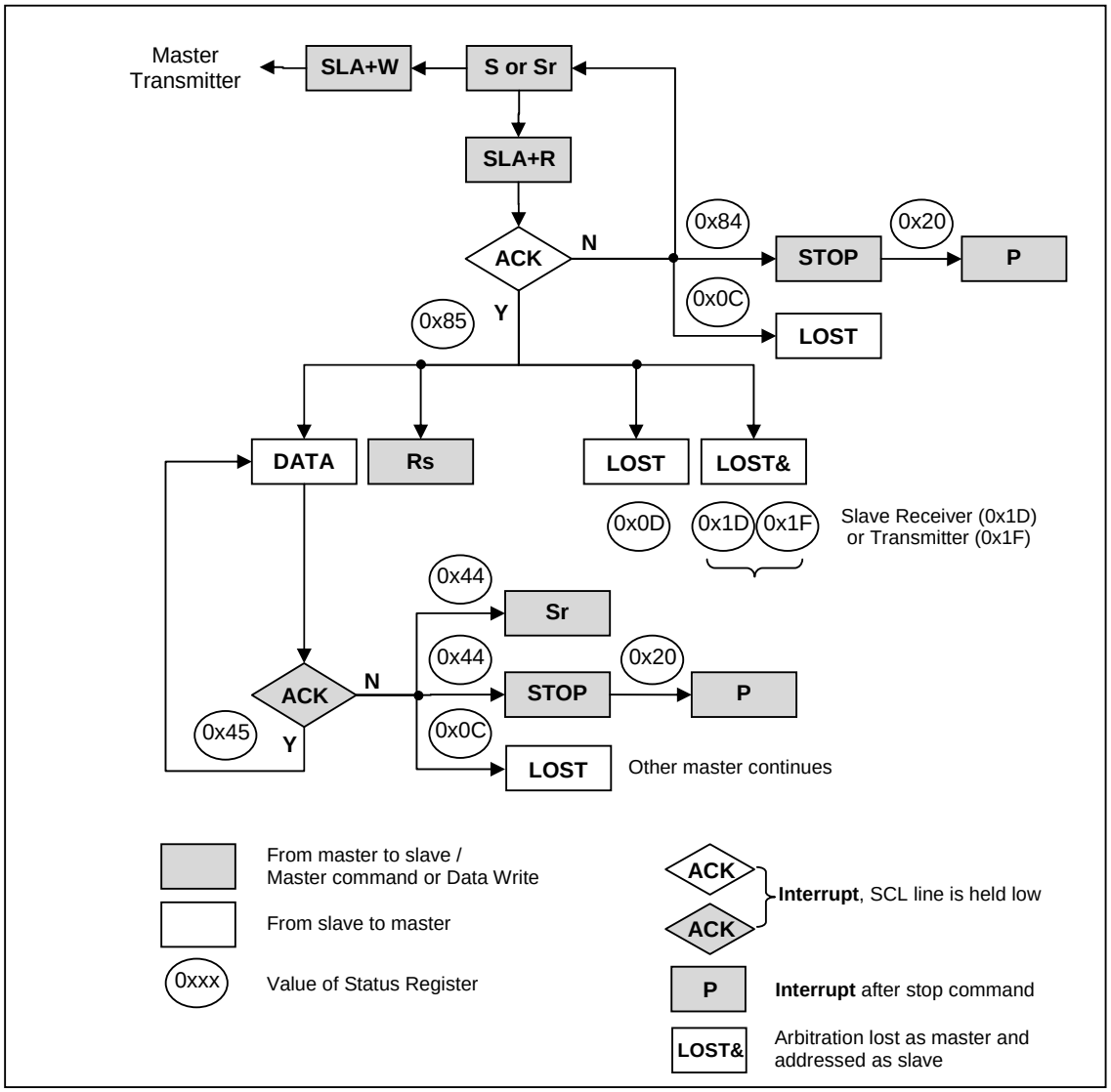

Figure 11-59 Formats and States in the Master Receiver Mode

	0	No detection
	1	Detection

EXTRF External Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0	No detection
1	Detection

WDTRF Watch Dog Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0	No detection
1	Detection

OCDRF On-Chip Debug Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0	No detection
1	Detection

BODRF Brown-Out Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0	No detection
1	Detection

BODLS[1:0] BOD level Voltage

BODLS1	BODLS0	Description
0	0	1.6V
0	1	2.5V
1	0	3.6V
1	1	4.2V

BODEN BOD operation

0	BOD disable
1	BOD enable

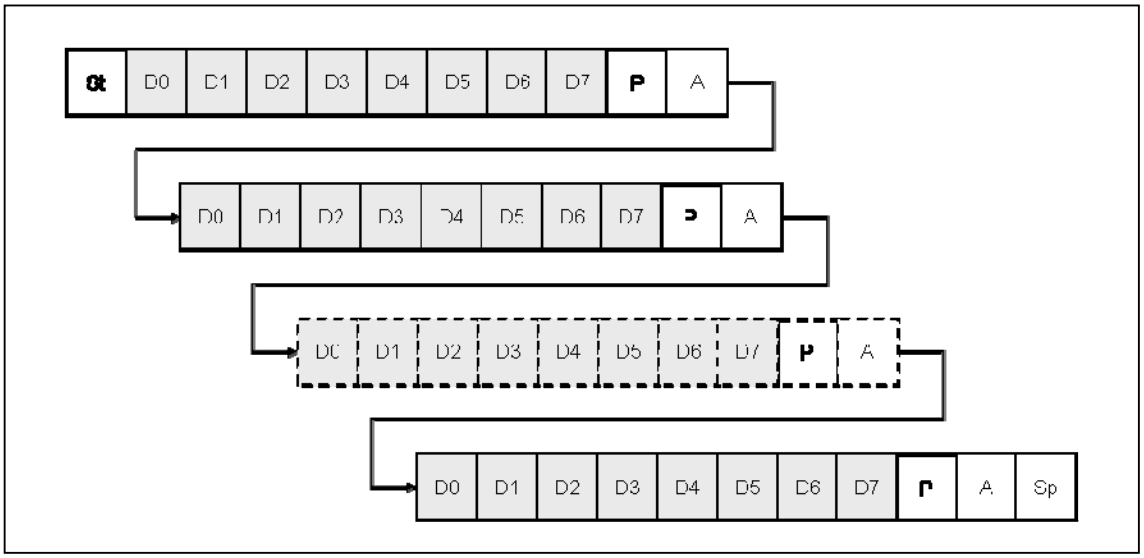

Figure 14-2 10-bit transmission packet

14.2.2 Packet transmission timing

14.2.2.1 Data transfer

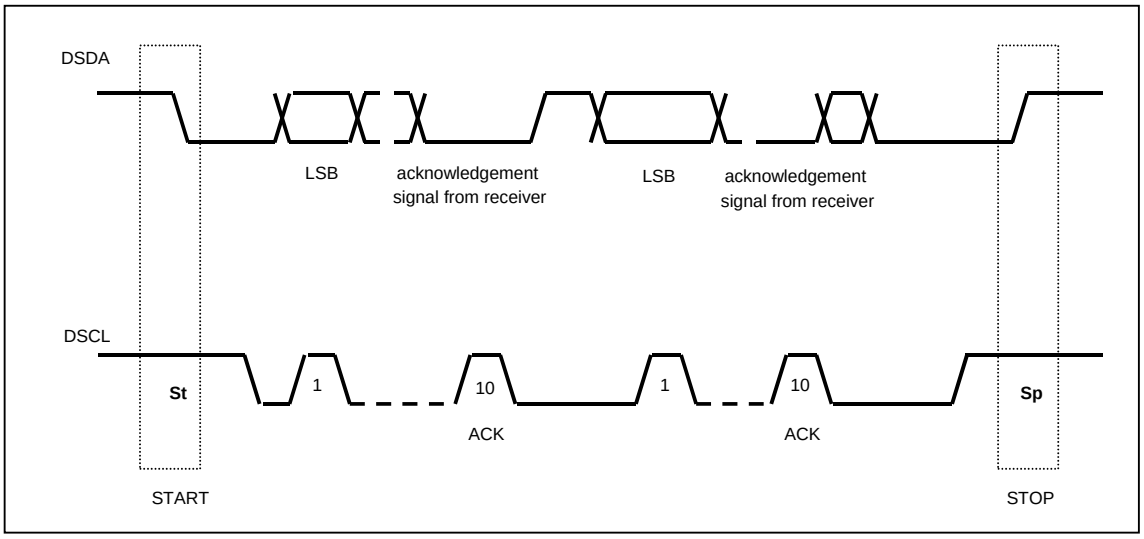

Figure 14-3 Data transfer on the twin bus