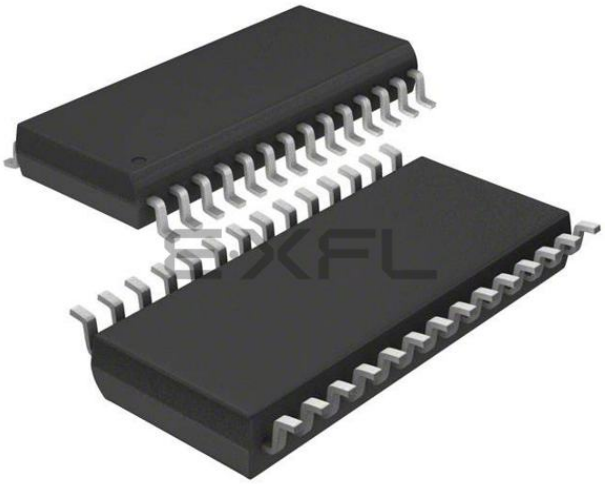

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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z51f0811rjx

9.2.7 Port Selection Register (PSRx)

PSRx registers prevent the input leakage current when ports are connected to analog inputs. If the bit of PSRx is '1', the dynamic current path of the schmitt OR gate of the port is cut off and the digital input of the corresponding port is always '1'.

9.2.8 Register Map

Table 9-1 Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	89H	R/W	00H	P0 Direction Register
P0PU	2F00H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	2F0CH	R/W	00H	P0 Open-drain Selection Register
P0DB	2F18H	R/W	00H	P0 Debounce Enable Register
PCI0	AEH	R/W	00H	P0 Pin Change Interrupt Enable Register
P1	88H	R/W	00H	P1 Data Register
P1IO	91H	R/W	00H	P1 Direction Register
P1PU	2F01H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	2F0DH	R/W	00H	P1 Open-drain Selection Register
P1DB	2F19H	R/W	00H	P1 Debounce Enable Register
P2	90H	R/W	00H	P2 Data Register
P2IO	99H	R/W	00H	P2 Direction Register
P2PU	2F02H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	2F0EH	R/W	00H	P2 Open-drain Selection Register
P2DB	2F1AH	R/W	00H	P2 Debounce Enable Register
P3	98H	R/W	00H	P3 Data Register
P3IO	A1H	R/W	00H	P3 Direction Register
P3PU	2F03H	R/W	00H	P3 Pull-up Resistor Selection Register
P3OD	2F0FH	R/W	00H	P3 Open-drain Selection Register
P3DB	2F1BH	R/W	00H	P3 Debounce Enable Register
PSR0	2F50H	R/W	00H	Port Selection Register 0
PSR1	2F51H	R/W	00H	Port Selection Register 1,2,3

9.3 Px Port

9.3.1 Px Port Description

Px is 8-bit I/O port. Px control registers consist of Data register (Px), direction register (PxIO), debounce enable register (PxDB), pull-up register selection register (PxPU), open-drain selection register (PxOD), pin change interrupt register (PCI0)

9.3.2 Register description for Px

Px (Px Data Register) : 80H, 88H, 90H, 98H

7	6	5	4	3	2	1	0
Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0

10. Interrupt Controller

10.1 Overview

The Z51F0811 supports up to 32 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The interrupt controller has following features:

- receive the request from 32 interrupt source
- 8 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is serviced
- Each interrupt source can control by EA bit and each IEx bit
- Interrupt latency: 5~8 machine cycles in single interrupt system

The maskable interrupts are enabled through six of interrupt enable registers (IE, IE1, IE2, IE3, IE4, IE5). Bits of IE, IE1, IE2, IE3, IE4, IE5 register each individually enable/disable a particular interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to '0', all interrupts are disabled: when EA is set to '1', interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The Z51F0811 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels by writing to IP or IP1.

Interrupt default mode is level-trigger basically but if needed, it is able to change edge-trigger mode. Table 10-1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority sets two bit which is to IP and IP1 register about group. Interrupt service routine services higher priority. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If the request of same or lower priority level is received, that request is not serviced.

Table 10-1 Interrupt Group Priority Level

Interrupt Group	Highest → Lowest				
0 (Bit0)	Interrupt0	Interrupt8	Interrupt16	Interrupt24	Highest
1 (Bit1)	Interrupt1	Interrupt9	Interrupt17	Interrupt25	
2 (Bit2)	Interrupt2	Interrupt10	Interrupt18	Interrupt26	
3 (Bit3)	Interrupt3	Interrupt11	Interrupt19	Interrupt27	
4 (Bit4)	Interrupt4	Interrupt12	Interrupt20	Interrupt28	
5 (Bit5)	Interrupt5	Interrupt13	Interrupt21	Interrupt29	
6 (Bit6)	Interrupt6	Interrupt14	Interrupt22	Interrupt30	
7 (Bit7)	Interrupt7	Interrupt15	Interrupt23	Interrupt31	Lowest

10.2 External Interrupt

The external interrupt on INT0, INT1, INT2, INT3, INT4, INT5, INT6 and INT7 pins receive various interrupt request depending on the EIEDGE (External Interrupt Edge register) and EIPOLA (External

11.2 BIT

11.2.1 Overview

The Z51F0811 has one 8-bit Basic Interval Timer that is free-run and can't stop. Block diagram is shown in Figure 11-2. In addition, the Basic Interval Timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITF).

The Z51F0811 has these Basic Interval Timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As clock function, time interrupt occurrence

11.2.2 Block Diagram

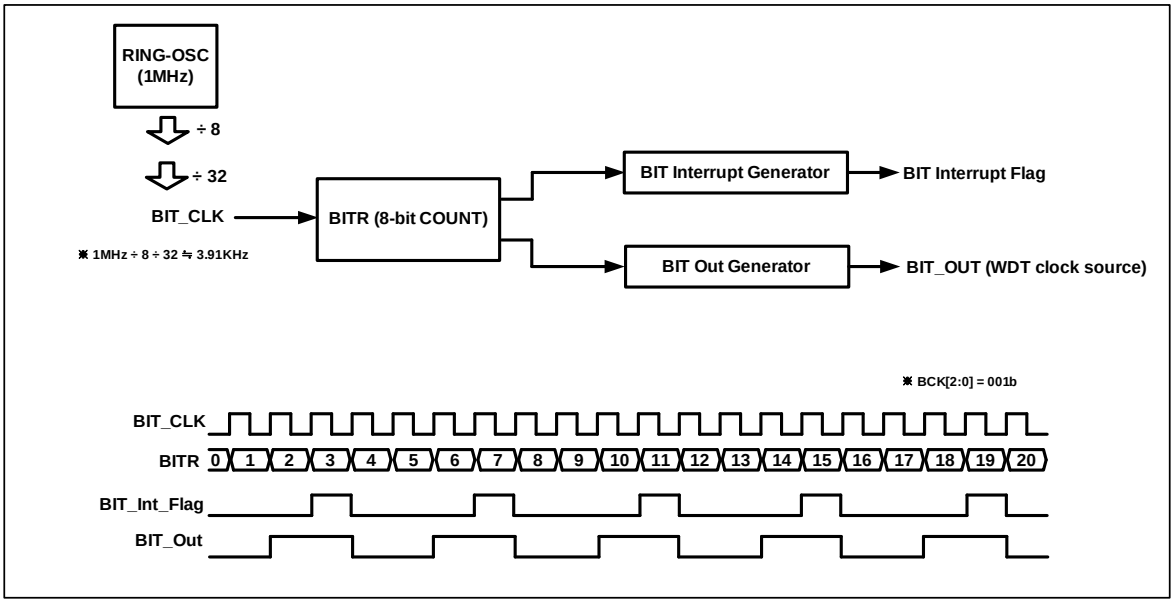

Figure 11-2 BIT Block Diagram

11.2.3 Register Map

Table 11-2 Register Map

Name	Address	Dir	Default	Description
BCCR	8BH	R/W	05H	BIT Clock Control Register
BITR	8CH	R	00H	Basic Interval Timer Register

11.2.4 Bit Interval Timer Register description

The Bit Interval Timer Register consists of BIT Clock control register (BCCR) and Basic Interval Timer register (BITR). If BCLR bit set to '1', BITR becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared as '0' automatically.

11.2.5 Register description for Bit Interval Timer

BCCR (BIT Clock Control Register) : 8BH

7	6	5	4	3	2	1	0
BITF	-	-	-	BCLR	BCK2	BCK1	BCK0
R/W	R	R	R	R/W	R/W	R/W	R/W

Initial value : 05H

BITF When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit.

0 no generation

1 generation

BCLR If BCLR Bit is written to '1', BIT Counter is cleared as '0'

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period (BIT Clock ≒3.9 KHz)

BCK2	BCK1	BCK0	
0	0	0	0.512msec (BIT Clock * 2)
0	0	1	1.024msec
0	1	0	2.048msec
0	1	1	4.096msec
1	0	0	8.192msec
1	0	1	16.384msec (default)
1	1	0	32.768msec
1	1	1	65.536msec

BITR (Basic Interval Timer Register) : 8CH

7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R	R	R	R	R	R	R	R

Initial value : 00H

BIT[7:0] BIT Counter

11.5.1.6 PWM Mode

The timer 1 has a high speed PWM (pulse Width Modulation) function. In PWM mode, the 6-channel pins output up to 10-bit resolution PWM output. This pin should be configured as a PWM output by set PWM1E to '1'. The period of the PWM output is determined by the T1PPR (PWM period register) + T1PHR[1:0], T1xDR (each channel PWM duty register) + T1PHR[7:2].

PWM Period = [T1PHR[1:0]T1PPR] X Source Clock
PWM Duty(A-ch) = [T1PHR[7:6] T1ADR] X Source Clock

Note> T1PPR must be set to higher than T1PDR for guaranteeing operation.

Table 11-6 PWM Frequency vs. Resolution at 8 Mhz

Resolution	Frequency		
	T1CK[3:0]=0001 (250ns)	T1CK[3:0]=0010 (500ns)	T1CK[3:0]=0100 (2us)
10 Bit	3.9KHz	1.95KHz	0.49KHz
9 Bit	7.8KHz	3.9KHz	0.98KHz
8 Bit	15.6KHz	7.8KHz	1.95KHz
7 Bit	31.2KHz	15.6KHz	3.91KHz

The POLx bit of T1PCR3 register decides the polarity of duty cycle. If the duty value is set same to the period value, the PWM output is determined by the bit POLx (1: High, 0: Low). And if the duty value is set to "00H", the PWM output is determined by the bit POLx (1: Low, 0: High).

Figure 11-21 Example of PWM External Synchronization with BLNKB Input

FORCE Drive ALL ch with A-ch mode

If FORCA bit sets to '1', it is possible to enable or disable all PWM output pins through PWM outputs which occur from A-ch duty counter. It is noted that the inversion outputs of A, B, C channel have the same A-ch output waveform. According to POLA/B/C, it is able to control the inversion of outputs.

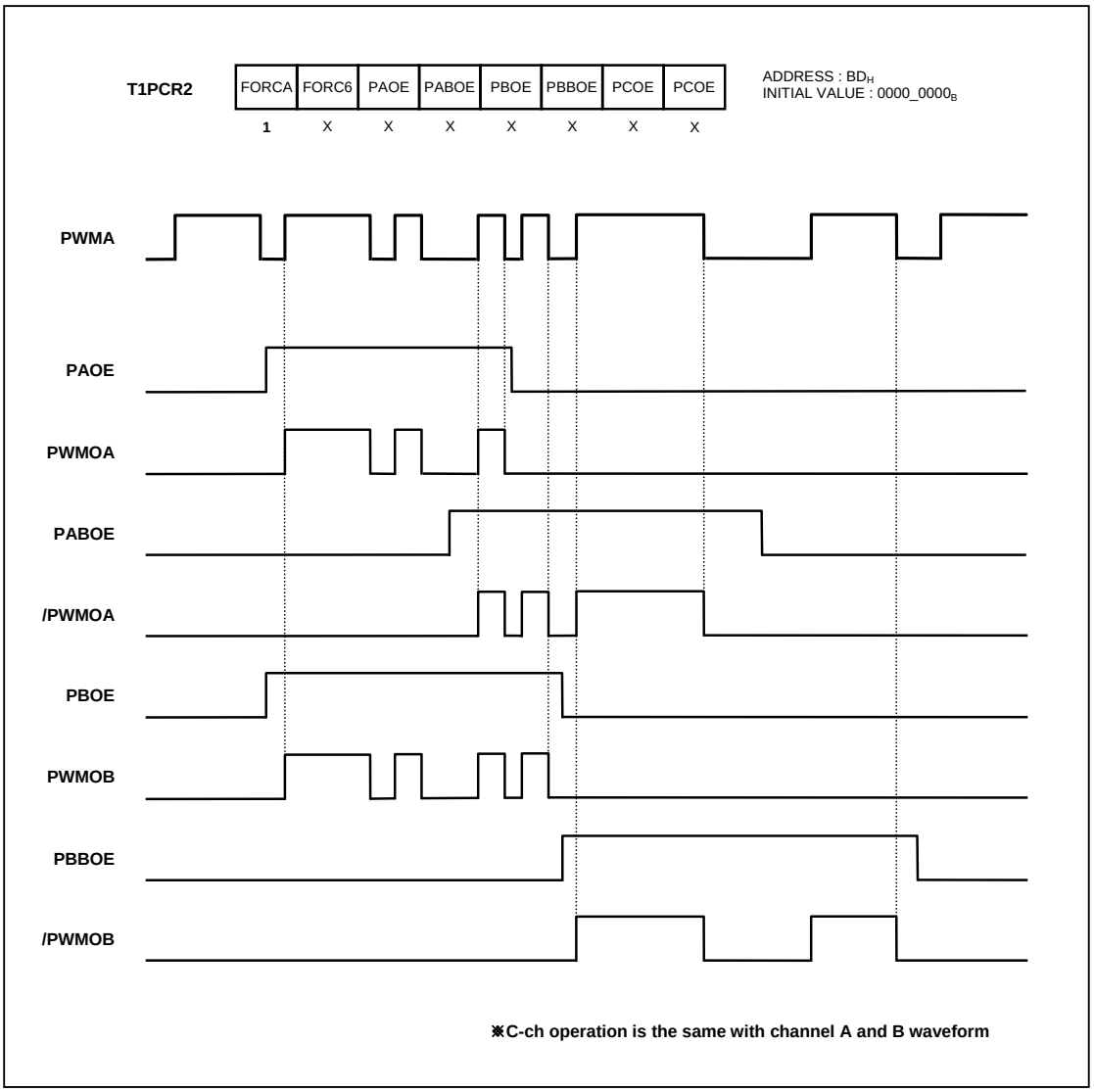

Figure 11-22 Example of Force Drive All-ch with A-ch

(T1CDR), Timer 1 PWM High Register (T1PHR), Timer 1 PWM Control Register 2 (T1PCR2), Timer 1 PWM Control Register 3 (T1PCR3), PWM1 Non-Overlap Delay Register ch. A/AB (T1DLYA), PWM1 Non-Overlap Delay Register ch. B/BB (T1DLYB), PWM1 Non-Overlap Delay Register ch. C/CB (T1DLYC), Timer 1 Interrupt Status Register (T1ISR), Timer 1 Interrupt Mask Register (T1IMSK) and PLL Control Register (PLLCR)

11.5.1.10 Register description for Timer/Counter 0, 1

T0CR (Timer 0 Mode Control Register) : B2H

7	6	5	4	3	2	1	0
T0EN	T0_PE	CAP0	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T0EN Control Timer 0
- 0 Timer 0 disable
- 1 Timer 0 enable

T0_PE Control Timer 0 Output port
- 0 Timer 0 Output disable
- 1 Timer 0 Output enable

CAP0 Control Timer 0 operation mode
- 0 Timer/Counter mode
- 1 Capture mode

T0CK[2:0] Select Timer 0 clock source. Fx is main system clock frequency

T0CK2	T0CK1	T0CK0	description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/32
1	0	0	fx/128
1	0	1	fx/512
1	1	0	fx/2048
1	1	1	External Clock (EC0)

T0CN Control Timer 0 Count pause/continue
- 0 Temporary count stop
- 1 Continue count

T0ST Control Timer 0 start/stop
- 0 Counter stop
- 1 Clear counter and start

T0 (Timer 0 Register: Read Case) : B3H

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00
R	R	R	R	R	R	R	R

Initial value : 00H

T0[7:0] T0 Counter

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PWM1E Control PWM
- 0 PWM disable
- 1 PWM enable

ESYNC Select the operation of External Sync Mode
- 0 External Sync Mode disable
- 1 External Sync Mode enable (using with BLNKB(P16))

BMOD Control Back-To-Back Mode operation
- 0 BtB mode disable (only up count)
- 1 BtB mode enable (Up/Down count)

PHLT Control PWM
- 0 PWM running
- 1 PWM stop

UPDT Determine the update time of PPR, PDR
- 0 Update at period match
- 1 Update at any time (after 3 timer clock, update)

UALL Control update all duty register
- 0 Write duty register separately
- 1 Write all duty registers (via A duty)

NOPS1[1:0] Select on-Overlap prescaler
Note) fpwm: PWM operation clock frequency

NOPS1	NOPS0	description
0	0	fpwm
0	1	fpwm/2
1	0	fpwm/4
1	1	fpwm/8

11.5.3.3 Register Map

Table 11-11 Register Map

Name	Address	Dir	Default	Description
T4CR	0xCE	R/W	00H	Timer 4 Mode Control Register
T4L	0xCF	R	00H	Timer 4 Low Register
T4LDR	0xCF	W	FFH	Timer 4 Low Data Register
LCDR4	0xCF	R	00H	Low Capture 4 Data Register
T4H	0xD5	R	00H	Timer 4 High Register
T4HDR	0xD5	R/W	00H	Timer 4 High Data Register
HCDR4	0xD5	R	00H	High Capture 4 Data Register

11.5.3.4 Timer 4 Register description

The timer 4 register consists of Timer 4 Mode Control Register (T4CR), Timer 4 Low Register (T4L), Timer 4 Low Data Register (T4LDR), Low Capture 4 Data Register (LCDR4), Timer 4 High Register (T4H), Timer 4 High Data Register (T4HDR), High Capture 4 Data Register (HCDR4).

11.5.3.5 Register description for Timer 4

T4CR (Timer 4 Mode Control Register) : CEH

7	6	5	4	3	2	1	0
T4EN	-	CAP4	T4CK2	T4CK1	T4CK0	T4CN	T4ST
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T4EN Control Timer 4 operation
- 0 Timer 4 disable
- 1 Timer 4 enable

CAP4 Control Timer 4 mode
- 0 Timer/Counter mode
- 1 Capture mode

T4CK[2:0] Select Timer 4 clock source. fx is main system clock frequency

T4CK2	T4CK1	T4CK0	Description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/16
1	0	0	fx/64
1	0	1	fx/256
1	1	0	fx/1024
1	1	1	fx/2048

T4CN Control Timer 4 Count pause/continue
- 0 Temporary count stop
- 1 Continue count

T4ST Control Timer 4 start/stop

11.6.3 Register Map

Table 11-13 Register Map

Name	Address	Dir	Default	Description
BUZDR	8FH	R/W	FFH	Buzzer Data Register
BUZCR	9FH	R/W	00H	Buzzer Control Register

11.6.4 Buzzer Driver Register description

Buzzer Driver consists of Buzzer Data Register (BUZDR), Buzzer Control Register (BUZCR).

11.6.5 Register description for Buzzer Driver

BUZDR (Buzzer Data Register) : 8FH

7	6	5	4	3	2	1	0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

BUZDR[7:0] This bits control the Buzzer frequency
Its resolution is 00H ~ FFH

BUZCR (Buzzer Control Register) : 9FH

7	6	5	4	3	2	1	0
-	-	-	-	-	BUCK1	BUCK0	BUZEN
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

BUCK[1:0] Buzzer Driver Source Clock Selection

BUCK1	BUCK0	Source Clock
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

BUZEN Buzzer Driver Operation Control

0	Buzzer Driver disable
1	Buzzer Driver enable

Note) fx: Main system clock oscillation frequency

11.8.5 Timing Waveform

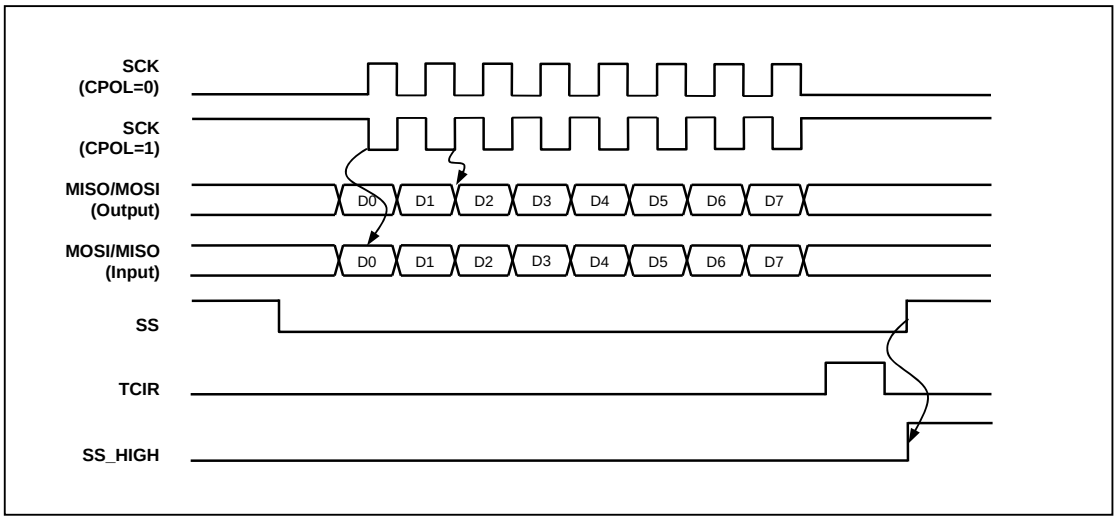

Figure 11-49 SPI Transmit/Receive Timing Diagram at CPHA = 0

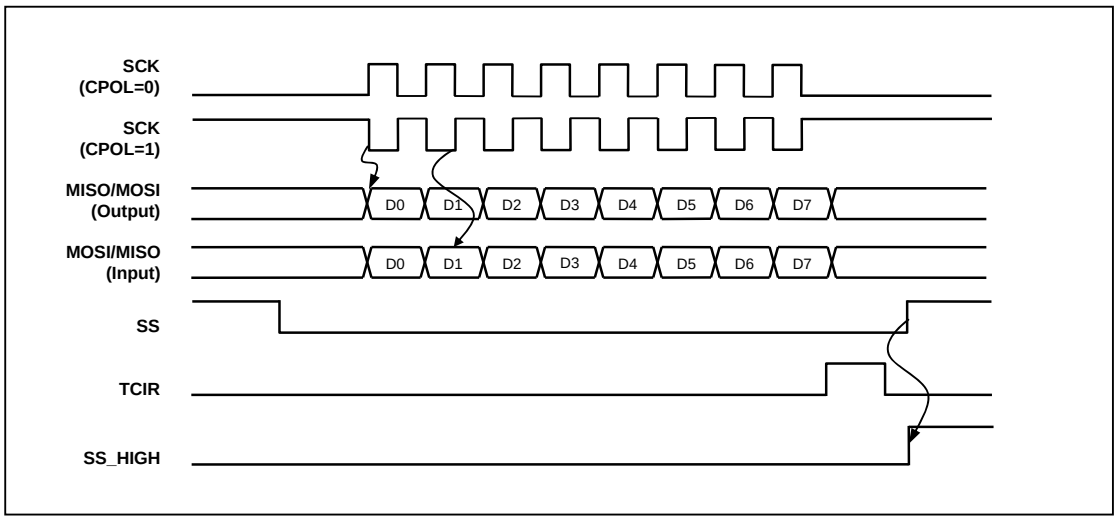

Figure 11-50 SPI Transmit/Receive Timing Diagram at CPHA = 1

11.8.6 Register Map

Table 11-18 Register Map

Name	Address	Dir	Default	Description
SPICR	D2H	R/W	0H	SPI Control Register
SPIDR	D3H	R/W	0H	SPI Data Register
SPISR	D4H	R/W	0H	SPI Status Register

11.8.7 SPI Register description

The SPI Register consists of SPI Control Register (SPICR), SPI Status Register (SPISR) and SPI Data Register (SPIDR)

I2CSAR (I^2C Slave Address Register) : D7H

7	6	5	4	3	2	1	0
SLA7	SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	GCALLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

SLA[7:1] These bits configure the slave address of this I^2C module when I^2C operates in slave mode.

GCALLEN This bit decides whether I^2C allows general call address or not when I^2C operates in slave mode.

0 Ignore general call address

1 Allow general call address

I2CSAR1 (I^2C Slave Address Register 1) : D6H

7	6	5	4	3	2	1	0
SLA7	SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	GCALLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

SLA[7:1] These bits configure the slave address of this I^2C module when I^2C operates in slave mode.

GCALLEN This bit decides whether I^2C allows general call address or not when I^2C operates in slave mode.

0 Ignore general call address

1 Allow general call address

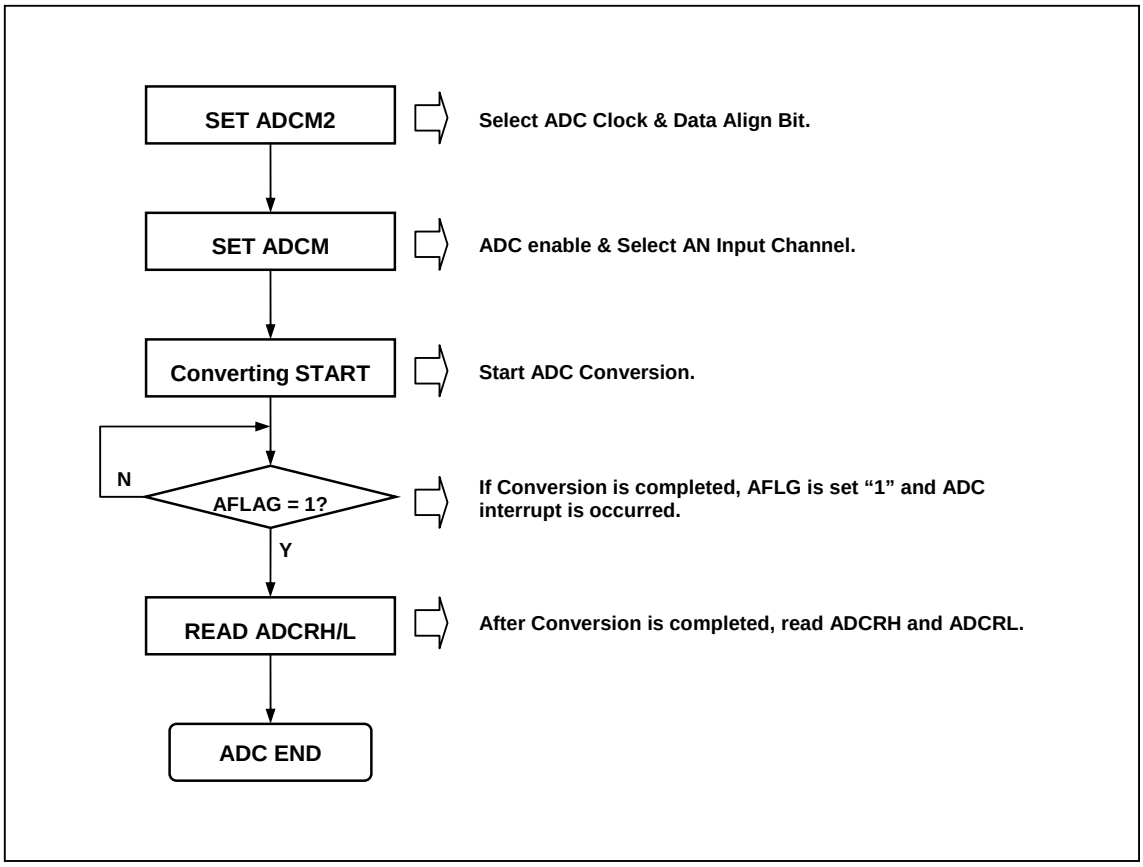

Figure 11-66 Converter Operation Flow

11.10.4 Register Map

Name	Address	Dir	Default	Description
ADCM	9AH	R/W	8FH	A/D Converter Mode Register
ADCRH	9BH	R	-	A/D Converter Result High Register
ADCRL	9CH	R	-	A/D Converter Result Low Register
ADCM2	9BH	R/W	8FH	A/D Converter Mode 2 Register

11.10.5 ADC Register description

The ADC Register consists of A/D Converter Mode Register (ADCM), A/D Converter Result High Register (ADCRH), A/D Converter Result Low Register (ADCRL), A/D Converter Mode 2 Register (ADCM2).

Note) when STBY bit is set to '1', ADCM2 can be read. If ADC enables, it is possible only to write ADCM2.When reading, ADCRH is read.

ADCRH (A/D Converter Result High Register) : 9BH

7	6	5	4	3	2	1	0
ADDM11	ADDM10	ADDM9	ADDM8	ADDM7 ADDL11	ADDM6 ADDL10	ADDM5 ADDL9	ADDM4 ADDL8
R	R	R	R	R	R	R	R

Initial value : xxH

ADDM[11:4] MSB align, A/D Converter High result (8-bit)
ADDL[11:8] LSB align, A/D Converter High result (4-bit)

ADCRL (A/D Converter Result Low Register) : 9CH

7	6	5	4	3	2	1	0
ADDM3 ADDL7	ADDM2 ADDL6	ADDM1 ADDL5	ADDM0 ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R	R	R	R

Initial value : xxH

ADDM[3:0] MSB align, A/D Converter Low result (4-bit)
ADDL[7:0] LSB align, A/D Converter Low result (8-bit)

11.11 Analog Comparator

11.11.1 Overview

The Analog Comparator compares the input values on the positive pin AC+ and the negative pin AC-. When the voltage on the positive pin AC+ is higher than the voltage on the negative pin AC-, the Analog Comparator output, ACOUT, is set.

11.11.2 Block Diagram

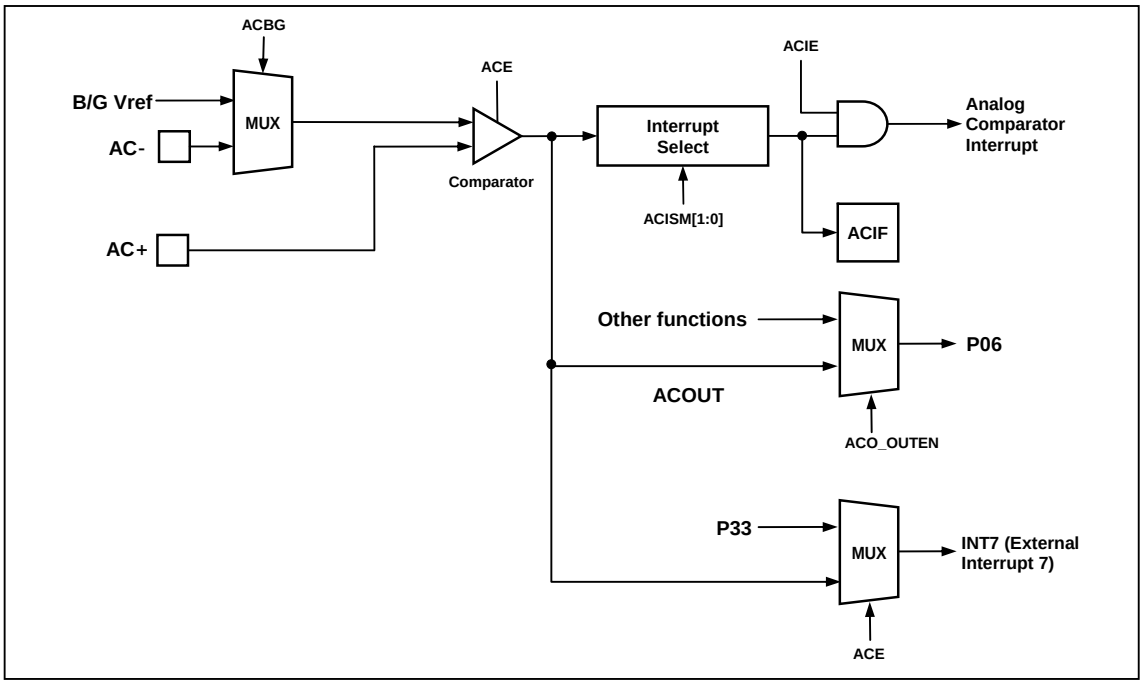

Figure 11-67 Analog Comparator Block Diagram

11.11.3 IN/OUT signal description

ACE : This enables Analog Comparator. When ACE is ‘0’, the output of Comparator goes LOW.

BGR : Band Gap Reference Voltage

ACBG : This selects (-) input source between BGR and AC-. When ACBG is ‘1’, the (-) input to AC is BGR.

AC- : This can be (-) input to the AC, and comes directly from external analog pad.

AC+ : This can be (+) input to the AC, and comes directly from external analog pad.

AMUXENB : This selects (+) input source between multiplexed output of ADC and AN5. AMUXENB is the inverted signal of AMUXEN bit in ADCM2 register. When AMUXENB is ‘0’, the (+) input to AC comes from ADC module which is selected by ADSEL[3:0], the channel selection bits in ADCM register.

ACOUT : This is the output of Comparator.

ACO_OUTEN : Analog Comparator output port Enable.

15. Memory Programming

15.1 Overview

15.1.1 Description

Z51F0811 incorporates flash and data EEPROM memory to which a program can be written, erased, and overwritten while mounted on the board. Also, data EEPROM can be programmed or erased in user program. Flash area can be programmed in only OCD or parallel ROM mode.

Serial ISP modes and byte-parallel ROM writer mode are supported.

15.1.2 Features

- Flash Size : 8Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Up to 100,000 program/erase cycles at typical voltage and temperature for data EEPROM memory
- Security feature

15.2 Flash and EEPROM Control and status register

Registers to control Flash and Data EEPROM are Mode Register (FEMR), Control Register (FECR), Status Register (FESR), Time Control Register (FETCR), Address Low Register (FEARL), Address Middle Register (FEARM), address High Register (FEARH) and Data Register (FEDR). They are mapped to SFR area and can be accessed only in programming mode.

15.2.1 Register Map

Table 15-1 Register Map

Name	Address	Dir	Default	Description
FEMR	EAH	R/W	00H	Flash and EEPROM Mode Register
FECR	EBH	R/W	03H	Flash and EEPROM Control Register
FESR	ECH	R/W	80H	Flash and EEPROM Status Register
FETCR	EDH	R/W	00H	Flash and EEPROM Time Control Register
FEARL	F2H	R/W	00H	Flash and EEPROM Address Low Register
FEARM	F3H	R/W	00H	Flash and EEPROM Address Middle Register
FEARH	F4H	R/W	00H	Flash and EEPROM Address High Register
FEDR	F5H	R/W	00H	Flash and EEPROM Data Register

FECR (Flash and EEPROM Control Register) : EBH

7	6	5	4	3	2	1	0
AEF	AEE	EXIT1	EXIT0	WRITE	READ	nFERST	nPBRST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 03H

AEF Enable flash bulk erase mode

0 Disable bulk erase mode of Flash memory

1 Enable bulk erase mode of Flash memory

AEE Enable data EEPROM bulk erase mode

0 Disable bulk erase mode of data EEPROM

1 Enable bulk erase mode of data EEPROM

EXIT[1:0] Exit from program mode. It is cleared automatically after 1 clock

EXIT1	EXIT0	Description
0	0	Don't exit from program mode
0	1	Don't exit from program mode
1	0	Don't exit from program mode
1	1	Exit from program mode

WRITE Start to program or erase of Flash and data EEPROM. It is cleared automatically after 1 clock

0 No operation

1 Start to program or erase of Flash and data EEPROM

READ Start auto-verify of Flash or data EEPROM. It is cleared automatically after 1 clock

0 No operation

1 Start auto-verify of Flash or data EEPROM

nFERST Reset Flash or data EEPROM control logic. It is cleared automatically after 1 clock

0 No operation

1 Reset Flash or data EEPROM control logic.

nPBRST Reset page buffer with PBUFF. It is cleared automatically after 1 clock

PBUFF	nPBRST	Description
0	0	Page buffer reset
1	0	Write checksum reset

WRITE and READ bits can be used in program, erase and verify mode with FEAR registers. Read or writes for memory cell or page buffer uses read and write enable signals from memory controller. Indirect address mode with FEAR is only allowed to program, erase and verify

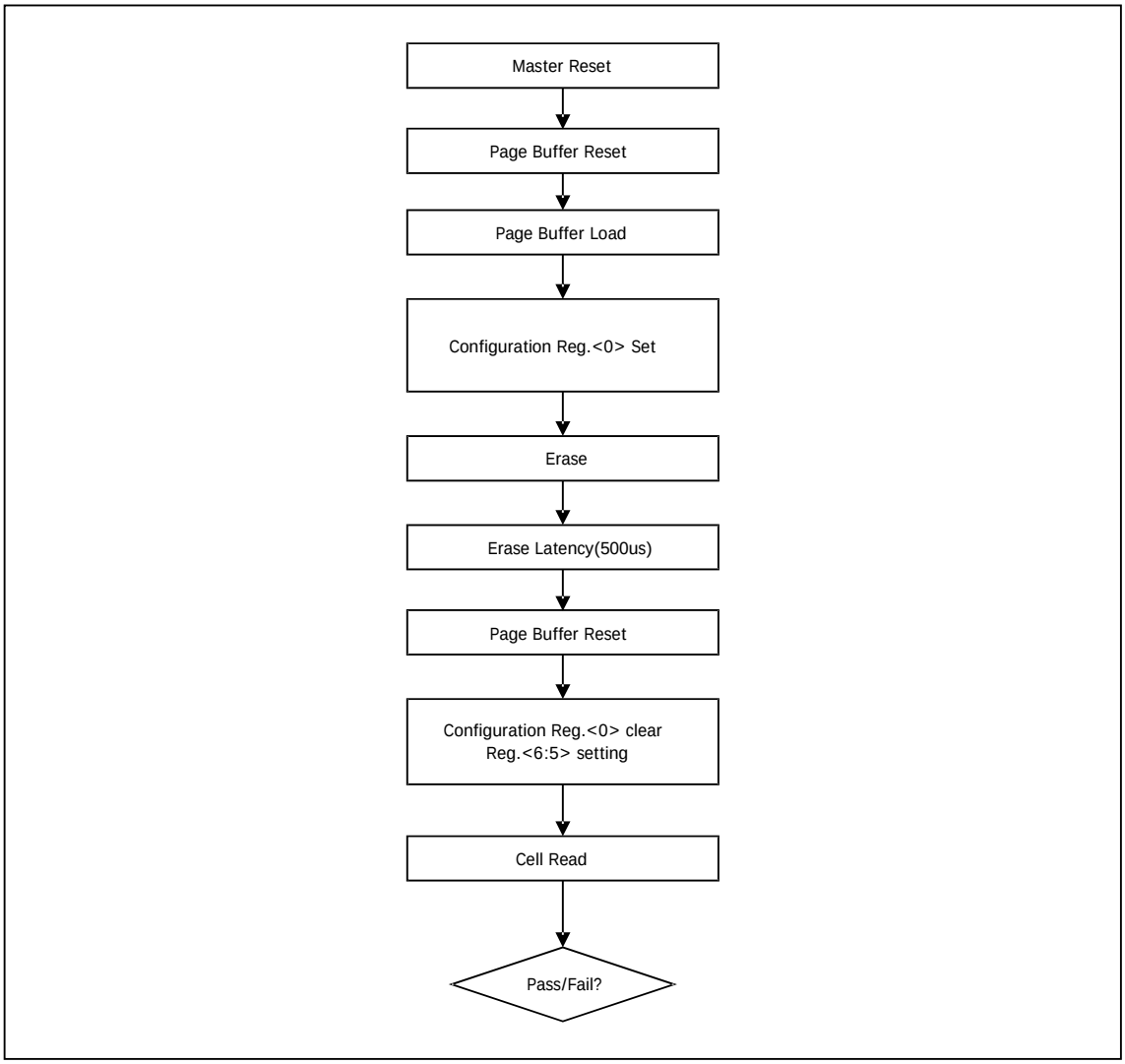

Figure 15-6 The sequence of bulk erase of Flash memory

15.4.1.1 Flash Read

Step 1. Enter OCD(=ISP) mode.
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Read data from Flash.

15.4.1.2 Enable program mode

Step 1. Enter OCD(=ISP) mode.[1]
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Enter program/erase mode sequence.[2]
(1) Write 0xAA to 0xF555.

15.5 Parallel Mode

15.5.1 Overview

Parallel program mode transfers address and data by byte. 3-byte address can be entered by one from the lease significant byte of address. If only LSB is changed, only one byte can be transferred. And if the second byte is changed, the first and second byte can be transferred. Upper 4-bit of the most significant byte selects memory to be accessed. Table 15-4 shows memory type to be accessible by parallel mode. Address auto-increment is supported when read or write data without address.

The erase and program sequence of Flash and data EEPROM is identical to that of ISP mode except the entrance of parallel mode . Refer to Table 15-5 for the entrance method for parallel mode.

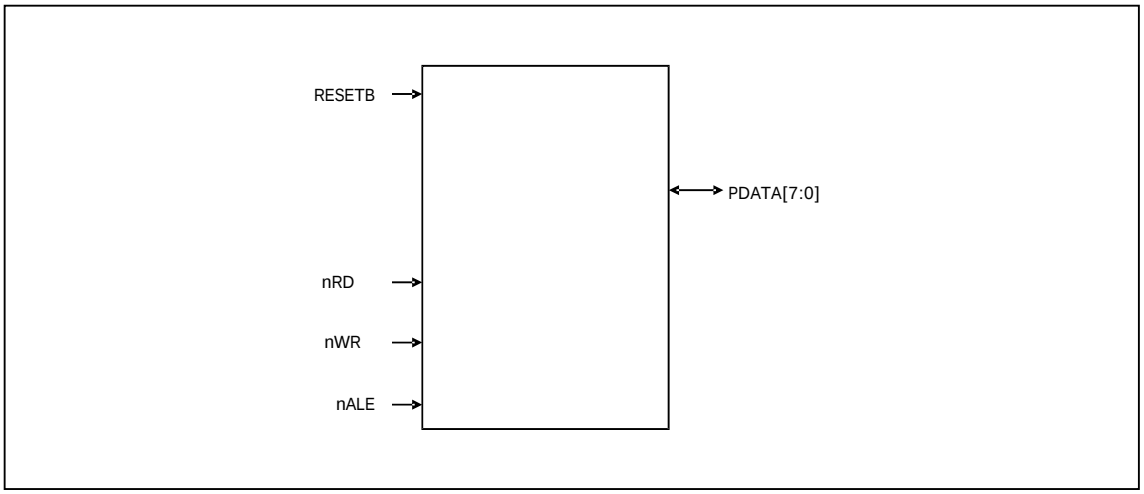

Figure 15-7 Pin diagram for parallel programming

Table 15-4 The selection of memory type by ADDRH[7:4]

ADDRH[7:4]				Memory Type
0	0	0	0	Program Memory
0	0	0	1	External Memory
0	0	1	0	SFR

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