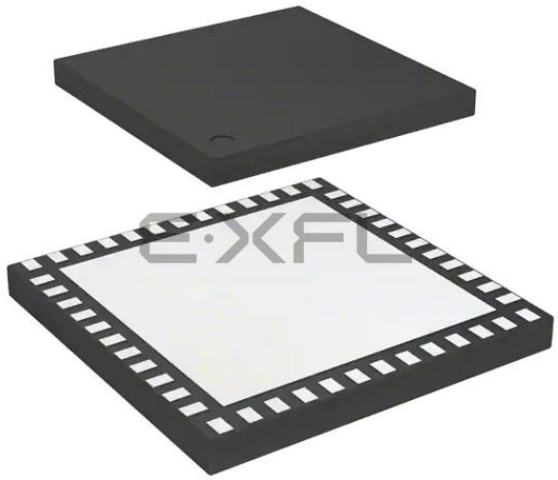

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFLGA Exposed Pad
Supplier Device Package	48-TLLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l016-d3ht

7.7.11 Mode Register

Name: MR

Access Type: Read/Write

Offset: 0x018 + n*0x040

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	RING	ETRIG	SIZE	

- **RING: Ring Buffer**
  0:The Ring buffer functionality is disabled.
  1:The Ring buffer functionality is enabled. When enabled, the reload registers, MARR and TCRR will not be cleared after reload.
- **ETRIG: Event Trigger**
  0:Start transfer when the peripheral selected in Peripheral Select Register (PSR) requests a transfer.
  1:Start transfer only when or after a peripheral event is received.
- **SIZE: Size of Transfer**

Table 7-5. Size of Transfer

SIZE	Size of Transfer
0	Byte
1	Halfword
2	Word
3	Reserved

9.4 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

9.4.1 Power Management

If the CPU enters a sleep mode that disables clocks used by the SAU, the SAU will stop functioning and resume operation after the system wakes up from sleep mode.

9.4.2 Clocks

The SAU has two bus clocks connected: One High Speed Bus clock (CLK_SAU_HSB) and one Peripheral Bus clock (CLK_SAU_PB). These clocks are generated by the Power Manager. Both clocks are enabled at reset, and can be disabled by writing to the Power Manager. The user has to ensure that CLK_SAU_HSB is not turned off before accessing the SAU. Likewise, the user must ensure that no bus access is pending in the SAU before disabling CLK_SAU_HSB. Failing to do so may deadlock the High Speed Bus.

9.4.3 Interrupt

The SAU interrupt request line is connected to the interrupt controller. Using the SAU interrupt requires the interrupt controller to be programmed first.

9.4.4 Debug Operation

When an external debugger forces the CPU into debug mode, the SAU continues normal operation. If the SAU is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

9.5 Functional Description

9.5.1 Enabling the SAU

The SAU is enabled by writing a one to the Enable (EN) bit in the Control Register (CR). This will set the SAU Enabled (EN) bit in the Status Register (SR).

9.5.2 Configuring the SAU Channels

The SAU has a set of channels, mapped in the HSB memory space. These channels can be configured by a Remap Target Register (RTR), located at the same memory address. When the SAU is in normal mode, the SAU channel is addressed, and when the SAU is in setup mode, the RTR can be addressed.

Before the SAU can be used, the channels must be configured and enabled. To configure a channel, the corresponding RTR must be programmed with the Remap Target Address. To do this, make sure the SAU is in setup mode by writing a one to the Setup Mode Enable (SEN) bit in CR. This makes sure that a write to the RTR address accesses the RTR, not the SAU channel. Thereafter, the RTR is written with the address to remap to, typically the address of a specific PB register. When all channels have been configured, return to normal mode by writing a one to the Setup Mode Disable (SDIS) in CR. The channels can now be enabled by writing ones to the corresponding bits in the Channel Enable Registers (CERH/L).

The SAU is only able to remap addresses above 0xFFFC0000.

18.4 I/O Lines Description

Pin Name	Description	Type
GPIOn	GPIO pin n	Digital

18.5 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

18.5.1 Power Management

If the CPU enters a sleep mode that disables clocks used by the GPIO, the GPIO will stop functioning and resume operation after the system wakes up from sleep mode.

If a peripheral function is configured for a GPIO pin, the peripheral will be able to control the GPIO pin even if the GPIO clock is stopped.

18.5.2 Clocks

The GPIO is connected to a Peripheral Bus clock (CLK_GPIO). This clock is generated by the Power Manager. CLK_GPIO is enabled at reset, and can be disabled by writing to the Power Manager. CLK_GPIO must be enabled in order to access the configuration registers of the GPIO or to use the GPIO interrupts. After configuring the GPIO, the CLK_GPIO can be disabled by writing to the Power Manager if interrupts are not used.

If the CPU Local Bus is used to access the configuration interface of the GPIO, the CLK_GPIO must be equal to the CPU clock to avoid data loss.

18.5.3 Interrupts

The GPIO interrupt request lines are connected to the interrupt controller. Using the GPIO interrupts requires the interrupt controller to be programmed first.

18.5.4 Peripheral Events

The GPIO peripheral events are connected via the Peripheral Event System. Refer to the Peripheral Event System chapter for details.

18.5.5 Debug Operation

When an external debugger forces the CPU into debug mode, the GPIO continues normal operation. If the GPIO is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

19. Universal Synchronous Asynchronous Receiver Transmitter (USART)

Rev: 4.4.0.6

19.1 Features

- Configurable baud rate generator
- 5- to 9-bit full-duplex, synchronous and asynchronous, serial communication
  - 1, 1.5, or 2 stop bits in asynchronous mode, and 1 or 2 in synchronous mode
  - Parity generation and error detection
  - Framing- and overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - Receiver frequency over-sampling by 8 or 16 times
  - Optional RTS-CTS hardware handshaking
  - Receiver Time-out and transmitter Timeguard
  - Optional Multidrop mode with address generation and detection
- SPI Mode
  - Master or slave
  - Configurable serial clock phase and polarity
  - CLK SPI serial clock frequency up to a quarter of the CLK_USART internal clock frequency
- LIN Mode
  - Compliant with LIN 1.3 and LIN 2.0 specifications
  - Master or slave
  - Processing of Frames with up to 256 data bytes
  - Configurable response data length, optionally defined automatically by the Identifier
  - Self synchronization in slave node configuration
  - Automatic processing and verification of the “Break Field” and “Sync Field”
  - The “Break Field” is detected even if it is partially superimposed with a data byte
  - Optional, automatic identifier parity management
  - Optional, automatic checksum management
  - Supports both “Classic” and “Enhanced” checksum types
  - Full LIN error checking and reporting
  - Frame Slot Mode: the master allocates slots to scheduled frames automatically.
  - Wakeup signal generation
- Test Modes
  - Automatic echo, remote- and local loopback
- Supports two Peripheral DMA Controller channels
  - Buffer transfers without processor intervention

19.2 Overview

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides a full duplex, universal, synchronous/asynchronous serial link. Data frame format is widely configurable, including basic length, parity, and stop bit settings, maximizing standards support. The receiver implements parity-, framing-, and overrun error detection, and can handle un-fixed frame lengths with the time-out feature. The USART supports several operating modes, providing an interface to, LIN, and SPI buses and infrared transceivers. Communication with slow and remote devices is eased by the timeguard. Duplex multidrop communication is supported by address and data differentiation through the parity bit. The hardware handshaking feature enables an out-of-band flow control, automatically managing RTS and CTS pins. The Peripheral DMA Controller connection enables memory transactions, and the USART supports chained

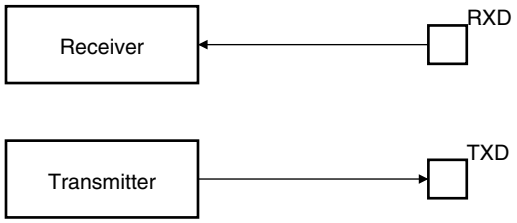
19.6.11 Test Modes

The internal loopback feature enables on-board diagnostics, and allows the USART to operate in three different test modes, with reconfigured pin functionality, as shown below.

19.6.11.1 Normal Mode

During normal operation, a receivers RXD pin is connected to a transmitters TXD pin.

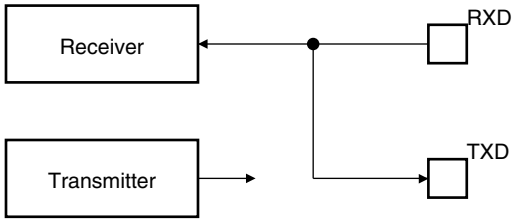
Figure 19-36. Normal Mode Configuration



19.6.11.2 Automatic Echo Mode

Automatic echo mode allows bit-by-bit retransmission. When a bit is received on the RXD pin, it is also sent to the TXD pin, as shown in Figure 19-37. Transmitter configuration has no effect.

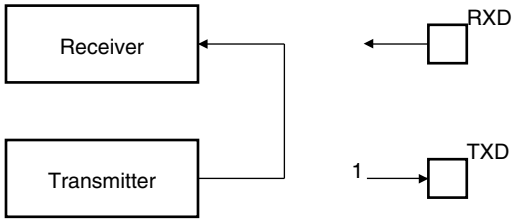
Figure 19-37. Automatic Echo Mode Configuration



19.6.11.3 Local Loopback Mode

Local loopback mode connects the output of the transmitter directly to the input of the receiver, as shown in Figure 19-38. The TXD and RXD pins are not used. The RXD pin has no effect on the receiver and the TXD pin is continuously driven high, as in idle state.

Figure 19-38. Local Loopback Mode Configuration



19.6.11.4 Remote Loopback Mode

Remote loopback mode connects the RXD pin to the TXD pin, as shown in Figure 19-39. The transmitter and the receiver are disabled and have no effect. This mode allows bit-by-bit retransmission.

- **CHRL: Character Length.**

Table 19-14.

CHRL		Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- **USCLKS: Clock Selection**

Table 19-15.

USCLKS		Selected Clock
0	0	CLK_USART
0	1	CLK_USART/DIV(1)
1	0	Reserved
1	1	CLK

Note: 1. The value of DIV is device dependent. Please refer to the Module Configuration section at the end of this chapter.

- **MODE**

Table 19-16.

MODE				Mode of the USART
0	0	0	0	Normal
0	0	1	0	Hardware Handshaking
1	0	1	0	LIN Master
1	0	1	1	LIN Slave
1	1	1	0	SPI Master
1	1	1	1	SPI Slave
Others				Reserved

20.8.4 Transmit Data Register

Name: TDR

Access Type: Write-only

Offset: 0x0C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	LASTXFER

23	22	21	20	19	18	17	16
-	-	-	-	PCS			

15	14	13	12	11	10	9	8
TD[15:8]							

7	6	5	4	3	2	1	0
TD[7:0]							

- **LASTXFER: Last Transfer**

  1: The current NPCS will be deasserted after the character written in TD has been transferred. When CSRn.CSAAT is one, this allows to close the communication with the current serial peripheral by raising the corresponding NPCS line as soon as TD transfer has completed.
  0: Writing a zero to this bit has no effect.

  This field is only used if Variable Peripheral Select is active (MR.PS = 1).

- **PCS: Peripheral Chip Select**

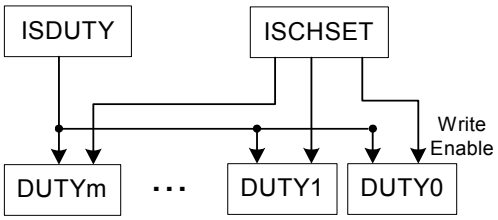
  If PCSDEC = 0:
  PCS = xxx0NPCS[3:0] = 1110
  PCS = xx01NPCS[3:0] = 1101
  PCS = x011NPCS[3:0] = 1011
  PCS = 0111NPCS[3:0] = 0111
  PCS = 1111forbidden (no peripheral is selected)
  (x = don't care)
  If PCSDEC = 1:
  NPCS[3:0] output signals = PCS

  This field is only used if Variable Peripheral Select is active (MR.PS = 1).

- **TD: Transmit Data**

  Data to be transmitted by the SPI Interface is stored in this register. Information to be transmitted must be written to the TDR register in a right-justified format.

Figure 23-3. Interlinked Single Value PWM Operation Flow

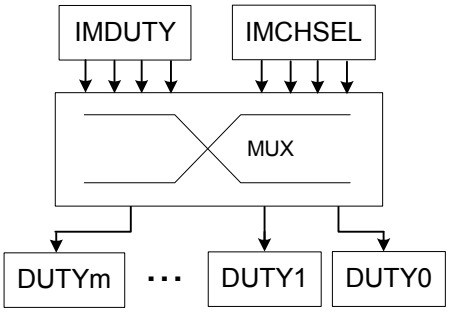


23.6.5.2 Interlinked Multiple Value PWM Operation

The interlinked multiple value PWM operation allows up to four channels to be updated simultaneously with different duty cycle values. These duty cycle values must be written to the IMDUTY register. The index number of the four channels to be updated is written to the four SEL fields in the Interlinked Multiple Value Channel Select (IMCHSEL) register (IMCHSEL.SEL). When the IMCHSEL register is written, the values stored in the IMDUTY register are synchronized to the duty cycle registers for the channels selected by the SEL fields. Figure 23-4 on page 524 shows the writing procedure.

Note that only writes to the implemented channels will be effective. If one of the IMCHSEL.SEL fields points to a non-existing channel, the corresponding value in the IMDUTY register will not be written. If the same channel is specified in multiple IMCHSEL.SEL fields, the channel will be updated with the value stored in the corresponding upper field of the IMDUTY register.

Figure 23-4. Interlinked Multiple Value PWM Operation Flow



23.6.6 Open Drain Mode

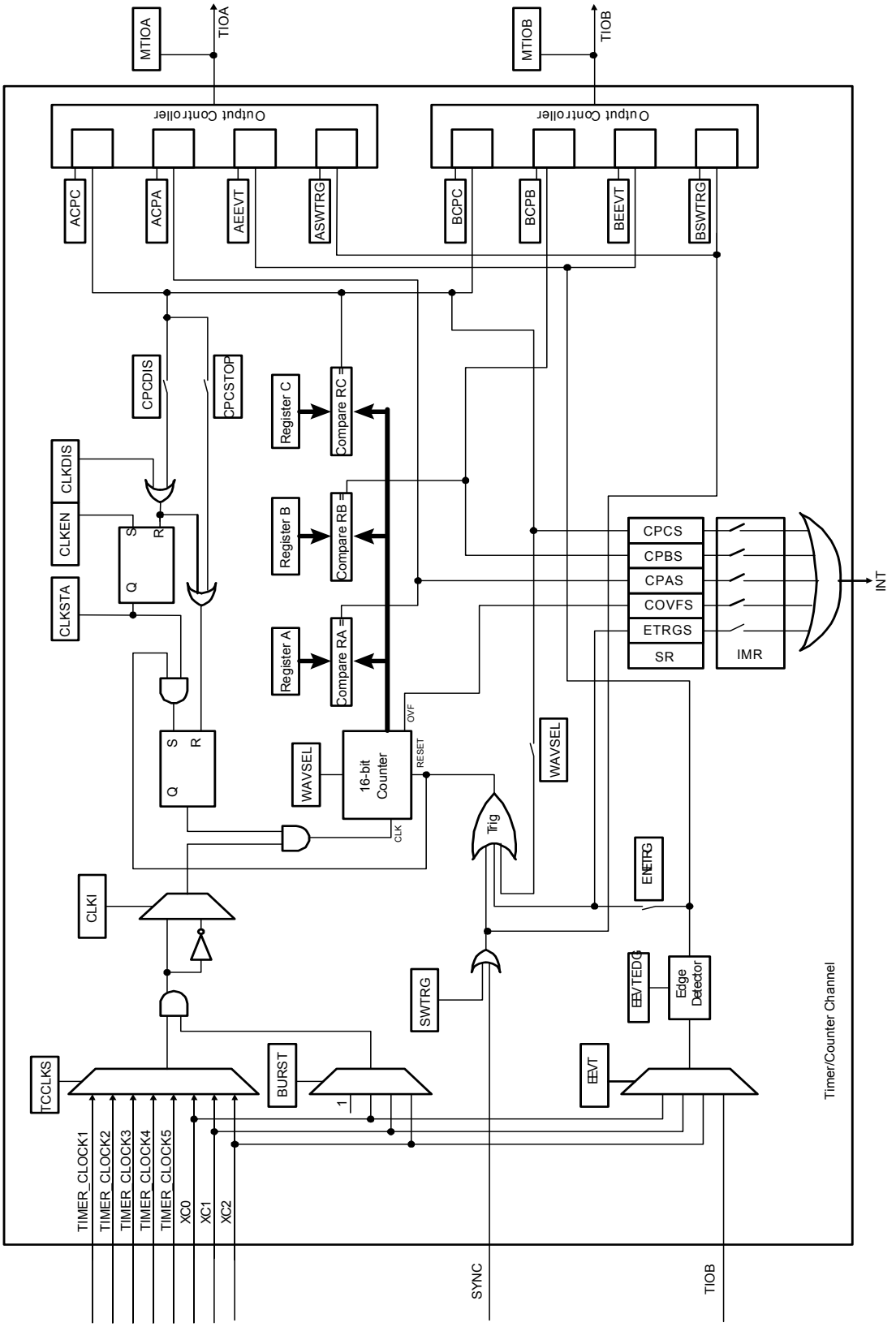
Some pins can be used in open drain mode, allowing the PWMA waveform to toggle between 0V and up to 5V on these pins. In this mode the PWMA will drive the pin to zero or leave the output open. An external pullup can be used to pull the pin up to the desired voltage.

To enable open drain mode on a pin the PWMAOD function must be selected instead of the PWMA function in the I/O Controller. Please refer to the Module Configuration chapter for information about which pins are available in open drain mode.

23.6.7 Synchronization

Both the timebase counter and the spread spectrum counter can be reset and the duty cycle registers can be written through the user interface of the module. This requires a synchronization between the PB and GCLK clock domains, which takes a few clock cycles of each clock domain. The BUSY bit in SR indicates when the synchronization is ongoing. Writing to the module while the BUSY bit is set will result in discarding the new value.

Figure 24-5. Waveform Mode



26.9.7 Interrupt Status Register

Name: ISR

Access Type: Read-only

Offset: 0x18

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	CELSE	CGT	CLT	-	-	BUSY	READY
7	6	5	4	3	2	1	0
-	-	NOCNT	PENCNT	-	-	OVRE	DRDY

- **CELSE: Compare Else Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **CGT: Compare Greater Than Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **CLT: Compare Lesser Than Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **BUSY: Busy Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **READY: Ready Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **NOCNT: No Contact Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **PENCNT: Pen Contact Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **OVRE: Overrun Error Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when the corresponding bit in SR has a zero-to-one transition.
- **DRDY: Data Ready Status**
  This bit is cleared when the corresponding bit in ICR is written to one.
  This bit is set when a conversion has completed and new data is available in LCDR.

27.9.7 Interrupt Status Clear Register

Name: ICR

Access Type: Write-only

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	WFINT3	WFINT2	WFINT1	WFINT0
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
SUTINT7	ACINT7	SUTINT6	ACINT6	SUTINT5	ACINT5	SUTINT4	ACINT4
7	6	5	4	3	2	1	0
SUTINT3	ACINT3	SUTINT2	ACINT2	SUTINT1	ACINT1	SUTINT0	ACINT0

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in ISR and the corresponding interrupt request.

Table 28-3. CAT Register Memory Map

Offset	Register	Register Name	Access	Reset
0x98	Analog Comparator Shift Offset Register 6	ACSHI6	Read/Write	0x00000000
0x9C	Analog Comparator Shift Offset Register 7	ACSHI7	Read/Write	0x00000000
0xF8	Parameter Register	PARAMETER	Read-only	
0xFC	Version Register	VERSION	Read-only	

28.7.27 Analog Comparator Shift Offset Register x

Name: ACSHIx

Access Type: Read/Write

Offset: 0x80, 0x84, 0x88, 0x8C, 0x90, 0x94, 0x98, and 0x9C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-							

23	22	21	20	19	18	17	16
-							

15	14	13	12	11	10	9	8
-				SHIVAL[11:8]			

7	6	5	4	3	2	1	0
SHIVAL[7:0]							

- **SHIVAL: Shift Offset Value**
  Specifies the amount to shift the count value from each comparator. This allows the offset of each comparator to be compensated.

Table 31-1. SAB Slaves, Addresses and Descriptions

Slave	Address [35:32]	Description
HSB	0x5	Alternative mapping for HSB space, for compatibility with other 32-bit AVR devices.
Memory Service Unit	0x6	Memory Service Unit registers
Reserved	Other	Unused

31.2.2 SAB Security Restrictions

The Service Access bus can be restricted by internal security measures. A short description of the security measures are found in the table below.

31.2.2.1 Security measure and control location

A security measure is a mechanism to either block or allow SAB access to a certain address or address range. A security measure is enabled or disabled by one or several control signals. This is called the control location for the security measure.

These security measures can be used to prevent an end user from reading out the code programmed in the flash, for instance.

Table 31-2. SAB Security Measures

Security Measure	Control Location	Description
Secure mode	FLASHCDW SECURE bits set	Allocates a portion of the flash for secure code. This code cannot be read or debugged. The User page is also locked.
Security bit	FLASHCDW security bit set	Programming and debugging not possible, very restricted access.
User code programming	FLASHCDW UPROT + security bit set	Restricts all access except parts of the flash and the flash controller for programming user code. Debugging is not possible unless an OS running from the secure part of the flash supports it.

Below follows a more in depth description of what locations are accessible when the security measures are active.

Table 31-3. Secure Mode SAB Restrictions

Name	Address Start	Address End	Access
Secure flash area	0x580000000	0x580000000 + (USERPAGE[15:0] << 10)	Blocked
Secure RAM area	0x500000000	0x500000000 + (USERPAGE[31:16] << 10)	Blocked
User page	0x580800000	0x581000000	Read
Other accesses	-	-	As normal

Note: 1. Second Word of the User Page, refer to the Fuses Settings section for details.

Table 31-23. MEMORY_BLOCK_ACCESS Details (Continued)

Instructions	Details
DR input value (Data write phase)	**dddddddd dddddddd dddddddd dddddddd** xx
DR output value (Data read phase)	eb **dddddddd dddddddd dddddddd dddddddd**
DR output value (Data write phase)	xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

The overhead using block word access is 4 cycles per 32 bits of data, resulting in an 88% transfer efficiency, or 2.1 MBytes per second with a 20 MHz TCK frequency.

31.5.3.6 CANCEL_ACCESS

If a very slow memory location is accessed during a SAB memory access, it could take a very long time until the busy bit is cleared, and the SAB becomes ready for the next operation. The CANCEL_ACCESS instruction provides a possibility to abort an ongoing transfer and report a timeout to the JTAG master.

When the CANCEL_ACCESS instruction is selected, the current access will be terminated as soon as possible. There are no guarantees about how long this will take, as the hardware may not always be able to cancel the access immediately. The SAB is ready to respond to a new command when the busy bit clears.

Starting in Run-Test/Idle, CANCEL_ACCESS is accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.

Table 31-24. CANCEL_ACCESS Details

Instructions	Details
IR input value	**10011** (0x13)
IR output value	peb01
DR Size	1
DR input value	x
DR output value	0

31.5.3.7 SYNC

This instruction allows external debuggers and testers to measure the ratio between the external JTAG clock and the internal system clock. The SYNC data register is a 16-bit counter that counts down to zero using the internal system clock. The busy bit stays high until the counter reaches zero.

Starting in Run-Test/Idle, SYNC instruction is used in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.

32.5 I/O Pin Characteristics

Table 32-7. Normal I/O Pin Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance		75	100	145	kOhm
V_{IL}	Input low-level voltage	V_{VDD} = 3.0V	-0.3		0.3*V_{VDD}	V
		V_{VDD} = 1.62V	-0.3		0.3*V_{VDD}	
V_{IH}	Input high-level voltage	V_{VDD} = 3.6V	0.7*V_{VDD}		V_{VDD} + 0.3	V
		V_{VDD} = 1.98V	0.7*V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage	V_{VDD} = 3.0V, I_{OL} = 3mA			0.4	V
		V_{VDD} = 1.62V, I_{OL} = 2mA			0.4	
V_{OH}	Output high-level voltage	V_{VDD} = 3.0V, I_{OH} = 3mA	V_{VDD} - 0.4			V
		V_{VDD} = 1.62V, I_{OH} = 2mA	V_{VDD} - 0.4			
f_{MAX}	Output frequency[2]	V_{VDD} = 3.0V, load = 10pF			45	MHz
		V_{VDD} = 3.0V, load = 30pF			23	
t_{RISE}	Rise time[2]	V_{VDD} = 3.0V, load = 10pF			4.7	ns
		V_{VDD} = 3.0V, load = 30pF			11.5	
t_{FALL}	Fall time[2]	V_{VDD} = 3.0V, load = 10pF			4.8	
		V_{VDD} = 3.0V, load = 30pF			12	
I_{LEAK}	Input leakage current	Pull-up resistors disabled			1	µA
C_{IN}	Input capacitance, all normal I/O pins except PA05, PA07, PA17, PA20, PA21, PB04, PB05	TQFP48 package		1.4		pF
		QFN48 package		1.1		
		TLLGA 48 package		1.1		
C_{IN}	Input capacitance, PA20	TQFP48 package		2.7		
		QFN48 package		2.4		
		TLLGA 48 package		2.4		
C_{IN}	Input capacitance, PA05, PA07, PA17, PA21, PB04, PB05	TQFP48 package		3.8		
		QFN48 package		3.5		
		TLLGA 48 package		3.5		

Notes: 1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3.2 on page 9 for details.
2. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

Table 32-8. High-drive I/O Pin Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance	PA06	30	50	110	kOhm
		PA02, PB01, RESET	75	100	145	
		PA08, PA09	10	20	45	

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. Please refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. Please refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

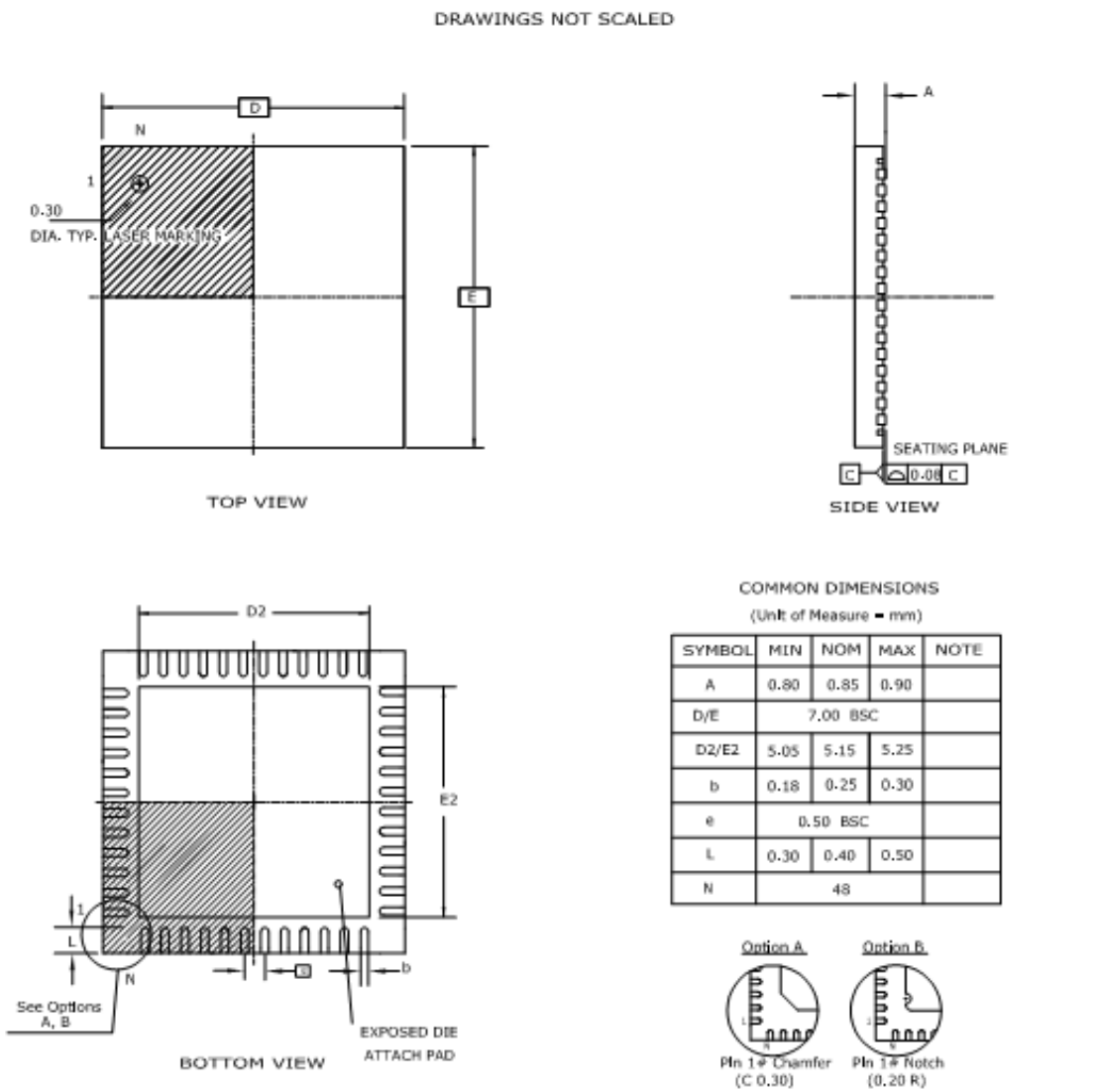
32.9.5 TWIM/TWIS Timing

Figure 32-42 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. Please refer to the TWIM and TWIS sections for more information.

Table 32-42. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		

Figure 33-2. QFN-48 Package Drawing



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

07/27/2011

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 33-5. Device and Package Maximum Weight

140	mg

Table 33-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 33-7. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	E3

- Disable RC32K by writing a zero to SCIF.RC32KCR.EN, and wait for this bit to be read as zero.

35.2.5 AST

1. **Reset may set status bits in the AST**
   If a reset occurs and the AST is enabled, the SR.ALARM0, SR.PER0, and SR.OVF bits may be set.
   Fix/Workaround
   If the part is reset and the AST is used, clear all bits in the Status Register before entering sleep mode.

2. **AST wake signal is released one AST clock cycle after the BUSY bit is cleared**
   After writing to the Status Clear Register (SCR) the wake signal is released one AST clock cycle after the BUSY bit in the Status Register (SR.BUSY) is cleared. If entering sleep mode directly after the BUSY bit is cleared the part will wake up immediately.
   Fix/Workaround
   Read the Wake Enable Register (WER) and write this value back to the same register. Wait for BUSY to clear before entering sleep mode.

35.2.6 WDT

1. **Clearing the Watchdog Timer (WDT) counter in second half of timeout period will issue a Watchdog reset**
   If the WDT counter is cleared in the second half of the timeout period, the WDT will immediately issue a Watchdog reset.
   Fix/Workaround
   Use twice as long timeout period as needed and clear the WDT counter within the first half of the timeout period. If the WDT counter is cleared after the first half of the timeout period, you will get a Watchdog reset immediately. If the WDT counter is not cleared at all, the time before the reset will be twice as long as needed.

2. **WDT Control Register does not have synchronization feedback**
   When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.
   Fix/Workaround
   -When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
   -When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

35.2.7 GPIO

1. **Clearing GPIO interrupt may fail**
   Writing a one to the GPIO.IFRC register to clear an interrupt will be ignored if interrupt is enabled for the corresponding port.
   Fix/Workaround
   Disable the interrupt, clear it by writing a one to GPIO.IFRC, then enable the interrupt.