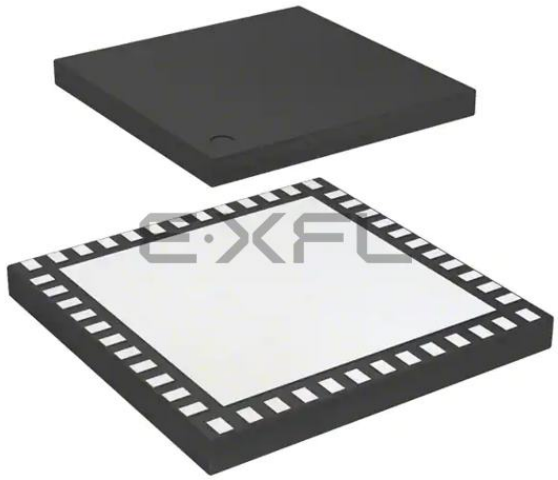

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

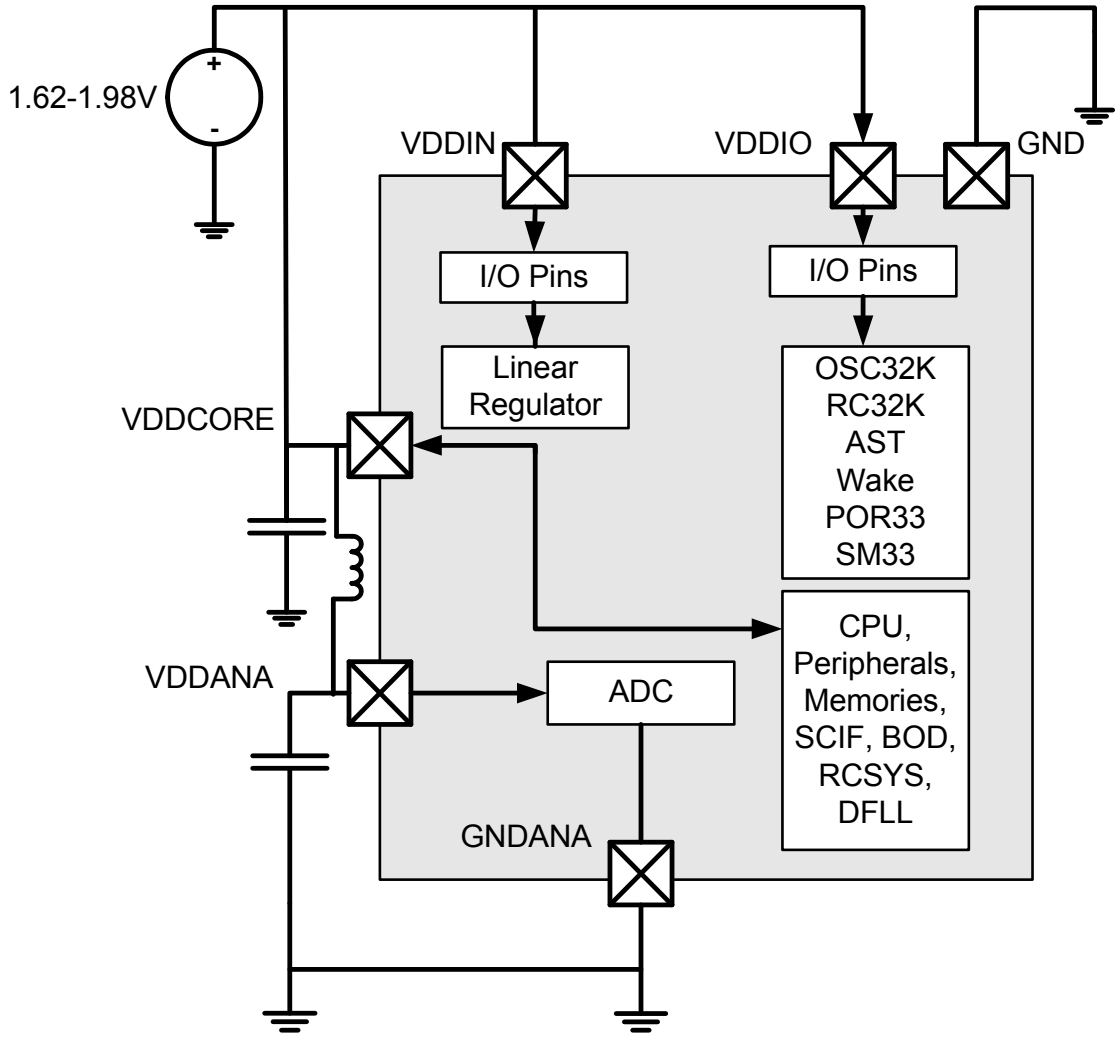
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFLGA Exposed Pad
Supplier Device Package	48-TLLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l032-d3hr

6.1.3.2 *1.8V Single Supply Mode*

In 1.8V single supply mode the internal regulator is not used, and VDDIO and VDDCORE are powered by a single 1.8V supply as shown in Figure 6-3. All I/O lines will be powered by the same power (VDDIN = VDDIO = VDDCORE).

Figure 6-3. 1.8V Single Supply Mode.



7.7.14 Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x024 + n*0x040

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	TERR	TRC	RCZ

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

- Unlock Register Error Status (URES) is set if an attempt was made to unlock a channel by writing to the Unlock Register while one or more error bits in SR were set (see Section 9.5.6). The unlock operation was aborted.
- Unlock Register Key Error (URKEY) is set if the Unlock Register was attempted written with an invalid key.
- Unlock Register Read (URREAD) is set if the Unlock Register was attempted read.
- Channel Access Unsuccessful (CAU) is set if the channel access was unsuccessful.
- Channel Access Successful (CAS) is set if the channel access was successful.
- Channel Unlock Expired (EXP) is set if the channel lock expired, with no channel being accessed after the channel was unlocked.

9.5.6 Error bits

If error bits are set when attempting to unlock a channel, SR.URES will be set. The following SR bits are considered error bits:

- EXP
- CAU
- URREAD
- URKEY
- URES
- MBERROR
- RTRADR

9.5.7 Bus Error Responses

By writing a one to the Bus Error Response Enable bit (CR.BERREN), serious access errors will be configured to return a bus error to the CPU. This will cause the CPU to execute its Bus Error Data Fetch exception routine.

The conditions that can generate a bus error response are:

- Reading the Unlock Register
- Trying to access a locked channel
- The SAU HSB master receiving a bus error response from its addressed slave

9.5.8 Disabling the SAU

To disable the SAU, the user must first ensure that no SAU bus operations are pending. This can be done by checking that the SR.IDLE bit is set.

The SAU may then be disabled by writing a one to the Disable (DIS) bit in CR.

- **CATRCMASK: CAT Request Clock Mask**
  0: CAT Request Clock is disabled
  1: CAT Request Clock is enabled
- **ACIFBRCMASK: ACIFB Request Clock Mask**
  0: ACIFB Request Clock is disabled
  1: ACIFB Request Clock is enabled
- **ADCIFBRCMASK: ADCIFB Request Clock Mask**
  0: ADCIFB Request Clock is disabled
  1: ADCIFB Request Clock is enabled
- **ASTRCMASK: AST Request Clock Mask**
  0: AST Request Clock is disabled
  1: AST Request Clock is enabled
- **TWIS0RCMASK: TWIS0 Request Clock Mask**
  0: TWIS0 Request Clock is disabled
  1: TWIS0 Request Clock is enabled
- **TWIS1RCMASK: TWIS1 Request Clock Mask**
  0: TWIS1 Request Clock is disabled
  1: TWIS1 Request Clock is enabled

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

locks will not be lost. When the reference clock has restarted, the FINE tracking will quickly compensate for any frequency drift during sleep.

13.5.3.8 Accuracy

There are mainly three factors that decide the accuracy of the f_{DFLL}. These can be tuned to obtain maximum accuracy when fine lock is achieved.

- FINE resolution: The frequency step between two FINE values. This is relatively smaller for high output frequencies.
- Resolution of the measurement: If the resolution of the measured f_{DFLL} is low, i.e. the ratio between CLK_DFLL frequency and CLK_DFLLIF_REF is small, then the DFLLIF might lock at a frequency that is lower than the targeted frequency. It is recommended to use a reference clock frequency of 32 KHz or lower to avoid this issue for low target frequencies.
- The accuracy of the reference clock.

13.5.3.9 Interrupts

A interrupt can be generated on a zero-to-one transaction on DFLLnLOCKC, DFLLnLOCKF, DFLLnLOCKA, DFLLnLOCKLOSTC, DFLLnLOCKLOSTF, DFLLnLOCKLOSTA, DFLLnRDY or DFLLnRCS.

13.5.4 Brown-Out Detection (BOD)

Rev: 1.0.1.0

The Brown-Out Detector monitors the VDDCORE supply pin and compares the supply voltage to the brown-out detection level.

The BOD is disabled by default, and is enabled by writing to the BOD Control field in the BOD Control Register (BOD.CTRL). This field can also be updated by flash fuses.

The BOD is powered by VDDIO and will not be powered during Shutdown sleep mode.

To prevent unexpected writes to the BOD register due to software bugs, write access to this register is protected by a locking mechanism. For details please refer to the UNLOCK register description.

To prevent further modifications by software, the content of the BOD register can be set as read-only by writing a one to the Store Final Value bit (BOD.SFV). When this bit is one, software can not change the BOD register content. This bit is cleared after flash calibration and after a reset except after a BOD reset.

The brown-out detection level is selected by writing to the BOD Level field in BOD (BOD.LEVEL). Please refer to the Electrical Characteristics chapter for parametric details.

If the BOD is enabled (BOD.CTRL is one or two) and the supply voltage goes below the detection level, the Brown-Out Detection bit in the Power and Clocks Status Register (PCLKSR.BODDET) is set. This bit is cleared when the supply voltage goes above the detection level. An interrupt request will be generated on a zero-to-one transition on PCLKSR.BODDET if the Brown-Out Detection bit in the Interrupt Mask Register (IMR.BODDET) is set. This bit is set by writing a one to the corresponding bit in the Interrupt Enable Register (IER.BODDET).

If BOD.CTRL is one, a BOD reset will be generated when the supply voltage goes below the detection level. If BOD.CTRL is two, the device will not be reset.

Writing a one to the BOD Hysteresis bit in BOD (BOD.HYST) will add a hysteresis on the BOD detection level.

21.7.3 Clocks

The clock for the TWIM bus interface (CLK_TWIM) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the TWIM before disabling the clock, to avoid freezing the TWIM in an undefined state.

21.7.4 DMA

The TWIM DMA handshake interface is connected to the Peripheral DMA Controller. Using the TWIM DMA functionality requires the Peripheral DMA Controller to be programmed after setting up the TWIM.

21.7.5 Interrupts

The TWIM interrupt request lines are connected to the interrupt controller. Using the TWIM interrupts requires the interrupt controller to be programmed first.

21.7.6 Debug Operation

When an external debugger forces the CPU into debug mode, the TWIM continues normal operation. If the TWIM is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

When writing a one to CR.TCLR, the timebase counter and the spread spectrum counter are reset at their lower limit values and the effective top value of the timebase counter will also be reset.

23.6.4 Duty Cycle and Waveform Properties

Each PWM channel has its own duty cycle value (DCV) which is write-only and cannot be read out. The duty cycle value can be changed in two approaches as described in Section23.6.5.

When the duty cycle value is zero, the PWM output is zero. Otherwise, the PWM output is set when the timebase counter is zero, and cleared when the timebase counter reaches the duty cycle value. This is summarized as:

$$\text{PWM Waveform} = \begin{cases} low \text{ when } DCV = 0 \text{ or } TC > DCV \\ high \text{ when } TC \leq DCV \text{ and } DCV \neq 0 \end{cases}$$

Note that when increasing the duty cycle value for one channel from 0 to 1, the number of GCLK cycles when the PWM waveform is high will jump from 0 to 2. When incrementing the duty cycle value by one for any other values, the number of GCLK cycle when the waveform is high will increase by one. This is summarized in Table 23-2.

Table 23-2. PMW Waveform Duty Cycles

Duty Cycle Value	#Clock Cycles When Waveform is High	#Clock Cycles When Waveform is Low
0	0	ETV+1
1	2	ETV-1
2	3	ETV-2
...	...	...
ETV-1	ETV	1
ETV	ETV+1	0

Every other output PWM waveform toggles on the negative edge of the GCLK instead of the positive edge. This is to avoid too many I/O toggling simultaneously on the output I/O lines.

23.6.5 Updating Duty Cycle Values

23.6.5.1 Interlinked Single Value PWM Operation

The PWM channels can be interlinked to allow multiple channels to be updated simultaneously with the same duty cycle value. This value must be written to the Interlinked Single Value Duty (ISDUTY) register. Each channel has a corresponding enabling bit in the Interlinked Single Value Channel Set (ISCHSETm) register. When a bit is written to one in the ISCHSETm register, the duty cycle register for the corresponding channel will be updated with the value stored in the ISDUTY register. It can only be updated when the READY bit in the Status Register (SR.READY) is one, indicating that the PWMA is ready for writing. Figure 23-3 on page 524 shows the writing procedure. It is thus possible to update the duty cycle values for up to 32 PWM channels within one ISCHSETm register at a time.

0: TIOB is used as an external trigger.

- **ETRGEDG: External Trigger Edge Selection**

ETRGEDG	Edge
0	none
1	rising edge
2	falling edge
3	each edge

- **LDBDIS: Counter Clock Disable with RB Loading**
  1: Counter clock is disabled when RB loading occurs.
  0: Counter clock is not disabled when RB loading occurs.
- **LDBSTOP: Counter Clock Stopped with RB Loading**
  1: Counter clock is stopped when RB loading occurs.
  0: Counter clock is not stopped when RB loading occurs.
- **BURST: Burst Signal Selection**

BURST	Burst Signal Selection
0	The clock is not gated by an external signal
1	XC0 is ANDed with the selected clock
2	XC1 is ANDed with the selected clock
3	XC2 is ANDed with the selected clock

- **CLKI: Clock Invert**
  1: The counter is incremented on falling edge of the clock.
  0: The counter is incremented on rising edge of the clock.
- **TCCLKS: Clock Selection**

TCCLKS	Clock Selected
0	TIMER_CLOCK1
1	TIMER_CLOCK2
2	TIMER_CLOCK3
3	TIMER_CLOCK4
4	TIMER_CLOCK5
5	XC0
6	XC1
7	XC2

Table 25-3. Peripheral Event Mapping from AST

Generator	Generated Event	User	Effect	Asynchronous
AST	Overflow event	ACIFB	Comparison is triggered if the ACIFB.CONFn register is written to 11 (Event Triggered Single Measurement Mode) and the EVENTEN bit in the ACIFB.CTRL register is written to 1.	Yes
	Periodic event			
	Alarm event			
	Overflow event	ADCIFB	Conversion is triggered if the TRGMOD bit in the ADCIFB.TRGR register is written to 111 (Peripheral Event Trigger).	
	Periodic event			
	Alarm event			
	Overflow event	CAT	Trigger one iteration of autonomous touch detection.	
	Periodic event			
	Alarm event			

Table 25-4. Peripheral Event Mapping from PWMA

Generator	Generated Event	User	Effect	Asynchronous
PWMA channel 0	Timebase counter reaches the duty cycle value.	ACIFB	Comparison is triggered if the ACIFB.CONFn register is written to 11 (Event Triggered Single Measurement Mode) and the EVENTEN bit in the ACIFB.CTRL register is written to 1.	No
		ADCIFB	Conversion is triggered if the TRGMOD bit in the ADCIFB.TRGR register is written to 111 (Peripheral Event Trigger).	

25.4.2 Peripheral Event Connections

Each generated peripheral event is connected to one or more users. If a peripheral event is connected to multiple users, the peripheral event can trigger actions in multiple modules.

A peripheral event user can likewise be connected to one or more peripheral event generators. If a peripheral event user is connected to multiple generators, the peripheral events are OR'ed together to a single peripheral event. This means that peripheral events from either one of the generators will result in a peripheral event to the user.

To configure a peripheral event, the peripheral event must be enabled at both the generator and user side. Even if a generator is connected to multiple users, only the users with the peripheral event enabled will trigger on the peripheral event.

25.4.3 Low Power Operation

As the peripheral events do not require CPU intervention, they are available in Idle mode. They are also available in deeper sleep modes if both the generator and user remain clocked in that mode.

Certain events are known as asynchronous peripheral events, as identified in Table 25-1 to Table 25-4. These can be issued even when the system clock is stopped, and revive unclocked user peripherals. The clock will be restarted for this module only, without waking the system from sleep mode. The clock remains active only as long as required by the triggered function, before being switched off again, and the system remains in the original sleep mode. The CPU and sys-

tem will only be woken up if the user peripheral generates an interrupt as a result of the operation. This concept is known as SleepWalking and is described in further detail in the Power Manager chapter. Note that asynchronous peripheral events may be associated with a delay due to the need to restart the system clock source if this has been stopped in the sleep mode.

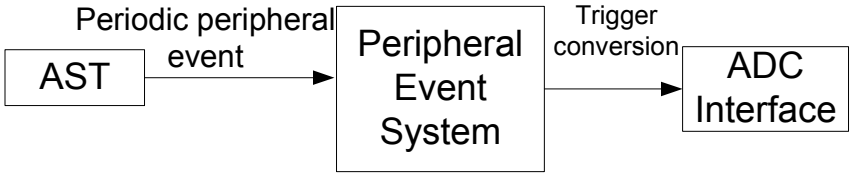
25.5 Application Example

This application example shows how the Peripheral Event System can be used to program the ADC Interface to perform ADC conversions at selected intervals.

Conversions of the active analog channels are started with a software or a hardware trigger. One of the possible hardware triggers is a peripheral event trigger, allowing the Peripheral Event System to synchronize conversion with some configured peripheral event source. From Table 25-3 and Table 25-4, it can be read that this peripheral event source can be either an AST peripheral event, or an event from the PWM Controller. The AST can generate periodic peripheral events at selected intervals, among other types of peripheral events. The Peripheral Event System can then be used to set up the ADC Interface to sample an analog signal at regular intervals.

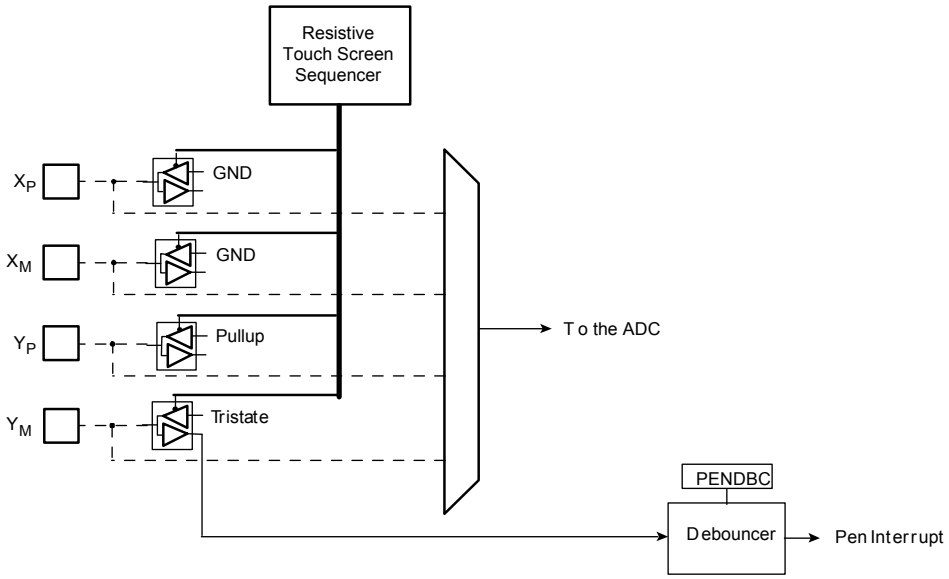
The user must enable peripheral events in the AST and in the ADC Interface to accomplish this. The periodic peripheral event in the AST is enabled by writing a one to the corresponding bit in the AST Event Enable Register (EVE). To select the peripheral event trigger for the ADC Interface, the user must write the value 0x7 to the Trigger Mode (TRGMOD) field in the ADC Interface Trigger Register (TRGR). When the peripheral events are enabled, the AST will generate peripheral events at the selected intervals, and the Peripheral Event System will route the peripheral events to the ADC Interface, which will perform ADC conversions at the selected intervals.

Figure 25-2. Application Example



Since the AST peripheral event is asynchronous, the description above will also work in sleep modes where the ADC clock is stopped. In this case, the ADC clock (and clock source, if needed) will be restarted during the ADC conversion. After the conversion, the ADC clock and clock source will return to the sleep state, unless the ADC generates an interrupt, which in turn will wake up the system. Using asynchronous interrupts thus allows ADC operation in much lower power states than would otherwise be possible.

Figure 26-4. Resistive Touch Screen Pen Detect



The Resistive Touch Screen Pen Detect can be used to generate an ADCIFB interrupt request or it can be used to trig a conversion, so that a position can be measured as soon as a contact is detected.

The Pen Detect Mode generates two types of status signals, reported in the Status Register (SR):

- The bit PENCNT is set when current flows and remains set until current stops.
- The bit NOCNT is set when no current flows and remains set until current flows.

Before a current change is reflected in the SR, the new status must be stable for the duration of the debouncing time.

Both status conditions can generate an interrupt request if the corresponding bit in the Interrupt Mask Register (IMR) is one. Refer to Section 26.6.11 on page 593.

28.7.7 Autonomous Touch Configuration Register 3

Name: ATCFG3

Access Type: Read/Write

Offset: 0x1C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-							
23	22	21	20	19	18	17	16
PTHR							
15	14	13	12	11	10	9	8
PDRIFT							
7	6	5	4	3	2	1	0
NDRIFT							

- **PTHR: Positive Recalibration Threshold**
  For the autonomous QTouch sensor, specifies how far a sensor's signal must move in a positive direction from the reference in order to cause a recalibration.
- **PDRIFT: Positive Drift Compensation**
  For the autonomous QTouch sensor, specifies how often a positive drift compensation should be performed. When this field is zero, positive drift compensation will never be performed. When this field is non-zero, the positive drift compensation time interval is given by the following formula:
  Tpdrift = PDRIFT * 65536 * (sample clock period)
- **NDRIFT: Negative Drift Compensation**
  For the autonomous QTouch sensor, specifies how often a negative drift compensation should be performed. When this field is zero, negative drift compensation will never be performed. When this field is non-zero, the negative drift compensation time interval is given by the following formula:
  Tndrift = NDRIFT * 65536 * (sample clock period)

With the typical sample clock frequency of 1 MHz, PDRIFT and NDRIFT can be set from 0.066 seconds to 16.7 seconds with 0.066 second resolution.

This bit is set when the clock is disabled.

This bit is cleared when the clock is enabled.

- **BUSY: Synchronizer Busy**

  0: The asynchronous interface is ready to accept more data.

  1: The asynchronous interface is busy and will block writes to CTRL, BRR, and THR.

  This bit is set when the asynchronous interface becomes busy.

  This bit is cleared when the asynchronous interface becomes ready.

Table 31-11. Instruction Description (Continued)

Instruction	Description
DR Size	Shows the number of bits in the data register chain when this instruction is active. Example: 34 bits
DR input value	Shows which bit pattern to shift into the data register in the Shift-DR state when this instruction is active. Multiple such lines may exist, e.g., to distinguish between reads and writes. Example: aaaaaaar xxxxxxxx xxxxxxxx xxxxxxxx xx
DR output value	Shows the bit pattern shifted out of the data register in the Shift-DR state when this instruction is active. Multiple such lines may exist, e.g., to distinguish between reads and writes. Example: xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

31.5.2 Public JTAG Instructions

The JTAG standard defines a number of public JTAG instructions. These instructions are described in the sections below.

31.5.2.1 IDCODE

This instruction selects the 32 bit Device Identification register (DID) as Data Register. The DID register consists of a version number, a device number, and the manufacturer code chosen by JEDEC. This is the default instruction after a JTAG reset. Details about the DID register can be found in the module configuration section at the end of this chapter.

Starting in Run-Test/Idle, the Device Identification register is accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Capture-DR: The IDCODE value is latched into the shift register.
7. In Shift-DR: The IDCODE scan chain is shifted by the TCK input.
8. Return to Run-Test/Idle.

Table 31-12. IDCODE Details

Instructions	Details
IR input value	**00001** (0x01)
IR output value	p0001
DR Size	32
DR input value	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
DR output value	Device Identification Register

31.5.2.2 SAMPLE_PRELOAD

This instruction takes a snap-shot of the input/output pins without affecting the system operation, and pre-loading the scan chain without updating the DR-latch. The boundary-scan chain is selected as Data Register.

Starting in Run-Test/Idle, the Device Identification register is accessed in the following way:

6. Scan in an 16-bit counter value.
7. Go to Update-DR and re-enter Select-DR Scan.
8. In Shift-DR: Scan out the busy bit, and until the busy bit clears goto 7.
9. Calculate an approximation to the internal clock speed using the elapsed time and the counter value.
10. Return to Run-Test/Idle.

The full 16-bit counter value must be provided when starting the synch operation, or the result will be undefined. When reading status, shifting may be terminated once the required number of bits have been acquired.

Table 31-25. SYNC_ACCESS Details

Instructions	Details
IR input value	**10111** (0x17)
IR output value	peb01
DR Size	16 bits
DR input value	dddddddd dddddddd
DR output value	xxxxxxxx xxxxxxeb

31.5.3.8 AVR_RESET

This instruction allows a debugger or tester to directly control separate reset domains inside the chip. The shift register contains one bit for each controllable reset domain. Setting a bit to one resets that domain and holds it in reset. Setting a bit to zero releases the reset for that domain.

The AVR_RESET instruction can be used in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Shift-DR: Scan in the value corresponding to the reset domains the JTAG master wants to reset into the data register.
7. Return to Run-Test/Idle.
8. Stay in run test idle for at least 10 TCK clock cycles to let the reset propagate to the system.

See the device specific documentation for the number of reset domains, and what these domains are.

For any operation, all bits must be provided or the result will be undefined.

Table 31-26. AVR_RESET Details

Instructions	Details
IR input value	**01100** (0x0C)
IR output value	p0001

Table 32-26. BOD Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{HYST}	BOD hysteresis	T = 25°C		10		mV
t_{DET}	Detection time	Time with VDDCORE < BODLEVEL necessary to generate a reset signal		1		µs
I_{BOD}	Current consumption			16		µA
$t_{STARTUP}$	Startup time			5		µs

32.8.5 Supply Monitor 33 Characteristics

Table 32-27. SM33 Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{TH}	Voltage threshold	Calibrated(1), T = 25°C	1.675	1.75	1.825	V
	Step size, between adjacent values in SCIF.SM33.CALIB			11		mV
V_{HYST}	Hysteresis			30		
t_{DET}	Detection time	Time with VDDIN < V_{TH} necessary to generate a reset signal		280		µs
I_{SM33}	Current consumption	Normal mode		15		µA
$t_{STARTUP}$	Startup time	Normal mode		140		µs

Note: 1. Calibration value can be read from the SCIF.SM33.CALIB field. This field is updated by the flash fuses after a reset. Refer to SCIF chapter for details.

32.9.6 JTAG Timing

Figure 32-18. JTAG Interface Signals

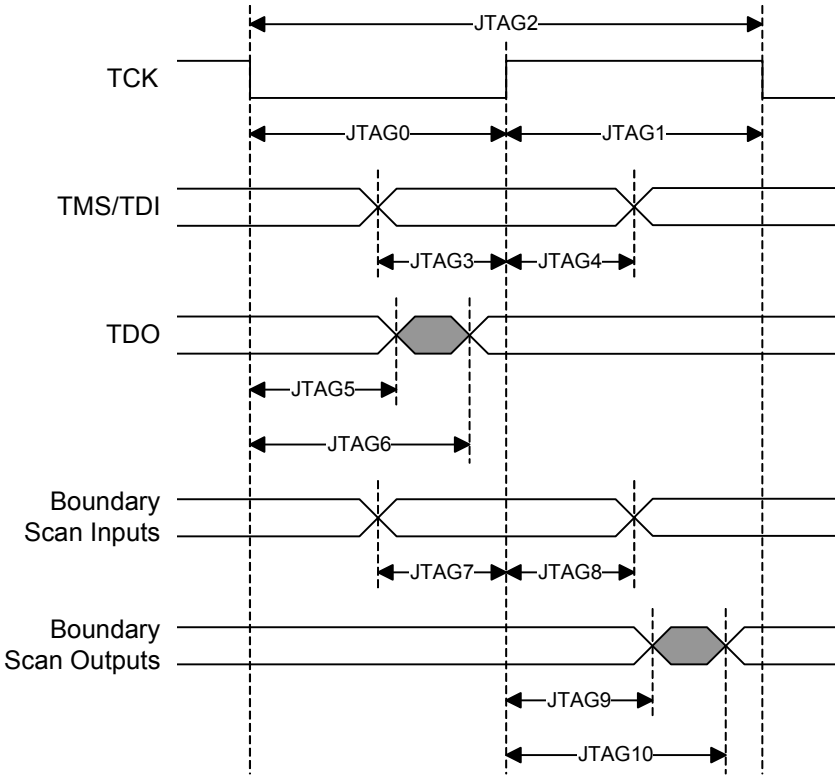


Table 32-43. JTAG Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
JTAG0	TCK Low Half-period	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	23.2		ns
JTAG1	TCK High Half-period		8.8		
JTAG2	TCK Period		32.0		
JTAG3	TDI, TMS Setup before TCK High		3.9		
JTAG4	TDI, TMS Hold after TCK High		0.6		
JTAG5	TDO Hold Time		4.5		
JTAG6	TCK Low to TDO Valid			23.2	
JTAG7	Boundary Scan Inputs Setup Time		0		
JTAG8	Boundary Scan Inputs Hold Time		5.0		
JTAG9	Boundary Scan Outputs Hold Time		8.7		
JTAG10	TCK to Boundary Scan Outputs Valid			17.7	

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

None.

2. **The aWire debug interface is reset after leaving Shutdown mode**
   If the aWire debug mode is used as debug interface and the program enters Shutdown mode, the aWire interface will be reset when the part receives a wakeup either from the WAKE_N pin or the AST.
   Fix/Workaround
   None.

35.2.14 CHIP

1. **In 3.3V Single Supply Mode, the Analog Comparator inputs affects the device's ability to start**
   When using the 3.3V Single Supply Mode the state of the Analog Comparator input pins can affect the device's ability to release POR reset. This is due to an interaction between the Analog Comparator input pins and the POR circuitry. The issue is not present in the 1.8V Supply Mode or the 3.3V Supply Mode with 1.8V Regulated I/O Lines.
   Fix/Workaround
   ACREFN (pin PA16) must be connected to GND until the POR reset is released and the Analog Comparator inputs should not be driven higher than 1.0V until the POR reset is released.

2. **Increased Power Consumption in VDDIO in sleep modes**
   If OSC0 is enabled in crystal mode when entering a sleep mode where the OSC0 is disabled, this will lead to an increased power consumption in VDDIO.
   Fix/Workaround
   Solution 1: Disable OSC0 by writing a zero to the Oscillator Enable bit in the System Control Interface (SCIF) Oscillator Control Register (SCIF.OSC0CTRL.OSCEN) before going to a sleep mode where OSC0 is disabled.
   Solution 2: Pull down or up XIN0 or XOUT0 with 1MOhm resistor.

35.2.15 I/O Pins

1. **PA17 has low ESD tolerance**
   PA17 only tolerates 500V ESD pulses (Human Body Model).
   Fix/Workaround
   Care must be taken during manufacturing and PCB design.

35.3 Rev. C

Not sampled.

35.4 Rev. B

35.4.1 Processor and Architecture

1. **RETS behaves incorrectly when MPU is enabled**
   RETS behaves incorrectly when MPU is enabled and MPU is configured so that system stack is not readable in unprivileged mode.
   Fix/Workaround
   Make system stack readable in unprivileged mode, or return from supervisor mode using rete instead of rets. This requires:
   1. Changing the mode bits from 001 to 110 before issuing the instruction. Updating the mode bits to the desired value must be done using a single mtsr instruction so it is done

36. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 Rev. I - 01/2012

1. Overview - Block diagram: CAT SMP corrected from I/O to output. SPI NPCS corrected from output to I/O.
2. Package and Pinout: PRND signal removed from Signal Descriptions List table and GPIO Controller Function Multiplexing table
3. ADCIFB: PRND signal removed from block diagram.
4. Electrical Characteristics: Added pin input capacitance C_{IN} for TLLGA package for “all normal I/O pins except PA05 , PA07, PA17, PA20, PA21, PB04, PB05”.
5. Errata: Added more errata for TWI and CAT modules.

36.2 Rev. H - 12/2011

1. Mechanical Characteristics: Updated the note related to the QFN48 Package Drawing.Updated thermal reistance data for TLLGA48 package. Updated package drawings for TQFP48 and QFN48 packages. Soldering profile updated (Time maintained above 217°C.)
2. Memories: Local bus address map corrected: The address offset for port 1 registers is 0x100, not 0x200.
3. SCIF DFLL: Removed “not” from “DFLLnSTEP.CSTEP and DFLLnSTEP.FSTEP should not be lower than 50% of the maximum value of DFLLnCONF.COARSE and DFLLnCONF.FINE”.
4. SCIF VREG POR descriptions updated. POR33 bits added in VREGCR.
5. SCIF VREG: Removed reference to flash fuses for CALIB field, user is recommended not writing to SELVDD field. Removed references to Electrical Characteristics.
6. SCIF: Fuses text removed from some submodules (SM33, VREG).
7. SCIF VREG: Flash recalibration is always done at POR.
8. SCIF SM33: Enabling SM33 will disable the POR33 detector.
9. Erratum regarding OSC32 disabling is not valid for RevB.
10. Flash Controller: Serial number address updated.
11. Block diagram and ADCIFB: Removed PRND signal from block diagram and ADCIFB block diagram.
12. USART: Added CTSIC bit description.
13. Power Manager: Updated Clock division and Clock ready flag sections.
14. ADCIFB: Added DMA section in Product Dependencies.