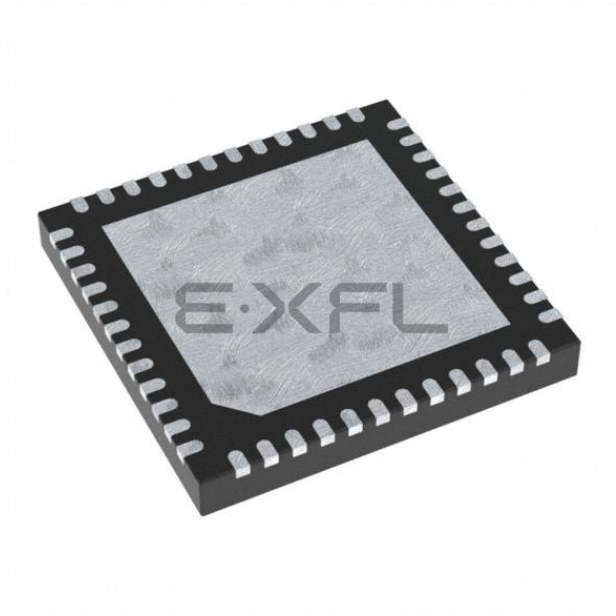

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l032-zaur

3.4.8 RC32OUT Pin

3.4.8.1 Clock output at startup

After power-up, the clock generated by the 32kHz RC oscillator (RC32K) will be output on PA20, even when the device is still reset by the Power-On Reset Circuitry. This clock can be used by the system to start other devices or to clock a switching regulator to rise the power supply voltage up to an acceptable value.

The clock will be available on PA20, but will be disabled if one of the following conditions are true:

- PA20 is configured to use a GPIO function other than F (SCIF-RC32OUT)
- PA20 is configured as a General Purpose Input/Output (GPIO)
- The bit FRC32 in the Power Manager PPCR register is written to zero (refer to the Power Manager chapter)

The maximum amplitude of the clock signal will be defined by VDDIN.

Once the RC32K output on PA20 is disabled it can never be enabled again.

3.4.8.2 XOUT32_2 function

PA20 selects RC32OUT as default enabled after reset. This function is not automatically disabled when the user enables the XOUT32_2 function on PA20. This disturbs the oscillator and may result in the wrong frequency. To avoid this, RC32OUT must be disabled when XOUT32_2 is enabled.

3.4.9 ADC Input Pins

These pins are regular I/O pins powered from the VDDIO. However, when these pins are used for ADC inputs, the voltage applied to the pin must not exceed 1.98V. Internal circuitry ensures that the pin cannot be used as an analog input pin when the I/O drives to VDD. When the pins are not used for ADC inputs, the pins may be driven to the full I/O voltage range.

- Programming Error: A bad keyword and/or an invalid command have been written in the FCMD register.
- Lock Error: At least one lock region is protected, or BOOTPROT is different from 0. The erase command has been aborted and no page has been erased. A “Unlock region containing given page” (UP) command must be executed to unlock any locked regions.

8.5.3 Region Lock Bits

The flash memory has *p* pages, and these pages are grouped into 16 lock regions, each region containing *p*/16 pages. Each region has a dedicated lock bit preventing writing and erasing pages in the region. After production, the device may have some regions locked. These locked regions are reserved for a boot or default application. Locked regions can be unlocked to be erased and then programmed with another application or other data.

To lock or unlock a region, the commands Lock Region Containing Page (LP) and Unlock Region Containing Page (UP) are provided. Writing one of these commands, together with the number of the page whose region should be locked/unlocked, performs the desired operation.

One error can be detected in the FSR register after issuing the command:

- Programming Error: A bad keyword and/or an invalid command have been written in the FCMD register.

The lock bits are implemented using the lowest 16 general-purpose fuse bits. This means that lock bits can also be set/cleared using the commands for writing/erasing general-purpose fuse bits, see Section 8.6. The general-purpose bit being in an erased (1) state means that the region is unlocked.

The lowermost pages in the flash can additionally be protected by the BOOTPROT fuses, see Section 8.6.

8.6 General-purpose Fuse Bits

The flash memory has a number of general-purpose fuse bits that the application programmer can use freely. The fuse bits can be written and erased using dedicated commands, and read

9.6.2 Configuration Register

Name: CONFIG

Access Type: Write-only

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	OPEN

15	14	13	12	11	10	9	8
UCYC							

7	6	5	4	3	2	1	0
UKEY							

- **OPEN: Open Mode Enable**
  Writing a zero to this bit disables open mode.
  Writing a one to this bit enables open mode.
- **UCYC: Unlock Number of Clock Cycles**
  Once a channel has been unlocked, it remains unlocked for this amount of CLK_SAU_HSB clock cycles or until one access to a channel has been made.
- **UKEY: Unlock Key**
  The value in this field must be written to UR.KEY to unlock a channel.

12.6.3.3 Waking from sleep modes

There are two types of wake-up sources from sleep mode, synchronous and asynchronous. Synchronous wake-up sources are all non-masked interrupts. Asynchronous wake-up sources are AST, WDT, external interrupts from EIC, external reset, external wake pin (WAKE_N), and all asynchronous wake-ups enabled in the Asynchronous Wake Up Enable (AWEN) register. The valid wake-up sources for each sleep mode are detailed in Table 12-3 on page 156.

In Shutdown the only wake-up sources are external reset, external wake-up pin or AST. See Section 12.6.4.3 on page 158.

Table 12-3. Wake-up Sources

Index[1]	Sleep Mode	Wake-up Sources
0	**Idle**	Synchronous, Asynchronous
1	**Frozen**	Synchronous[2], Asynchronous
2	**Standby**	Asynchronous
3	**Stop**	Asynchronous
4	**DeepStop**	Asynchronous
5	**Static**	Asynchronous[3]
6	**Shutdown**	External reset, External wake-up pin

Notes:
1. The sleep mode index is used as argument for the sleep instruction.
2. Only PB modules operational, as HSB module clocks are stopped.
3. WDT only available if clocked from pre-enabled OSC32K.

12.6.3.4 SleepWalking

In all sleep modes where the PBx clocks are stopped, except for Shutdown mode, the device can partially wake up if a PBx module asynchronously discovers that it needs its clock. Only the requested clocks and clock sources needed will be started, all other clocks will remain masked to zero. E.g. if the main clock source is OSC0, only OSC0 will be started even if other clock sources were enabled in normal mode. Generic clocks can also be started in a similar way. The state where only requested clocks are running is referred to as SleepWalking.

The time spent to start the requested clock is mostly limited by the startup time of the given clock source. This allows PBx modules to handle incoming requests, while still keeping the power consumption at a minimum.

When the device is SleepWalking any asynchronous wake-up can wake the device up at any time without stopping the requested PBx clock.

All requests to start clocks can be masked by writing to the Peripheral Power Control Register (PPCR), all requests are enabled at reset.

During SleepWalking the interrupt controller clock will be running. If an interrupt is pending when entering SleepWalking, it will wake the whole device up.

12.6.3.5 Precautions when entering sleep mode

Modules communicating with external circuits should normally be disabled before entering a sleep mode that will stop the module operation. This will prevent erratic behavior caused by entering or exiting sleep modes. Please refer to the relevant module documentation for recommended actions.

13.6.13 DFLLn Spread Spectrum Generator Control Register

Name: DFLLnSSG

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	STEPSIZE[4:0]				

15	14	13	12	11	10	9	8
-	-	-	AMPLITUDE[4:0]				

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PRBS	EN

- **STEPSIZE: SSG Step Size**
  Sets the step size of the spread spectrum.
- **AMPLITUDE: SSG Amplitude**
  Sets the amplitude of the spread spectrum.
- **PRBS: Pseudo Random Bit Sequence**
  0: Each spread spectrum frequency is applied at constant intervals
  1: Each spread spectrum frequency is applied at pseudo-random intervals
- **EN: Enable**
  0: SSG is disabled.
  1: SSG is enabled.

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

14.6.9 Alarm Register 0

Name: AR0

Access Type: Read/Write

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
VALUE[31:24]							

23	22	21	20	19	18	17	16
VALUE[23:16]							

15	14	13	12	11	10	9	8
VALUE[15:8]							

7	6	5	4	3	2	1	0
VALUE[7:0]							

When the SR.BUSY bit is set writes to this register will be discarded and this register will read as zero.

- **VALUE: Alarm Value**
  When the counter reaches this value, an alarm is generated.

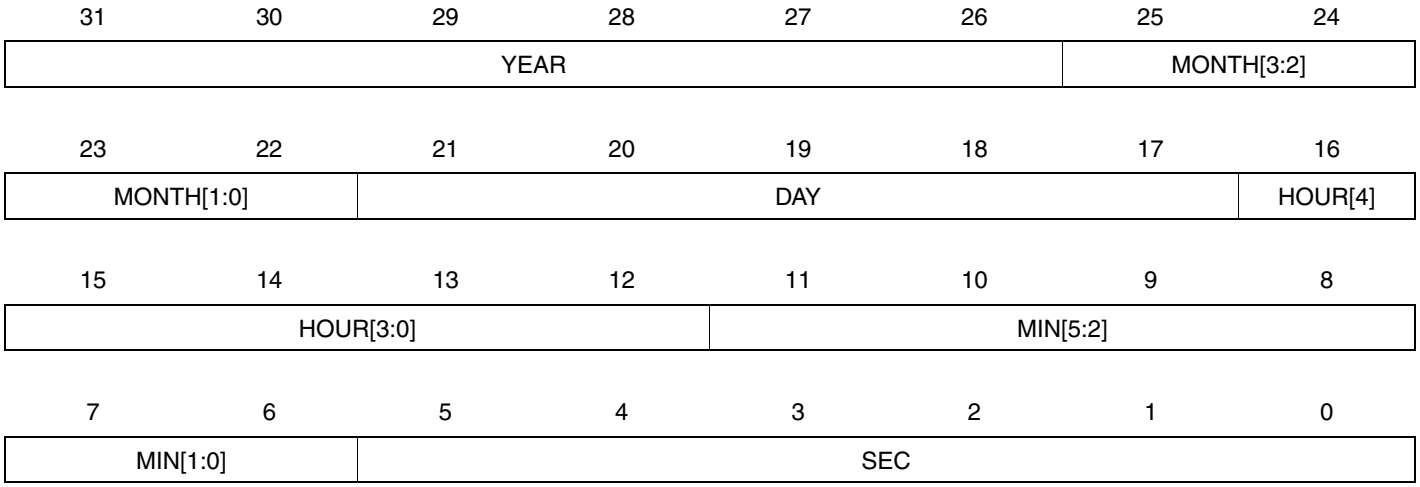
14.6.18 Calendar Value

Name: CALV

Access Type: Read/Write

Offset: 0x54

Reset Value: 0x00000000



When the SR.BUSY bit is set writes to this register will be discarded and this register will read as zero.

- **YEAR: Year**
  Current year. The year is considered a leap year if YEAR[1:0] = 0.
- **MONTH: Month**
  1 = January
  2 = February
  ...
  12 = December
- **DAY: Day**
  Day of month, starting with 1.
- **HOUR: Hour**
  Hour of day, in 24-hour clock format.
  Legal values are 0 through 23.
- **MIN: Minute**
  Minutes, 0 through 59.
- **SEC: Second**
  Seconds, 0 through 59.

17. Frequency Meter (FREQM)

Rev: 3.0.1.1

17.1 Features

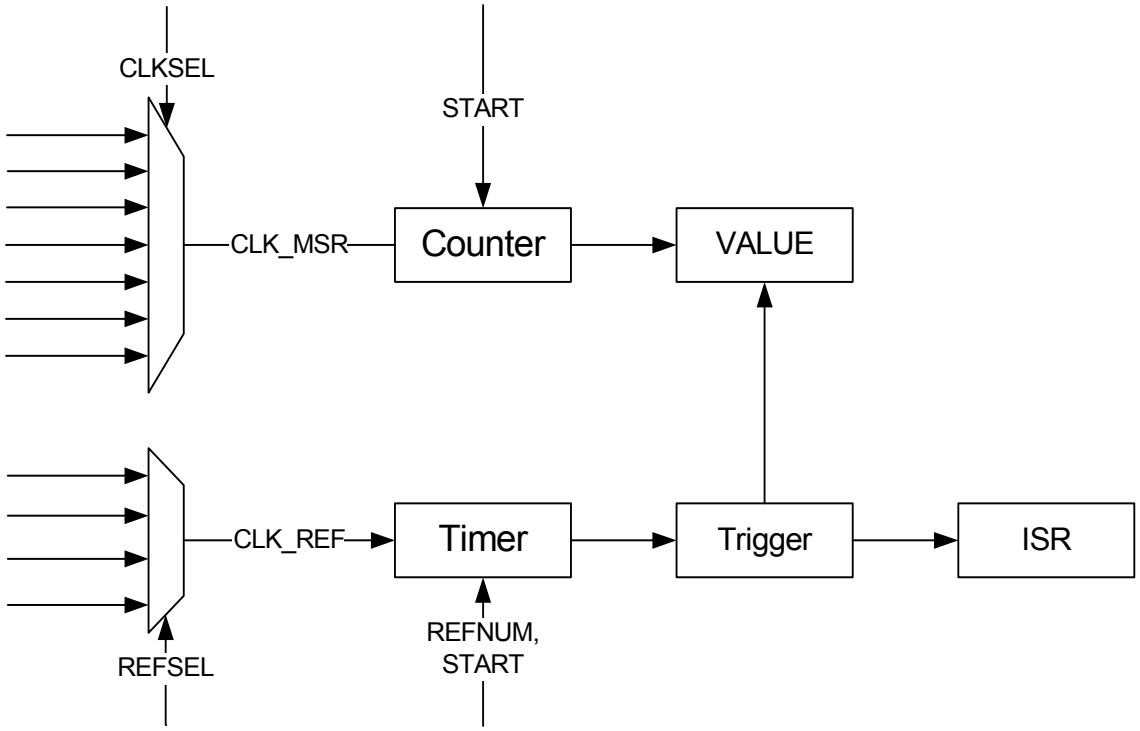
- **Accurately measures a clock frequency**
- **Selectable reference clock**
- **A selectable clock can be measured**
- **Ratio can be measured with 24-bit accuracy**

17.2 Overview

The Frequency Meter (FREQM) can be used to accurately measure the frequency of a clock by comparing it to a known reference clock.

17.3 Block Diagram

Figure 17-1. Frequency Meter Block Diagram



17.4 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

17.4.1 Power Management

The device can enter a sleep mode while a measurement is ongoing. However, make sure that neither CLK_MSR nor CLK_REF is stopped in the actual sleep mode. FREQM interrupts can wake up the device from sleep modes when the measurement is done, but only from sleep modes where CLK_FREQM is running. Please refer to the Power Manager chapter for details.

17.6 User Interface

Table 17-1. FREQM Register Memory Map

Offset	Register	Register Name	Access	Reset
0x000	Control Register	CTRL	Write-only	0x00000000
0x004	Mode Register	MODE	Read/Write	0x00000000
0x008	Status Register	STATUS	Read-only	0x00000000
0x00C	Value Register	VALUE	Read-only	0x00000000
0x010	Interrupt Enable Register	IER	Write-only	0x00000000
0x014	Interrupt Disable Register	IDR	Write-only	0x00000000
0x018	Interrupt Mask Register	IMR	Read-only	0x00000000
0x01C	Interrupt Status Register	ISR	Read-only	0x00000000
0x020	Interrupt Clear Register	ICR	Write-only	0x00000000
0x3FC	Version Register	VERSION	Read-only	-(1)

Note: 1. The reset value for this register is device specific. Please refer to the Module Configuration section at the end of this chapter.

Table 18-2. GPIO Register Memory Map

Offset	Register	Function	Register Name	Access	Reset	Config. Protection	Access Protection
0x02C	Peripheral Mux Register 1	Toggle	PMR1T	Write-only		Y	N
0x030	Peripheral Mux Register 2	Read/Write	PMR2	Read/Write	-(1)	Y	N
0x034	Peripheral Mux Register 2	Set	PMR2S	Write-only		Y	N
0x038	Peripheral Mux Register 2	Clear	PMR2C	Write-only		Y	N
0x03C	Peripheral Mux Register 2	Toggle	PMR2T	Write-only		Y	N
0x040	Output Driver Enable Register	Read/Write	ODER	Read/Write	-(1)	Y	N
0x044	Output Driver Enable Register	Set	ODERS	Write-only		Y	N
0x048	Output Driver Enable Register	Clear	ODERC	Write-only		Y	N
0x04C	Output Driver Enable Register	Toggle	ODERT	Write-only		Y	N
0x050	Output Value Register	Read/Write	OVR	Read/Write	-(1)	N	N
0x054	Output Value Register	Set	OVRS	Write-only		N	N
0x058	Output Value Register	Clear	OVRC	Write-only		N	N
0x05c	Output Value Register	Toggle	OVRT	Write-only		N	N
0x060	Pin Value Register	Read	PVR	Read-only	Depending on pin states	N	N
0x064	Pin Value Register	-	-	-		N	N
0x068	Pin Value Register	-	-	-		N	N
0x06c	Pin Value Register	-	-	-		N	N
0x070	Pull-up Enable Register	Read/Write	PUER	Read/Write	-(1)	Y	N
0x074	Pull-up Enable Register	Set	PUERS	Write-only		Y	N
0x078	Pull-up Enable Register	Clear	PUERC	Write-only		Y	N
0x07C	Pull-up Enable Register	Toggle	PUERT	Write-only		Y	N
0x090	Interrupt Enable Register	Read/Write	IER	Read/Write	-(1)	N	N
0x094	Interrupt Enable Register	Set	IERS	Write-only		N	N
0x098	Interrupt Enable Register	Clear	IERC	Write-only		N	N
0x09C	Interrupt Enable Register	Toggle	IERT	Write-only		N	N
0x0A0	Interrupt Mode Register 0	Read/Write	IMR0	Read/Write	-(1)	N	N
0x0A4	Interrupt Mode Register 0	Set	IMR0S	Write-only		N	N
0x0A8	Interrupt Mode Register 0	Clear	IMR0C	Write-only		N	N
0x0AC	Interrupt Mode Register 0	Toggle	IMR0T	Write-only		N	N
0x0B0	Interrupt Mode Register 1	Read/Write	IMR1	Read/Write	-(1)	N	N
0x0B4	Interrupt Mode Register 1	Set	IMR1S	Write-only		N	N
0x0B8	Interrupt Mode Register 1	Clear	IMR1C	Write-only		N	N
0x0BC	Interrupt Mode Register 1	Toggle	IMR1T	Write-only		N	N

23.7.4 Interlinked Multiple Value Channel Select

Name: IMCHSEL

Access Type: Write-only

Offset: 0x0C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
SEL3							
23	22	21	20	19	18	17	16
SEL2							
15	14	13	12	11	10	9	8
SEL1							
7	6	5	4	3	2	1	0
SEL0							

- **SELn: Channel Select**

  The duty cycle of the PWMA channel SELn will be updated with the value in the DUTYn field of the IMDUTY register when IMCHSEL is written. If SELn points to a non-implemented channel, the write will be discarded.

Note: The duty registers will be updated with the value stored in the IMDUTY register when the IMCHSEL register is written. Synchronization takes place immeidately when an IMCHSEL register is written. The duty cycle registers will, however, not be updated until the synchronization is completed and the timebase counter reaches its top value in order to avoid glitches.

23.8 Module Configuration

The specific configuration for each PWMA instance is listed in the following tables. The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 23-4. PWMA Configuration

Feature	PWMA
Number of PWM channels	36
Channels supporting incoming peripheral events	0, 6, 8, 9, 11, 14, 19, and 20
PWMA channels with Open Drain mode	21, 27, and 28

Table 23-5. PWMA Clocks

Clock Name	Descripton
CLK_PWMA	Clock for the PWMA bus interface
GCLK	The generic clock used for the PWMA is GCLK3

Table 23-6. Register Reset Values

Register	Reset Value
VERSION	0x00000101
PARAMETER	0x00000024

24.7 User Interface

Table 24-3. TC Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Channel 0 Control Register	CCR0	Write-only	0x00000000
0x04	Channel 0 Mode Register	CMR0	Read/Write	0x00000000
0x10	Channel 0 Counter Value	CV0	Read-only	0x00000000
0x14	Channel 0 Register A	RA0	Read/Write(1)	0x00000000
0x18	Channel 0 Register B	RB0	Read/Write(1)	0x00000000
0x1C	Channel 0 Register C	RC0	Read/Write	0x00000000
0x20	Channel 0 Status Register	SR0	Read-only	0x00000000
0x24	Interrupt Enable Register	IER0	Write-only	0x00000000
0x28	Channel 0 Interrupt Disable Register	IDR0	Write-only	0x00000000
0x2C	Channel 0 Interrupt Mask Register	IMR0	Read-only	0x00000000
0x40	Channel 1 Control Register	CCR1	Write-only	0x00000000
0x44	Channel 1 Mode Register	CMR1	Read/Write	0x00000000
0x50	Channel 1 Counter Value	CV1	Read-only	0x00000000
0x54	Channel 1 Register A	RA1	Read/Write(1)	0x00000000
0x58	Channel 1 Register B	RB1	Read/Write(1)	0x00000000
0x5C	Channel 1 Register C	RC1	Read/Write	0x00000000
0x60	Channel 1 Status Register	SR1	Read-only	0x00000000
0x64	Channel 1 Interrupt Enable Register	IER1	Write-only	0x00000000
0x68	Channel 1 Interrupt Disable Register	IDR1	Write-only	0x00000000
0x6C	Channel 1 Interrupt Mask Register	IMR1	Read-only	0x00000000
0x80	Channel 2 Control Register	CCR2	Write-only	0x00000000
0x84	Channel 2 Mode Register	CMR2	Read/Write	0x00000000
0x90	Channel 2 Counter Value	CV2	Read-only	0x00000000
0x94	Channel 2 Register A	RA2	Read/Write(1)	0x00000000
0x98	Channel 2 Register B	RB2	Read/Write(1)	0x00000000
0x9C	Channel 2 Register C	RC2	Read/Write	0x00000000
0xA0	Channel 2 Status Register	SR2	Read-only	0x00000000
0xA4	Channel 2 Interrupt Enable Register	IER2	Write-only	0x00000000
0xA8	Channel 2 Interrupt Disable Register	IDR2	Write-only	0x00000000
0xAC	Channel 2 Interrupt Mask Register	IMR2	Read-only	0x00000000
0xC0	Block Control Register	BCR	Write-only	0x00000000
0xC4	Block Mode Register	BMR	Read/Write	0x00000000
0xF8	Features Register	FEATURES	Read-only	-(2)
0xFC	Version Register	VERSION	Read-only	-(2)

0: TIOB is used as an external trigger.

- **ETRGEDG: External Trigger Edge Selection**

ETRGEDG	Edge
0	none
1	rising edge
2	falling edge
3	each edge

- **LDBDIS: Counter Clock Disable with RB Loading**
  1: Counter clock is disabled when RB loading occurs.
  0: Counter clock is not disabled when RB loading occurs.
- **LDBSTOP: Counter Clock Stopped with RB Loading**
  1: Counter clock is stopped when RB loading occurs.
  0: Counter clock is not stopped when RB loading occurs.
- **BURST: Burst Signal Selection**

BURST	Burst Signal Selection
0	The clock is not gated by an external signal
1	XC0 is ANDed with the selected clock
2	XC1 is ANDed with the selected clock
3	XC2 is ANDed with the selected clock

- **CLKI: Clock Invert**
  1: The counter is incremented on falling edge of the clock.
  0: The counter is incremented on rising edge of the clock.
- **TCCLKS: Clock Selection**

TCCLKS	Clock Selected
0	TIMER_CLOCK1
1	TIMER_CLOCK2
2	TIMER_CLOCK3
3	TIMER_CLOCK4
4	TIMER_CLOCK5
5	XC0
6	XC1
7	XC2

26.7.4 Resistive Touch Screen Sequencer

The Resistive Touch Screen Sequencer is responsible for applying voltage to the resistive touch screen films as described in Section 26.7.2. This is done by controlling the output enable and the output value of the ADP and AD pins. This allows the Resistive Touch Screen Sequencer to add a voltage gradient on one film while keeping the other film floating so a touch can be measured.

The Resistive Touch Screen Sequencer will when measuring the vertical position, apply VDD and GND to the pins connected to X_P and X_M. The Y_P and Y_M pins are put in tristate mode so the measurement of Y_P can proceed without interference. To compensate for ADC offset errors and non ideal pad drivers, the actual voltage of X_P and X_M is measured as well, so the real values for VDD and GND can be used in the contact point calculation to increase accuracy. See second formula in Section 26.7.2.

When the vertical values are converted the same setup is applies for the second axes, by setting X_P and X_M in tristate mode and applying VDD and GND to Y_P and Y_M. Refer to Section 26.8.3 for details.

26.7.5 Pen Detect

If no contact is applied to the resistive touch screen films, any resistive touch screen conversion result will be undefined as the film being measured is floating. This can be avoided by enabling Pen Detect and only trigger resistive touch screen conversions when the Pen Contact (PENCNT) status bit in the Status Register (SR) is one. Pen Detect is enabled by writing a one to the Pen Detect (PENDET) bit in the Mode Register (MR).

When Pen Detect is enabled, the ADCIFB grounds the vertical panel by applying GND to X_P and X_M and polarizes the horizontal panel by enabling pull-up on the pin connected to Y_P. The Y_M pin will in this mode be tristated. Since there is no contact, no current is flowing and there is no related power consumption. As soon as a contact occurs, GND will propagate to Y_M by pulling down Y_P, allowing the contact to be registered by the ADCIFB.

A programmable debouncing filter can be used to filter out false pen detects because of noise. The debouncing filter is programmable from one CLK_ADC period and up to 2^{15} CLK_ADC periods. The debouncer length is set by writing to the PENDBC field in MR.

This bit is set when pen contact is detected and pen detect is enabled.

- **OVRE: Overrun Error Status**
  This bit is cleared when no Overrun Error has occurred since the start of a conversion sequence.
  This bit is set when one or more Overrun Error has occurred since the start of a conversion sequence.
- **DRDY: Data Ready Status**
  0: No data has been converted since the last reset.
  1: One or more conversions have completed since the last reset and data is available in LCDR.
  This bit is cleared when CR.SWRST is written to one.
  This bit is set when one or more conversions have completed and data is available in LCDR.

Because the CAT module is configured with Peripheral DMA Controller capability that can transfer data from memory to MBLEN and from ACOUNT to memory, the Peripheral DMA Controller can perform long acquisition sequences and store results in memory without CPU intervention.

28.6.2 Prescaler and Charge Length

Each QTouch acquisition type (autonomous QTouch, QTouch group A, and QTouch group B) has its own prescaler. Each QTouch prescaler divides down the CLK_CAT clock to an appropriate sampling frequency for its particular acquisition type. Typical frequencies are 1 MHz for QTouch acquisition and 4 MHz for QMatrix burst timing control.

Each QTouch prescaler is controlled by the DIV field in the appropriate Configuration Register 0 (ATCFG0, TGACFG0, or TGBCFG0). The QMatrix burst timing prescaler is controlled by the DIV field in MGCFG0. Each prescaler uses the following formula to generate the sampling clock:

Sampling clock = CLK_CAT / (2(DIV+1))

The capacitive sensor charge length, discharge length, and settle length can be determined for each acquisition type using the CHLEN, DILEN, and SELEN fields in Configuration Registers 0 and 1. The lengths are specified in terms of prescaler clocks. In addition, the QMatrix Cx discharge length can be determined using the CXDILEN field in MGCFG2.

For QMatrix acquisition, the duration of CHLEN should not be set to the same value as the period of any periodic signal on any other pin. If the duration of CHLEN is the same as the period of a signal on another pin, it is likely that the other signal will significantly affect measurements due to stray capacitive coupling. For example, if a 1 MHz signal is generated on another pin of the device, then CHLEN should not be 1 microsecond.

For the QMatrix method, burst and capture lengths are set for each (X,Y) pair by writing the desired length values to the MBLEN register. The write must be done before each X line can start its acquisition and is indicated by the status bit MBLREQ in the Status Register (SR). A DMA handshake interface is also connected to this status bit to reduce CPU overhead during QMatrix acquisitions.

Four burst lengths (BURST0..3) can be written at one time into the MBLEN register. If the current configuration uses Y lines larger than Y3 the register has to be written a second time. The first write to MBLEN specifies the burst length for Y lines 0 to 3 in the BURST0 to BURST3 fields, respectively. The second write specifies the burst length for Y lines 4 to 7 in fields BURST0 to BURST3, respectively, and so on.

The Y and YK pins remain clamped to ground apart from the specified number of burst pulses, when charge is transferred and captured into the sampling capacitor.

28.6.3 Capacitive Count Acquisition

For the QMatrix, QTouch group A, and QTouch group B types of acquisition, the module acquires count values from the sensors, buffers them, and makes them available for reading in the ACOUNT register. Further processing of the count values must be performed by the CPU.

When the module performs QMatrix acquisition using multiple Y lines, it starts the capture for each Y line at the appropriate time in the burst sequence so that all captures finish simultaneously. For example, suppose that an acquisition is performed on Y0 and Y1 with BURST0=53 and BURST1=60. The module will first toggle the X line 7 times while capturing on Y1 while Y0 and YK0 are clamped to ground. The module will then toggle the X line 53 times while capturing on both Y1 and Y0.

28.7 User Interface

Table 28-3. CAT Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Control Register	CTRL	Read/Write	0x00000000
0x04	Autonomous Touch Pin Selection Register	ATPINS	Read/Write	0x00000000
0x08	Pin Mode Register 0	PINMODE0	Read/Write	0x00000000
0x0C	Pin Mode Register 1	PINMODE1	Read/Write	0x00000000
0x10	Autonomous Touch Configuration Register 0	ATCFG0	Read/Write	0x00000000
0x14	Autonomous Touch Configuration Register 1	ATCFG1	Read/Write	0x00000000
0x18	Autonomous Touch Configuration Register 2	ATCFG2	Read/Write	0x00000000
0x1C	Autonomous Touch Configuration Register 3	ATCFG3	Read/Write	0x00000000
0x20	Touch Group A Configuration Register 0	TGACFG0	Read/Write	0x00000000
0x24	Touch Group A Configuration Register 1	TGACFG1	Read/Write	0x00000000
0x28	Touch Group B Configuration Register 0	TGBCFG0	Read/Write	0x00000000
0x2C	Touch Group B Configuration Register 1	TGBCFG1	Read/Write	0x00000000
0x30	Matrix Group Configuration Register 0	MGCFG0	Read/Write	0x00000000
0x34	Matrix Group Configuration Register 1	MGCFG1	Read/Write	0x00000000
0x38	Matrix Group Configuration Register 2	MGCFG2	Read/Write	0x00000000
0x3C	Status Register	SR	Read-only	0x00000000
0x40	Status Clear Register	SCR	Write-only	-
0x44	Interrupt Enable Register	IER	Write-only	-
0x48	Interrupt Disable Register	IDR	Write-only	-
0x4C	Interrupt Mask Register	IMR	Read-only	0x00000000
0x50	Acquisition Initiation and Selection Register	AISR	Read/Write	0x00000000
0x54	Acquired Count Register	ACOUNT	Read-only	0x00000000
0x58	Matrix Burst Length Register	MBLEN	Write-only	-
0x5C	Discharge Current Source Register	DICS	Read/Write	0x00000000
0x60	Spread Spectrum Configuration Register	SSCFG	Read/Write	0x00000000
0x64	CSA Resistor Control Register	CSARES	Read/Write	0x00000000
0x68	CSB Resistor Control Register	CSBRES	Read/Write	0x00000000
0x6C	Autonomous Touch Base Count Register	ATBASE	Read-only	0x00000000
0x70	Autonomous Touch Current Count Register	ATCURR	Read-only	0x00000000
0x80	Analog Comparator Shift Offset Register 0	ACSHI0	Read/Write	0x00000000
0x84	Analog Comparator Shift Offset Register 1	ACSHI1	Read/Write	0x00000000
0x88	Analog Comparator Shift Offset Register 2	ACSHI2	Read/Write	0x00000000
0x8C	Analog Comparator Shift Offset Register 3	ACSHI3	Read/Write	0x00000000
0x90	Analog Comparator Shift Offset Register 4	ACSHI4	Read/Write	0x00000000
0x94	Analog Comparator Shift Offset Register 5	ACSHI5	Read/Write	0x00000000

Table 31-59. STATUS_INFO Details

Response	Details
Response value	0xC4
Additional data	2 status bytes

31.6.8.8 MEMORY_SPEED

Counts the number of RC120M clock cycles it takes to sync one message to the SAB interface and back again. The SAB clock speed (f_{sab}) can be calculated using the following formula:

$$f_{sab} = \frac{3f_{aw}}{CV - 3}$$

Table 31-60. MEMORY_SPEED Details

Response	Details
Response value	0xC5
Additional data	Clock cycle count (MS)

31.6.9 Security Restrictions

When the security fuse in the Flash is programmed, the following aWire commands are limited:

- MEMORY_WRITE
- MEMORY_READ

Unlimited access to these instructions is restored when the security fuse is erased by the CHIP_ERASE aWire command.

Note that the security bit will read as programmed and block these instructions also if the Flash Controller is statically reset.