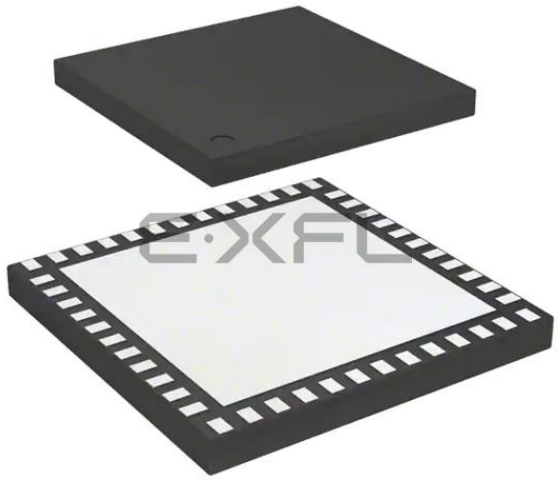

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFLGA Exposed Pad
Supplier Device Package	48-TLLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l064-d3hr

7.7.21 Performance Channel 0 Write Data Cycles

Name: PWDATA0

Access Type: Read-only

Offset: 0x810

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA[31:24]							

23	22	21	20	19	18	17	16
DATA[23:16]							

15	14	13	12	11	10	9	8
DATA[15:8]							

7	6	5	4	3	2	1	0
DATA[7:0]							

- **DATA: Data Cycles Counted Since Last Reset**
  Clock cycles are counted using the CLK_PDCA_HSB clock

7.7.25 Performance Channel 1 Read Stall Cycles

Name: PRSTALL1

Access Type: Read-only

Offset: 0x820

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
STALL[31:24]							

23	22	21	20	19	18	17	16
STALL[23:16]							

15	14	13	12	11	10	9	8
STALL[15:8]							

7	6	5	4	3	2	1	0
STALL[7:0]							

- **STALL: Stall Cycles Counted Since Last Reset**
  Clock cycles are counted using the CLK_PDCA_HSB clock

8.8.4 Flash Parameter Register

Name: FPR

Access Type: Read-only

Offset: 0x0C

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	PSZ		

7	6	5	4	3	2	1	0
-	-	-	-	FSZ			

- **PSZ: Page Size**
  The size of each flash page.

Table 8-9. Flash Page Size

PSZ	Page Size
0	32 Byte
1	64 Byte
2	128 Byte
3	256 Byte
4	512 Byte
5	1024 Byte
6	2048 Byte
7	4096 Byte

Table 10-1. HMATRIX Register Memory Map (Continued)

Offset	Register	Name	Access	Reset Value
0x012C	Special Function Register 7	SFR7	Read/Write	–
0x0130	Special Function Register 8	SFR8	Read/Write	–
0x0134	Special Function Register 9	SFR9	Read/Write	–
0x0138	Special Function Register 10	SFR10	Read/Write	–
0x013C	Special Function Register 11	SFR11	Read/Write	–
0x0140	Special Function Register 12	SFR12	Read/Write	–
0x0144	Special Function Register 13	SFR13	Read/Write	–
0x0148	Special Function Register 14	SFR14	Read/Write	–
0x014C	Special Function Register 15	SFR15	Read/Write	–

- **ON: Voltage Regulator On Status**
  0: The voltage regulator is currently disabled.
  1: The voltage regulator is currently enabled.
  This bit is read-only. Writing to this bit has no effect.
- **VREGOK: Voltage Regulator OK Status**
  0: The voltage regulator is disabled or has not yet reached a stable output voltage.
  1: The voltage regulator has reached the output voltage threshold level after being enabled.
  This bit is read-only. Writing to this bit has no effect.
- **EN: Enable**
  0: The voltage regulator is disabled.
  1: The voltage regulator is enabled.
  Note: This bit is set after a Power-on Reset (POR).
- **SELVDD: Select VDD**
  Output voltage of the Voltage Regulator. The default value of this bit corresponds to an output voltage of 1.8V.

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

13.6.24 Generic Clock Control

Name: GCCTRL

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DIV[15:8]							

23	22	21	20	19	18	17	16
DIV[7:0]							

15	14	13	12	11	10	9	8
-	-	-	OSCSEL[4:0]				

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DIVEN	CEN

There is one GCCTRL register per generic clock in the design.

- **DIV: Division Factor**
  The number of DIV bits for each generic clock is as shown in the “Generic Clock number of DIV bits” table in the SCIF Module Configuration section.
- **OSCSEL: Oscillator Select**
  Selects the source clock for the generic clock. Please refer to the “Generic Clock Sources” table in the SCIF Module Configuration section.
- **DIVEN: Divide Enable**
  0: The generic clock equals the undivided source clock.
  1: The generic clock equals the source clock divided by 2*(DIV+1).
- **CEN: Clock Enable**
  0: The generic clock is disabled.
  1: The generic clock is enabled.

Table 13-13. Register Reset Values

Register	Reset Value
OSC0VERSION	0x00000100
OSC32VERSION	0x00000101
DFLLIFVERSION	0x00000201
BODIFAVERSION	0x00000101
VREGIFBVERSION	0x00000101
RCOSCIFAVERSION	0x00000101
SM33IFAVERSION	0x00000100
TSENSEIFAVERSION	0x00000100
RC120MIFAVERSION	0x00000101
BRIFAVERSION	0x00000100
RC32KIFAVERSION	0x00000100
GCLKVERSION	0x00000100
VERSION	0x00000102

The peripheral event will be generated if the corresponding bit in the Event Mask (EVM) register is set. Bits in EVM register are set by writing a one to the corresponding bit in the Event Enable (EVE) register, and cleared by writing a one to the corresponding bit in the Event Disable (EVD) register.

14.5.5 AST wakeup

The AST can wake up the CPU directly, without the need to trigger an interrupt. A wakeup can be generated when the counter overflows, when the counter reaches the selected alarm value, or when the selected prescaler bit has a 0-to-1 transition. In this case, the CPU will continue executing from the instruction following the sleep instruction.

The AST wakeup is enabled by writing a one to the corresponding bit in the Wake Enable Register (WER). When the CPU wakes from sleep, the wake signal must be cleared by writing a one to the corresponding bit in SCR to clear the internal wake signal to the sleep controller. If the wake signal is not cleared after waking from sleep, the next sleep instruction will have no effect because the CPU will wake immediately after this sleep instruction.

The AST wakeup can wake the CPU from any sleep mode where the source clock is active. The AST wakeup can be configured independently of the interrupt masking.

14.5.6 Shutdown Mode

If the AST is configured to use a clock that is available in Shutdown mode, the AST can be used to wake up the system from shutdown. Both the alarm wakeup, periodic wakeup, and overflow wakeup mechanisms can be used in this mode.

When waking up from Shutdown mode all control registers will have the same value as before the shutdown was entered, except the Interrupt Mask Register (IMR). IMR will be reset with all interrupts turned off. The software must first reconfigure the interrupt controller and then enable the interrupts in the AST to again receive interrupts from the AST.

The CV register will be updated with the current counter value directly after wakeup from shutdown. The SR will show the status of the AST, including the status bits set during shutdown operation.

When waking up the system from shutdown the CPU will start executing code from the reset start address.

14.5.7 Digital Tuner

The digital tuner adds the possibility to compensate for a too-slow or a too-fast input clock. The ADD bit in the Digital Tuner Register (DTR.ADD) selects if the prescaler frequency should be reduced or increased. If ADD is ‘0’, the prescaler frequency is reduced:

$$f_{TUNED} = f_0\left(1 - \frac{1}{\text{roundup}\left(\frac{256}{VALUE}\right)\cdot(2^{EXP})+1}\right)$$

where f_{TUNED} is the tuned frequency, f_0 is the original prescaler frequency, and VALUE and EXP are the corresponding fields to be programmed in DTR. Note that DTR.EXP must be greater than zero. Frequency tuning is disabled by programming DTR.VALUE as zero.

15.7 Module Configuration

The specific configuration for each WDT instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 15-2. WDT Clocks

Clock Name	Description
CLK_WDT	Clock for the WDT bus interface

Table 15-3. Register Reset Values

Register	Reset Value
VERSION	0x00000402

18.8 Module Configuration

The specific configuration for each GPIO instance is listed in the following tables. The module bus clocks listed here are connected to the system bus clocks. Refer to the Power Manager chapter for details.

Table 18-3. GPIO Configuration

Feature	GPIO
Number of GPIO ports	2
Number of peripheral functions	8

Table 18-4. Implemented Pin Functions

Pin Function	Implemented	Notes
Pull-up	On all pins	Controlled by PUER or peripheral

Table 18-5. GPIO Clocks

Module Name	Clock Name	Description
GPIO	CLK_GPIO	Clock for the GPIO bus interface

The reset values for all GPIO registers are zero, with the following exceptions:

Table 18-6. Register Reset Values

Port	Register	Reset Value
0	GPER	0x004DFF5F
0	PMR0	0x00320020
0	PMR1	0x00020080
0	PMR2	0x00100800
0	PUER	0x00000001
0	GFER	0x007FFFFF
0	PARAMETER	0x007FFFFF
0	VERSION	0x00000211
1	GPER	0x00001FCF
1	PMR0	0x00000030
1	PMR1	0x00000030
1	GFER	0x00001FFF
1	PARAMETER	0x00001FFF
1	VERSION	0x00000211

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with NCPHA to produce the required clock/data relationship between master and slave devices.

21.8.2.2 Setting up and Performing a Transfer

Operation of the TWIM is mainly controlled by the Control Register (CR) and the Command Register (CMDR). TWIM status is provided in the Status Register (SR). The following list presents the main steps in a typical communication:

1. Before any transfers can be performed, bus timings must be configured by writing to the Clock Waveform Generator Register (CWGR). If operating in SMBus mode, the SMBus Timing Register (SMBTR) register must also be configured.
2. If the Peripheral DMA Controller is to be used for the transfers, it must be set up.
3. CMDR or NCMDR must be written with a value describing the transfer to be performed.

The interrupt system can be set up to give interrupt requests on specific events or error conditions in the SR, for example when the transfer is complete or if arbitration is lost. The Interrupt Enable Register (IER) and Interrupt Disable Register (IDR) can be written to specify which bits in the SR will generate interrupt requests.

The SR.BUSFREE bit is set when activity is completed on the two-wire bus. The SR.CRDY bit is set when CMDR and/or NCMDR is ready to receive one or more commands.

The controller will refuse to start a new transfer while ANAK, DNAK, or ARBLST in the Status Register (SR) is one. This is necessary to avoid a race when the software issues a continuation of the current transfer at the same time as one of these errors happen. Also, if ANAK or DNAK occurs, a STOP condition is sent automatically. The user will have to restart the transmission by clearing the error bits in SR after resolving the cause for the NACK.

After a data or address NACK from the slave, a STOP will be transmitted automatically. Note that the VALID bit in CMDR is NOT cleared in this case. If this transfer is to be discarded, the VALID bit can be cleared manually allowing any command in NCMDR to be copied into CMDR.

When a data or address NACK is returned by the slave while the master is transmitting, it is possible that new data has already been written to the THR register. This data will be transferred out as the first data byte of the next transfer. If this behavior is to be avoided, the safest approach is to perform a software reset of the TWIM.

21.8.3 Master Transmitter Mode

A START condition is transmitted and master transmitter mode is initiated when the bus is free and CMDR has been written with START=1 and READ=0. START and SADR+W will then be transmitted. During the address acknowledge clock pulse (9th pulse), the master releases the data line (HIGH), enabling the slave to pull it down in order to acknowledge the address. The master polls the data line during this clock pulse and sets the Address Not Acknowledged bit (ANAK**)** in the Status Register if no slave acknowledges the address.

After the address phase, the following is repeated:

while (NBYTES>0)

1. Wait until THR contains a valid data byte, stretching low period of TWCK. SR.TXRDY indicates the state of THR. Software or the Peripheral DMA Controller must write the data byte to THR.
2. Transmit this data byte
3. Decrement NBYTES
4. If (NBYTES==0) and STOP=1, transmit STOP condition

Writing CMDR with START=STOP=1 and NBYTES=0 will generate a transmission with no data bytes, ie START, SADR+W, STOP.

21.9.7 Transmit Holding Register

Name: THR

Access Type: Write-only

Offset: 0x18

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
TXDATA							

- **TXDATA: Data to Transmit**
  Write data to be transferred on the TWI bus here.

22.9.12 Parameter Register

Name: PR

Access Type: Read-only

Offset: 0x2C

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

22.10 Module Configuration

The specific configuration for each TWIS instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 22-7. Module Clock Name

Module Name	Clock Name	Description
TWIS0	CLK_TWIS0	Clock for the TWIS0 bus interface
TWIS1	CLK_TWIS1	Clock for the TWIS1 bus interface

Table 22-8. Register Reset Values

Register	Reset Value
VERSION	0x00000112
PARAMETER	0x00000000

24.7.6 Channel Register B

Name: RB

Access Type: Read-only if CMRn.WAVE = 0, Read/Write if CMRn.WAVE = 1

Offset: 0x18 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
RB[15:8]							

7	6	5	4	3	2	1	0
RB[7:0]							

- **RB: Register B**
  RB contains the Register B value in real time.

27.9.3 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	WFINT3	WFINT2	WFINT1	WFINT0
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
SUTINT7	ACINT7	SUTINT6	ACINT6	SUTINT5	ACINT5	SUTINT4	ACINT4
7	6	5	4	3	2	1	0
SUTINT3	ACINT3	SUTINT2	ACINT2	SUTINT1	ACINT1	SUTINT0	ACINT0

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will set the corresponding bit in IMR.

31.4.5.1 I/O Lines

The TMS, TDI, TDO, and TCK pins are multiplexed with I/O lines. When the JTAG is used the associated pins must be enabled. To enable the JTAG pins, refer to Section 31.4.7.

While using the multiplexed JTAG lines all normal peripheral activity on these lines is disabled. The user must make sure that no external peripheral is blocking the JTAG lines while debugging.

31.4.5.2 Power Management

When an instruction that accesses the SAB is loaded in the instruction register, before entering a sleep mode, the system clocks are not switched off to allow debugging in sleep modes. This can lead to a program behaving differently when debugging.

31.4.5.3 Clocks

The JTAG Interface uses the external TCK pin as clock source. This clock must be provided by the JTAG master.

Instructions that use the SAB bus requires the internal main clock to be running.

31.4.6 JTAG Interface

The JTAG Interface is accessed through the dedicated JTAG pins shown in Table 31-8 on page 729. The TMS control line navigates the TAP controller, as shown in Figure 31-6 on page 731. The TAP controller manages the serial access to the JTAG Instruction and Data registers. Data is scanned into the selected instruction or data register on TDI, and out of the register on TDO, in the Shift-IR and Shift-DR states, respectively. The LSB is shifted in and out first. TDO is high-Z in other states than Shift-IR and Shift-DR.

The device implements a 5-bit Instruction Register (IR). A number of public JTAG instructions defined by the JTAG standard are supported, as described in Section 31.5.2, as well as a number of 32-bit AVR-specific private JTAG instructions described in Section 31.5.3. Each instruction selects a specific data register for the Shift-DR path, as described for each instruction.

31.5.4.3 Boundary-Scan Chain

The Boundary-Scan Chain has the capability of driving and observing the logic levels on the digital I/O pins, as well as driving and observing the logic levels between the digital I/O pins and the internal logic. Typically, output value, output enable, and input data are all available in the boundary scan chain.

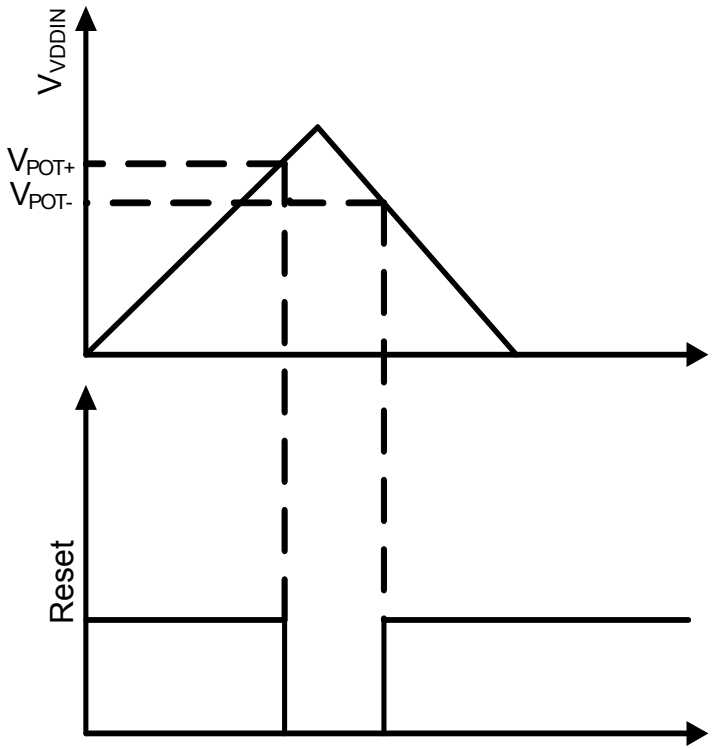
The boundary scan chain is described in the BDSL (Boundary Scan Description Language) file available at the Atmel web site.

32.8.3 Power-on Reset 33 Characteristics

Table 32-24. POR33 Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT+}	Voltage threshold on V_{VDDIN} rising			1.49	1.58	V
V_{POT-}	Voltage threshold on V_{VDDIN} falling		1.3	1.45		
t_{DET}	Detection time	Time with VDDIN < V_{POT-} necessary to generate a reset signal		460		µs
I_{POR33}	Current consumption	After t_{RESET}		15		µA
$t_{STARTUP}$	Startup time			400		µs

Figure 32-6. POR33 Operating Principles



32.8.4 Brown Out Detector Characteristics

The values in Table 32-25 describe the values of the BODLEVEL in the flash General Purpose Fuse register.

Table 32-25. BODLEVEL Values

BODLEVEL Value	Min	Typ	Max	Units
011111 binary (31) 0x1F		1.56		V
100111 binary (39) 0x27		1.65		