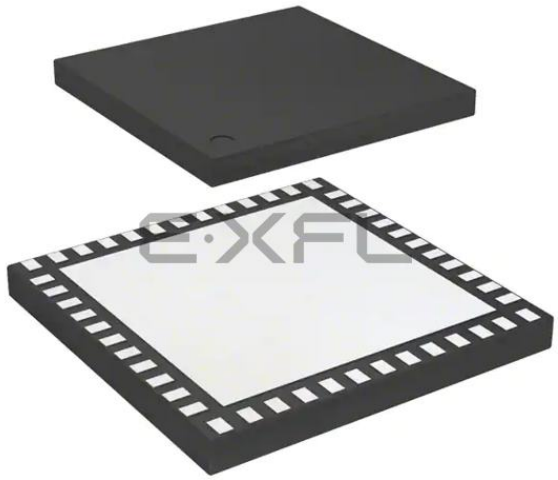

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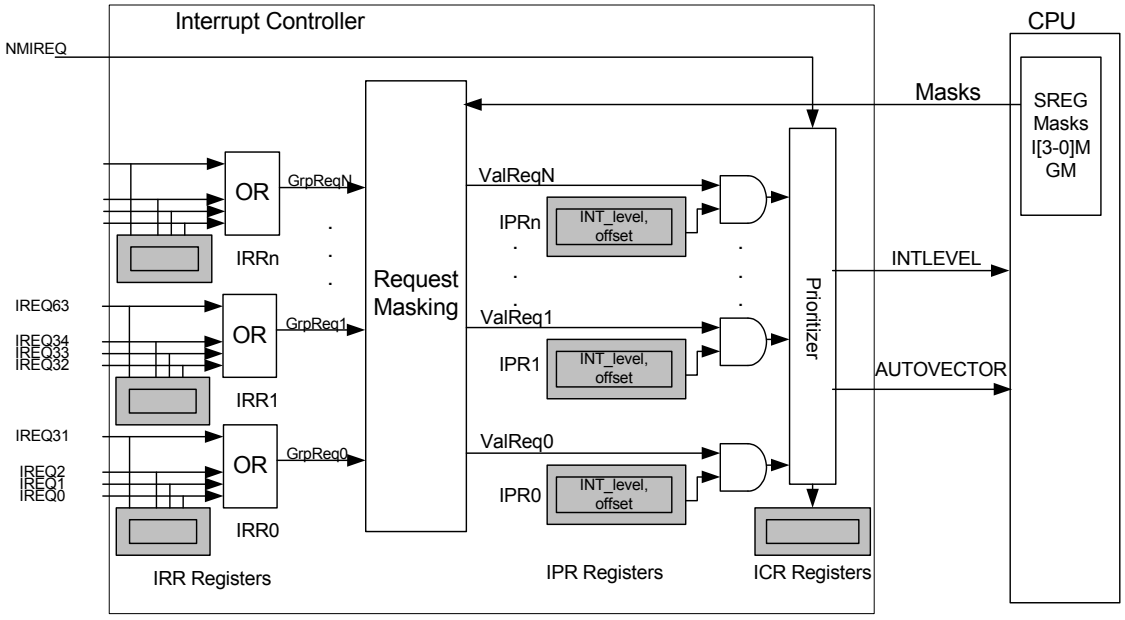
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFLGA Exposed Pad
Supplier Device Package	48-TLLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l064-d3ur

Figure 11-1. INTC Block Diagram



11.4 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

11.4.1 Power Management

If the CPU enters a sleep mode that disables CLK_SYNC, the INTC will stop functioning and resume operation after the system wakes up from sleep mode.

11.4.2 Clocks

The clock for the INTC bus interface (CLK_INTC) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager.

The INTC sampling logic runs on a clock which is stopped in any of the sleep modes where the system RC oscillator is not running. This clock is referred to as CLK_SYNC. This clock is enabled at reset, and only turned off in sleep modes where the system RC oscillator is stopped.

11.4.3 Debug Operation

When an external debugger forces the CPU into debug mode, the INTC continues normal operation.

11.5 Functional Description

All of the incoming interrupt requests (IREQs) are sampled into the corresponding Interrupt Request Register (IRR). The IRRs must be accessed to identify which IREQ within a group that is active. If several IREQs within the same group are active, the interrupt service routine must prioritize between them. All of the input lines in each group are logically ORed together to form the GrpReqN lines, indicating if there is a pending interrupt in the corresponding group.

The Request Masking hardware maps each of the GrpReq lines to a priority level from INT0 to INT3 by associating each group with the Interrupt Level (INTLEVEL) field in the corresponding

12.7.12 Interrupt Status Register

Name: ISR

Access Type: Read-only

Offset: 0x0CC

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
AE	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	CKRDY	-	-	-	-	CFD

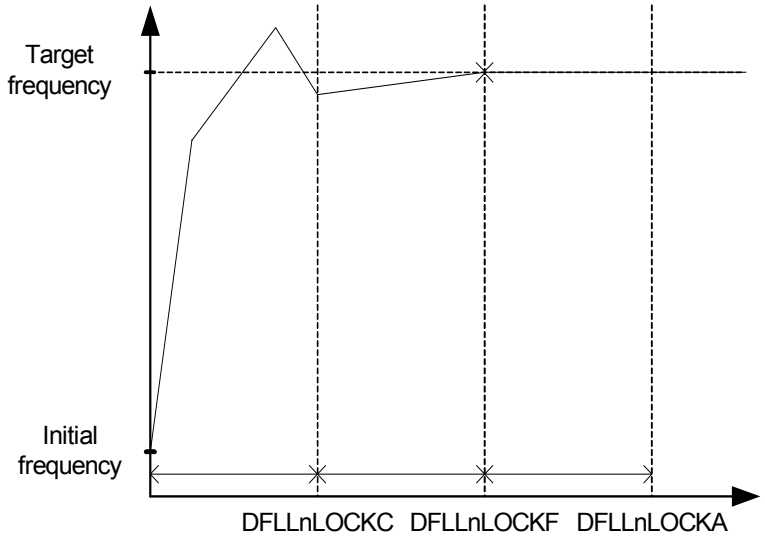
0: The corresponding interrupt is cleared.

1: The corresponding interrupt is pending.

This bit is cleared when the corresponding bit in ICR is written to one.

This bit is set on a zero-to-one transition of the corresponding bit in the Status Register (SR).

Figure 13-3. DFLL Locking in Closed loop



CLK_DFLL is ready to be used when the DFLLn Synchronization Ready bit (DFLLnRDY) in PCLKSR is set after enabling the DFLL. However, the accuracy of the output frequency depends on which locks are set.

For lock times, please refer to the Electrical Characteristics chapter.

Drift compensation

The frequency tuner will automatically compensate for drift in the f_{DFLL} without losing either of the locks. If the FINE value overflows or underflows, which should normally not happen, but could occur due to large drift in temperature and voltage, all locks will be lost, and the COARSE and FINE values will be recalibrated as described earlier. If any lock is lost the corresponding bit in PCLKSR will be set, DFLLn Lock Lost on Coarse Value bit (DFLLnLOCKLOSTC) for lock lost on COARSE value, DFLLn Lock Lost on Fine Value bit (DFLLnLOCKLOSTF) for lock lost on FINE value and DFLLn Lock Lost on Accurate Value bit (DFLLnLOCKLOSTA) for lock lost on ACCURATE value. The corresponding lock status bit will be cleared when the lock lost bit is set, and vice versa.

Reference clock stop detection

If CLK_DFLLIF_REF stops or is running at a very slow frequency, the DFLLn Reference Clock Stopped bit (DFLLnRCS) in PCLKSR will be set. Note that the detection of the clock stop will take a long time. The DFLLIF operate as if it was in open loop mode if it detects that the reference clock has stopped. This means that the COARSE and FINE values will be kept constant while PCLKSR.DFLLnRCS is set. Closed loop mode operation will automatically resume if the CLK_DFLLIF_REF is restarted, and compensate for any drift during the time CLK_DFLLIF_REF was stopped. No locks will be lost.

Frequency error measurement

The ratio between CLK_DFLLIF_REF and CLK_DFLL is measured automatically by the DFLLIF. The difference between this ratio and DFLLnMUL is stored in the Multiplication Ratio Difference field (RATIODIFF) in the DFLLn Ratio Register (DFLLnRATIO). The relative error on CLK_DFLL compared to the target frequency can be calculated as follows:

writing a zero to CEN the other bits in GCCTRL should not be changed until CEN reads as zero, to avoid glitches on the generic clock. The generic clocks will be automatically re-enabled when waking from sleep.

13.5.13.3 Changing clock frequency

When changing the generic clock frequency by changing OSCSEL or DIV, the clock should be disabled before being re-enabled with the new clock source or division setting. This prevents glitches during the transition.

13.5.13.4 Generic clock allocation

The generic clocks are allocated to different functions as shown in the “Generic Clock Allocation” table in the SCIF Module Configuration section.

13.5.14 Interrupts

The SCIF has the following interrupt sources:

- AE - Access Error:
  - A protected SCIF register was accessed without first being correctly unlocked.
- BRIFARDY - Backup Register Interface Ready.
  - A 0 to 1 transition on the PCLKSR.BRIFARDY bit is detected.
- DFLL0RCS - DFLL Reference Clock Stopped:
  - A 0 to 1 transition on the PCLKSR.DFLLRCS bit is detected.
- DFLL0RDY - DFLL Ready:
  - A 0 to 1 transition on the PCLKSR.DFLLRDY bit is detected.
- DFLL0LOCKLOSTA - DFLL lock lost on Accurate value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKLOSTA bit is detected.
- DFLL0LOCKLOSTF - DFLL lock lost on Fine value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKLOSTF bit is detected.
- DFLL0LOCKLOSTC - DFLL lock lost on Coarse value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKLOSTC bit is detected.
- DFLL0LOCKA - DFLL Locked on Accurate value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKA bit is detected.
- DFLL0LOCKF - DFLL Locked on Fine value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKF bit is detected.
- DFLL0LOCKC - DFLL Locked on Coarse value:
  - A 0 to 1 transition on the PCLKSR.DFLLLOCKC bit is detected.
- BODDET - Brown out detection:
  - A 0 to 1 transition on the PCLKSR.BODDET bit is detected.
- SM33DET - Supply Monitor 3.3V Detector:
  - A 0 to 1 transition on the PCLKSR.SM33DET bit is detected.
- VREGOK - Voltage Regulator OK:
  - A 0 to 1 transition on the PCLKSR.VREGOK bit is detected.
- OSC0RDY - Oscillator Ready:
  - A 0 to 1 transition on the PCLKSR.OSC0RDY bit is detected.

13.6.17 Voltage Regulator Calibration Register

Name: VREGCR

Access Type: Read/Write

Reset Value: -

31	30	29	28	27	26	25	24
SFV	INTPD	-	-	-	DBG-	-	-
23	22	21	20	19	18	17	16
-	-	-	POR33MASK	POR33STATUS	POR33EN	DEEPDIS	FCD
15	14	13	12	11	10	9	8
-	-	-	-	CALIB			
7	6	5	4	3	2	1	0
ON	VREGOK	EN	-	-	SELVDD		

- **SFV: Store Final Value**
  0: The register is read/write.
  1: The register is read-only, to protect against further accidental writes.
  This bit is cleared by a Power-on Reset.
- **INTPD: Internal Pull-down**
  This bit is used for test purposes only.
  0: The voltage regulator output is not pulled to ground.
  1: The voltage regulator output has a pull-down to ground.
- **POR33MASK: Power-on Reset 3.3V Output Mask**
  0: Power-on Reset 3.3V is not masked.
  1: Power-on Reset 3.3V is masked.
- **POR33STATUS: Power-on Reset 3.3V Status**
  0: Power-on Reset is disabled.
  1: Power-on Reset is enabled.
  This bit is read-only. Writing to this bit has no effect.
- **POR33EN: Power-on Reset 3.3V Enable**
  0: Writing a zero to this bit disables the POR33 detector.
  1: Writing a one to this bit enables the POR33 detector.
- **DEEPDIS: Disable Regulator Deep Mode**
  0: Regulator will enter deep mode in low-power sleep modes for lower power consumption.
  1: Regulator will stay in full-power mode in all sleep modes for shorter start-up time.
- **FCD: Flash Calibration Done**
  0: The flash calibration will be redone after any reset.
  1: The flash calibration will only be redone after a Power-on Reset.
  This bit is cleared after a Power-on Reset.
  This bit is set when the CALIB field has been updated by flash calibration after a reset.
- **CALIB: Calibration Value**
  Calibration value for Voltage Regulator. This is calibrated during production and should not be changed.

14.6.8 Wake Enable Register

Name: WER

Access Type: Read/Write

Offset: 0x1C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	PER1	PER0

15	14	13	12	11	10	9	8
-	-	-	-	-	-	ALARM1	ALARM0

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVF

When the SR.BUSY bit is set writes to this register will be discarded and this register will read as zero.

This register enables the wakeup signal from the AST.

- **PERn: Periodic n**
  0: The CPU will not wake up from sleep mode when the selected bit in the prescaler has a 0-to-1 transition.
  1: The CPU will wake up from sleep mode when the selected bit in the prescaler has a 0-to-1 transition.
- **ALARMn: Alarm n**
  0: The CPU will not wake up from sleep mode when the counter reaches the selected alarm value.
  1: The CPU will wake up from sleep mode when the counter reaches the selected alarm value.
- **OVF: Overflow**
  0: A counter overflow will not wake up the CPU from sleep mode.
  1: A counter overflow will wake up the CPU from sleep mode.

16.7.4 Interrupt Status Register

Name: ISR

Access Type: Read-only

Offset: 0x00C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	INT30	INT29	INT28	INT27	INT26	INT25	INT24
23	22	21	20	19	18	17	16
INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16
15	14	13	12	11	10	9	8
INT15	INT14	INT13	INT12	INT11	INT10	INT9	INT8
7	6	5	4	3	2	1	0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	NMI

- **INTn: External Interrupt n**
  0: An interrupt event has not occurred.
  1: An interrupt event has occurred.
  This bit is cleared by writing a one to the corresponding bit in ICR.
  Please refer to the Module Configuration section for the number of external interrupts.
- **NMI: Non-Maskable Interrupt**
  0: An interrupt event has not occurred.
  1: An interrupt event has occurred.
  This bit is cleared by writing a one to the corresponding bit in ICR.

16.7.13 Disable Register

Name: DIS

Access Type: Write-only

Offset: 0x034

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	INT30	INT29	INT28	INT27	INT26	INT25	INT24
23	22	21	20	19	18	17	16
INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16
15	14	13	12	11	10	9	8
INT15	INT14	INT13	INT12	INT11	INT10	INT9	INT8
7	6	5	4	3	2	1	0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	NMI

- **INTn: External Interrupt n**
  Writing a zero to this bit has no effect.
  Writing a one to this bit will disable the corresponding external interrupt.
  Please refer to the Module Configuration section for the number of external interrupts.
- **NMI: Non-Maskable Interrupt**
  Writing a zero to this bit has no effect.
  Writing a one to this bit will disable the Non-Maskable Interrupt.

16.7.15 Version Register

Name: VERSION

Access Type: Read-only

Offset: 0x3FC

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	VERSION[11:8]			

7	6	5	4	3	2	1	0
VERSION[7:0]							

- **VERSION: Version number**
  Version number of the module. No functionality associated.

18.7.19 Unlock Register

Name: UNLOCK

Access: Write-only

Offset: 0x1E0

Reset Value: -

31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	OFFSET	
7	6	5	4	3	2	1	0
OFFSET							

- **OFFSET: Register Offset**
  This field must be written with the offset value of the LOCK, LOCKC or LOCKT register to unlock. This offset must also include the port offset for the register to unlock. LOCKS can not be locked so no unlock is required before writing to this register.
- **KEY: Unlocking Key**
  This bitfield must be written to 0xAA for a write to this register to have an effect.

  This register always reads as zero.

18.8 Module Configuration

The specific configuration for each GPIO instance is listed in the following tables. The module bus clocks listed here are connected to the system bus clocks. Refer to the Power Manager chapter for details.

Table 18-3. GPIO Configuration

Feature	GPIO
Number of GPIO ports	2
Number of peripheral functions	8

Table 18-4. Implemented Pin Functions

Pin Function	Implemented	Notes
Pull-up	On all pins	Controlled by PUER or peripheral

Table 18-5. GPIO Clocks

Module Name	Clock Name	Description
GPIO	CLK_GPIO	Clock for the GPIO bus interface

The reset values for all GPIO registers are zero, with the following exceptions:

Table 18-6. Register Reset Values

Port	Register	Reset Value
0	GPER	0x004DFF5F
0	PMR0	0x00320020
0	PMR1	0x00020080
0	PMR2	0x00100800
0	PUER	0x00000001
0	GFER	0x007FFFFF
0	PARAMETER	0x007FFFFF
0	VERSION	0x00000211
1	GPER	0x00001FCF
1	PMR0	0x00000030
1	PMR1	0x00000030
1	GFER	0x00001FFF
1	PARAMETER	0x00001FFF
1	VERSION	0x00000211

- **BITS: Bits Per Transfer**
  The BITS field determines the number of data bits transferred. Reserved values should not be used.

BITS	Bits Per Transfer
0000	8
0001	9
0010	10
0011	11
0100	12
0101	13
0110	14
0111	15
1000	16
1001	4
1010	5
1011	6
1100	7
1101	Reserved
1110	Reserved
1111	Reserved

- **CSAAT: Chip Select Active After Transfer**
  1: The Peripheral Chip Select does not rise after the last transfer is achieved. It remains active until a new transfer is requested on a different chip select.
  0: The Peripheral Chip Select Line rises as soon as the last transfer is achieved.
- **CSNAAT: Chip Select Not Active After Transfer (Ignored if CSAAT = 1)**
  0: The Peripheral Chip Select does not rise between two transfers if the TDR is reloaded before the end of the first transfer and if the two transfers occur on the same Chip Select.
  1: The Peripheral Chip Select rises systematically between each transfer performed on the same slave for a minimal duration of:

  $\frac{DLYBCS}{CLKSPI}$ (if DLYBCT field is different from 0)

  $\frac{DLYBCS + 1}{CLK\overline{SPI}}$ (if DLYBCT field equals 0)
- **NCPHA: Clock Phase**
  1: Data is captured after the leading (inactive-to-active) edge of SPCK and changed on the trailing (active-to-inactive) edge of SPCK.
  0: Data is changed on the leading (inactive-to-active) edge of SPCK and captured after the trailing (active-to-inactive) edge of SPCK.
  NCPHA determines which edge of SPCK causes data to change and which edge causes data to be captured. NCPHA is used with CPOL to produce the required clock/data relationship between master and slave devices.
- **CPOL: Clock Polarity**
  1: The inactive state value of SPCK is logic level one.
  0: The inactive state value of SPCK is logic level zero.

3. Start the transfer by enabling the Peripheral DMA Controller to receive.
4. Wait for the Peripheral DMA Controller end-of-receive flag.
5. Disable the Peripheral DMA Controller.

22.8.6 SMBus Mode

SMBus mode is enabled by writing a one to the SMBus Mode Enable (SMEN) bit in CR. SMBus mode operation is similar to I²C operation with the following exceptions:

- Only 7-bit addressing can be used.
- The SMBus standard describes a set of timeout values to ensure progress and throughput on the bus. These timeout values must be written to TR.
- Transmissions can optionally include a CRC byte, called Packet Error Check (PEC).
- A dedicated bus line, SMBALERT, allows a slave to get a master's attention.
- A set of addresses have been reserved for protocol handling, such as Alert Response Address (ARA) and Host Header (HH) Address. Address matching on these addresses can be enabled by configuring CR appropriately.

22.8.6.1 Packet Error Checking (PEC)

Each SMBus transfer can optionally end with a CRC byte, called the PEC byte. Writing a one to the Packet Error Checking Enable (PECEN) bit in CR enables automatic PEC handling in the current transfer. The PEC generator is always updated on every bit transmitted or received, so that PEC handling on following linked transfers will be correct.

In slave receiver mode, the master calculates a PEC value and transmits it to the slave after all data bytes have been transmitted. Upon reception of this PEC byte, the slave will compare it to the PEC value it has computed itself. If the values match, the data was received correctly, and the slave will return an ACK to the master. If the PEC values differ, data was corrupted, and the slave will return a NAK value. The SR.SMBPECERR bit is set automatically if a PEC error occurred.

In slave transmitter mode, the slave calculates a PEC value and transmits it to the master after all data bytes have been transmitted. Upon reception of this PEC byte, the master will compare it to the PEC value it has computed itself. If the values match, the data was received correctly. If the PEC values differ, data was corrupted, and the master must take appropriate action.

The PEC byte is automatically inserted in a slave transmitter transmission if PEC enabled when NBYTES reaches zero. The PEC byte is identified in a slave receiver transmission if PEC enabled when NBYTES reaches zero. NBYTES must therefore be set to the total number of data bytes in the transmission, including the PEC byte.

22.8.6.2 Timeouts

The Timing Register (TR) configures the SMBus timeout values. If a timeout occurs, the slave will leave the bus. The SR.SMBTOUT bit is also set.

22.8.6.3 SMBALERT

A slave can get the master's attention by pulling the SMBALERT line low. This is done by writing a one to the SMBus Alert (SMBALERT) bit in CR. This will also enable address match on the Alert Response Address (ARA).

22.9.9 Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
BTF	REP	STO	SMBDAM	SMBHHM	SMBALERTM	GCM	SAM

15	14	13	12	11	10	9	8
-	BUSERR	SMBPECERR	SMBTOUT	-	-	-	NAK

7	6	5	4	3	2	1	0
ORUN	URUN	-	-	TCOMP	-	TXRDY	RXRDY

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

23.5.1 I/O Lines

The pins used for interfacing the PWMA may be multiplexed with I/O Controller lines. The programmer must first program the I/O Controller to assign the desired PWMA pins to their peripheral function.

It is only required to enable the PWMA outputs actually in use.

23.5.2 Power Management

If the CPU enters a sleep mode that disables clocks used by the PWMA, the PWMA will stop functioning and resume operation after the system wakes up from sleep mode.

23.5.3 Clocks

The clock for the PWMA bus interface (CLK_PWMA) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the PWMA before disabling the clock, to avoid freezing the PWMA in an undefined state.

Additionally, the PWMA depends on a dedicated Generic Clock (GCLK). The GCLK can be set to a wide range of frequencies and clock sources and must be enabled in the System Control Interface (SCIF) before the PWMA can be used.

23.5.4 Interrupts

The PWMA interrupt request lines are connected to the interrupt controller. Using the PWMA interrupts requires the interrupt controller to be programmed first.

23.5.5 Peripheral Events

The PWMA peripheral events are connected via the Peripheral Event System. Refer to the Peripheral Event System chapter for details.

23.5.6 Debug Operation

When an external debugger forces the CPU into debug mode, the PWMA continues normal operation. If the PWMA is configured in a way that requires it to be periodically serviced by the CPU through interrupts, improper operation or data loss may result during debugging.

23.6 Functional Description

The PWMA embeds a number of PWM channel submodules, each providing an output PWM waveform. Each PWM channel contains a duty cycle register and a comparator. A common timebase counter for all channels determines the frequency and the period for all the PWM waveforms.

23.6.1 Enabling the PWMA

Once the GCLK has been enabled, the PWMA is enabled by writing a one to the EN bit in the Control Register (CR).

23.6.2 Timebase Counter

The top value of the timebase counter defines the period of the PWMA output waveform. The timebase counter starts at zero when the PWMA is enabled and counts upwards until it reaches its effective top value (ETV). The effective top value is defined by specifying the desired number of GCLK clock cycles in the TOP field of CR (CR.TOP) in normal operation (CR.SPREAD is

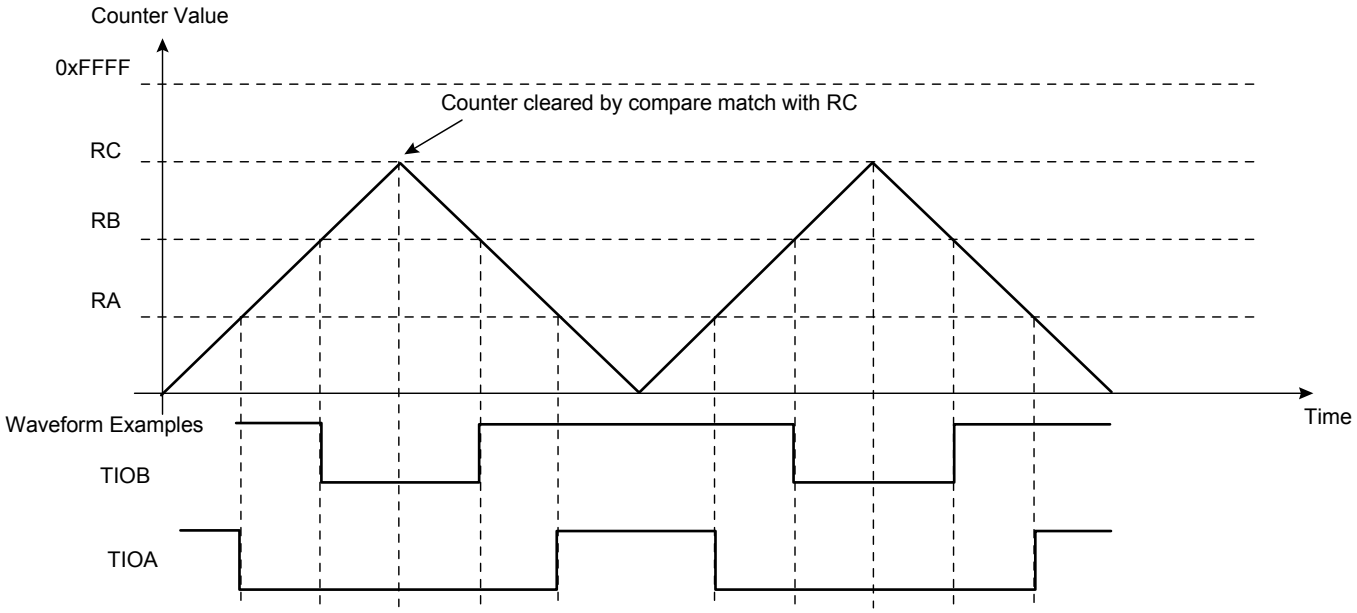
24.6.3.5 WAVSEL = 3

When CMRn.WAVSEL is three, the value of CVn is incremented from zero to RC. Once RC is reached, the value of CVn is decremented to zero, then re-incremented to RC and so on. See Figure 24-12 on page 555.

A trigger such as an external event or a software trigger can modify CVn at any time. If a trigger occurs while CVn is incrementing, CVn then decrements. If a trigger is received while CVn is decrementing, CVn then increments. See Figure 24-13 on page 556.

RC Compare can stop the counter clock (CMRn.CPCSTOP = 1) and/or disable the counter clock (CMRn.CPCDIS = 1).

Figure 24-12. WAVSEL = 3 Without Trigger



26.9.16 Channel Disable Register

Name: CHDR

Access Type: Write-only

Offset: 0x44

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
23	22	21	20	19	18	17	16
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
15	14	13	12	11	10	9	8
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- **CHn: Channel N Disable**

  Writing a zero to a bit in this register has no effect.

  Writing a one to a bit in this register disables the corresponding channel.

  Warning: If the corresponding channel is disabled during a conversion, or if it is disabled and then re-enabled during a conversion, its associated data and its corresponding DRDY and OVRE bits in SR are unpredictable.

  The number of available channels is device dependent. Please refer to the Module Configuration section at the end of this chapter for information regarding how many channels are implemented.

Starting in Run-Test/Idle, OCD registers are accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Shift-DR: Scan in the direction bit (1=read, 0=write) and the 7-bit address for the OCD register.
7. Go to Update-DR and re-enter Select-DR Scan.
8. In Shift-DR: For a read operation, scan out the contents of the addressed register. For a write operation, scan in the new contents of the register.
9. Return to Run-Test/Idle.

For any operation, the full 7 bits of the address must be provided. For write operations, 32 data bits must be provided, or the result will be undefined. For read operations, shifting may be terminated once the required number of bits have been acquired.

Table 31-18. NEXUS_ACCESS Details

Instructions	Details
IR input value	**10000** (0x10)
IR output value	peb01
DR Size	34 bits
DR input value (Address phase)	**aaaaaaar** xxxxxxxx xxxxxxxx xxxxxxxx xx
DR input value (Data read phase)	**xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx** xx
DR input value (Data write phase)	**dddddddd dddddddd dddddddd dddddddd** xx
DR output value (Address phase)	xx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb
DR output value (Data read phase)	eb **dddddddd dddddddd dddddddd dddddddd**
DR output value (Data write phase)	xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

31.5.3.2 MEMORY_SERVICE

This instruction allows access to registers in an optional Memory Service Unit. The 7-bit register index, a read/write control bit, and the 32-bit data is accessed through the JTAG port.

The data register is alternately interpreted by the SAB as an address register and a data register. The SAB starts in address mode after the MEMORY_SERVICE instruction is selected, and toggles between address and data mode each time a data scan completes with the busy bit cleared.

Starting in Run-Test/Idle, Memory Service registers are accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Shift-DR: Scan in the direction bit (1=read, 0=write) and the 7-bit address for the Memory Service register.

The VERSION register reads 0x100 instead of 0x101.
Fix/Workaround
None.

35.4.18 ACIFB

1. **Generic clock sources in sleep modes.**
The ACIFB should not use RC32K or CLK_1K as generic clock source if the chip uses sleep modes.
Fix/Workaround
None.

2. **Negative offset**
The static offset of the analog comparator is approximately -50mV
Fix/Workaround
None.

3. **CONFW.WEVSRC and CONFW.WEVEN are not correctly described in the user interface**
CONFW.WEVSRC is only two bits instead of three bits wide. Only values 0, 1, and 2 can be written to this register. CONFW.WEVEN is in bit position 10 instead of 11.
Fix/Workaround
Only write values 0, 1, and 2 to CONFW.WEVSRC. When reading CONFW.WEVSRC, disregard the third bit. Read/write bit 10 to access CONFW.WEVEN.

4. **VERSION register reads 0x200**
The VERSION register reads 0x200 instead of 0x212.
Fix/Workaround
None.

35.4.19 CAT

1. **Switch off discharge current when reaching 0V**
The discharge current will switch off when reaching MGCFG1.MAX, not when reaching 0V.
Fix/Workaround
None.

2. **CAT external capacitors are not clamped to ground when CAT is idle**
The CAT module does not clamp the external capacitors to ground when it is idle. The capacitors are left floating, so they could accumulate small amounts of charge.
Fix/Workaround
None.

3. **DISHIFT field is stuck at zero**
The DISHIFT field in the MGCFG1, TGACFG1, TGBCFG1, and ATCFG1 registers is stuck at zero and cannot be written to a different value. Capacitor discharge time will only be determined by the DILEN field.
Fix/Workaround
None.

4. **MGCFG2.CONSEN field is stuck at zero**
The CONSEN field in the MGCFG2 register is stuck at zero and cannot be written to a different value. The CAT consensus filter does not function properly, so termination of QMatrix data acquisition is controlled only by the MAX field in MGCFG1.

11. PM: Entering Shutdown mode description updated.
12. SCIF: DFLL output frequency is 40-150MHz, not 20-150MHz or 30-150MHz.
13. SCIF: Temperature sensor is connected to ADC channel 9, not 7.
14. SCIF: Updated the oscillator connection figure for OSC0
15. GPIO: Removed unimplemented features (pull-down, buskeeper, drive strength, slew rate, Schmidt trigger, open drain).
16. SPI: RDR.PCS field removed (RDR[19:16]).
17. TWIS: Figures updated.
18. ADCIFB: The sample and hold time and the startup time formulas have been corrected (ADC Configuration Register).
19. ADCIFB: Updated ADC signal names.
20. ACIFB: CONFW.WEVSRC is bit 8-10, CONFW.EWEVEN is bit 11. CONF.EVENP and CONF.EVENN bits are swapped.
21. CAT: Matrix size is 16 by 8, not 18 by 8.
22. Electrical Characteristics: General update.
23. Mechanical Characteristics: Added numbers for package drawings.
24. Mechanical Characteristics: In the TQFP-48 package drawing the Lead Coplanarity is 0.102mm, not 0.080mm.
25. Ordering Information: Ordering code for TLLGA-48 package updated.

36.9 Rev. A – 06/2009

1. Initial revision.