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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 58x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60fn1m0vlq15

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{IH}	Input high voltage (digital pins) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage (digital pins) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis (digital pins)	$0.06 \times V_{DD}$	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ 	-5	—	mA	1
I_{ICAIO}	Analog ² , EXTAL0/XTAL0, and EXTAL1/XTAL1 pin DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection) 	-5	—	mA	3
		—	+5		
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection Positive current injection 	-25	—	mA	
		—	+25		
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{DIO_MIN} ($=V_{SS}-0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{IC}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} ($=V_{SS}-0.3\text{V}$) and V_{IN} is less than V_{AIO_MAX} ($=V_{DD}+0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• VLLS3 → RUN	—	114	μs	
	• LLS → RUN	—	5.0	μs	
	• VLPS → RUN	—	5	μs	
	• STOP → RUN	—	4.8	μs	

1. Normal boot (FTFE_FOFT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	59.6	180	mA	
	• @ 3.0V	—	59.6	185	mA	
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3
	• @ 1.8V	—	89.9	205	mA	
	• @ 3.0V	—	89.9	210	mA	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	40.9	95	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	19.6	65	mA	4
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	1.3	3.8	mA	
	• @ 70°C	—	3.0	27	mA	
	• @ 105°C	—	7.5	42	mA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.4	32	mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	2.2	38	mA	6
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	0.926	22	mA	7

Table continues on the next page...

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode is greater than 100 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

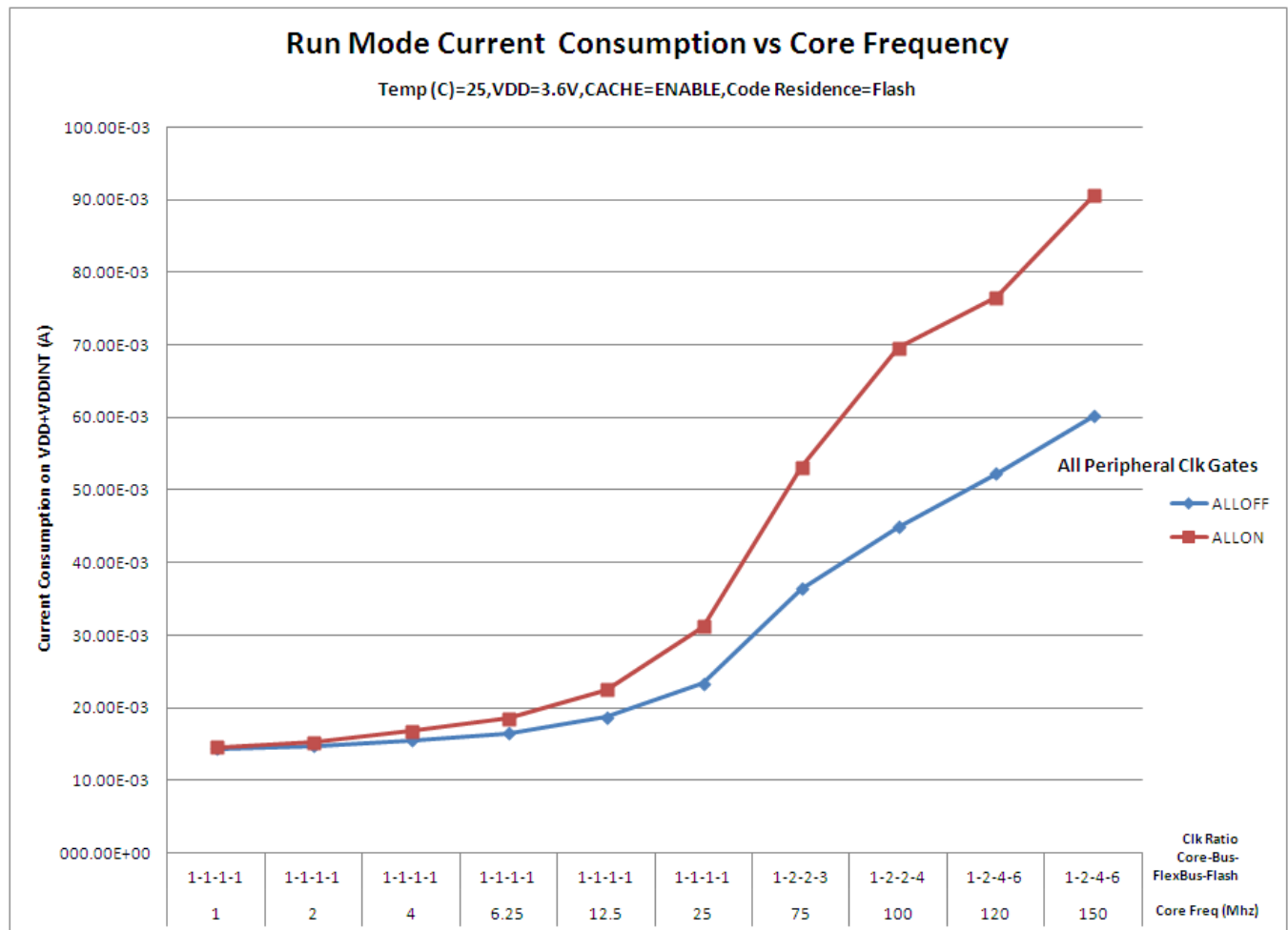


Figure 2. Run mode supply current vs. core frequency

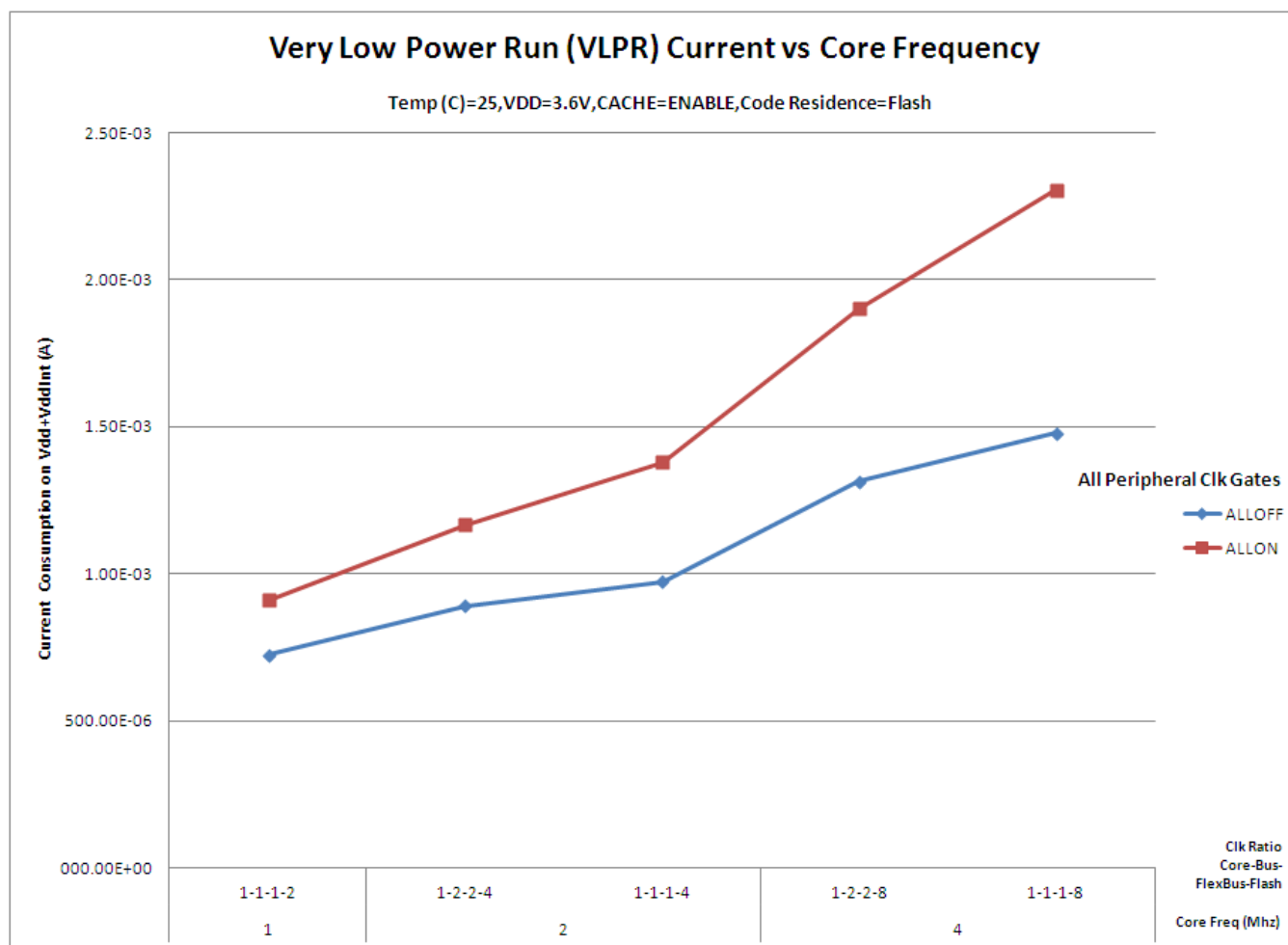


Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 256MAPBGA

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	21	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	24	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	29	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	28	dBμV	

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 72 MHz, f_{BUS} = 72MHz

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
t_{i050}	Port rise and fall time (high drive strength)				6
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	7	ns	—
	• $2.7 \leq V_{DD} \leq 3.6V$	—	3	ns	—
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	28	ns	—
t_{i050}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	18	ns	—
	• $2.7 \leq V_{DD} \leq 3.6V$	—	9	ns	—
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	48	ns	—
t_{i060}	Port rise and fall time (high drive strength)				6
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	6	ns	—
	• $2.7 \leq V_{DD} \leq 3.6V$	—	3	ns	—
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	28	ns	—
t_{i060}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	18	ns	—
	• $2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	—
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	48	ns	—

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load
6. 25pF load
7. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	50	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	30	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	30	27	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	17	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	10	°C/W	3

Table continues on the next page...

Peripheral operating requirements and behaviors

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

5.5 Power sequencing

Voltage supplies must be sequenced in the proper order to avoid damaging internal diodes. There is no limit on how long after one supply powers up before the next supply must power up. Note that V_{DD} and V_{DD_INT} can use the same power source.

The power-up sequence is:

1. V_{DD}
2. V_{DD_INT}
3. V_{DDA}
4. V_{DD_DDR}

The power-down sequence is the reverse:

1. V_{DD_DDR}
2. V_{DDA}
3. V_{DD_INT}
4. V_{DD}

6 Peripheral operating requirements and behaviors

6.1 Core modules

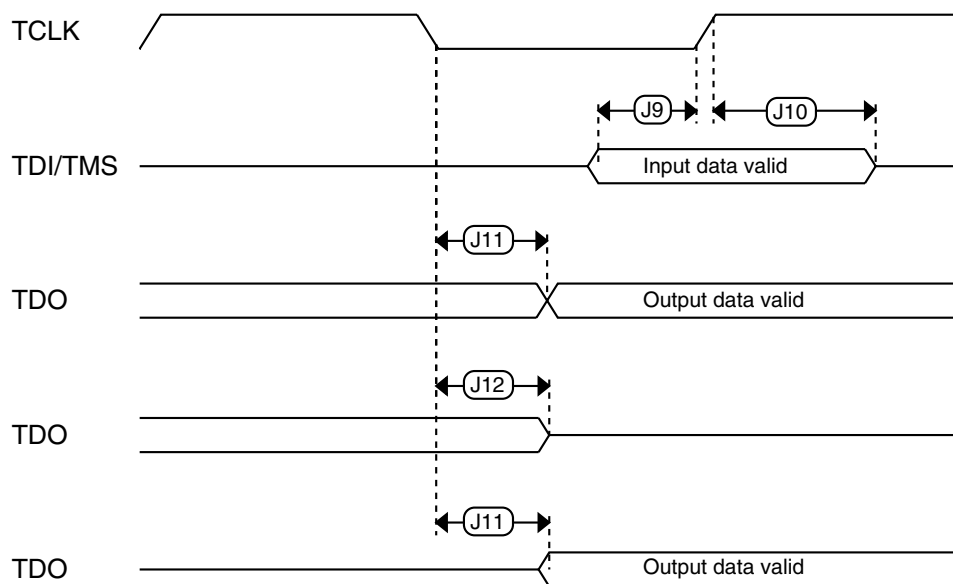
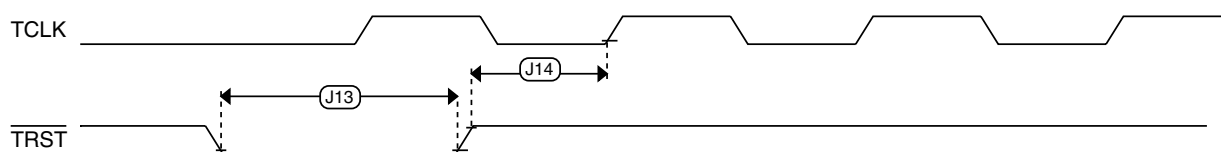


Figure 8. Test Access Port timing

Figure 9. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter <ul style="list-style-type: none"> $f_{VCO} = 48 \text{ MHz}$ $f_{VCO} = 98 \text{ MHz}$ 	—	180	—	ps	
$t_{fll_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL0,1						
f_{pll_ref}	PLL reference frequency range	8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency	180	—	360	MHz	
f_{vcoclk}	PLL output frequency	90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency	90	—	180	MHz	
I_{pll}	PLL0 operating current <ul style="list-style-type: none"> VCO @ 180 MHz ($f_{osc_hi_1} = 32 \text{ MHz}$, $f_{pll_ref} = 8 \text{ MHz}$, VDIV multiplier = 22) 	—	2.8	—	mA	7
I_{pll}	PLL0 operating current <ul style="list-style-type: none"> VCO @ 360 MHz ($f_{osc_hi_1} = 32 \text{ MHz}$, $f_{pll_ref} = 8 \text{ MHz}$, VDIV multiplier = 45) 	—	4.7	—	mA	7
I_{pll}	PLL1 operating current <ul style="list-style-type: none"> VCO @ 180 MHz ($f_{osc_hi_1} = 32 \text{ MHz}$, $f_{pll_ref} = 8 \text{ MHz}$, VDIV multiplier = 22) 	—	2.3	—	mA	7
I_{pll}	PLL1 operating current <ul style="list-style-type: none"> VCO @ 360 MHz ($f_{osc_hi_1} = 32 \text{ MHz}$, $f_{pll_ref} = 8 \text{ MHz}$, VDIV multiplier = 45) 	—	3.6	—	mA	7
t_{pll_lock}	Lock detector detection time	—	—	$100 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	8
J_{cyc_pll}	PLL period jitter (RMS) <ul style="list-style-type: none"> $f_{vco} = 180 \text{ MHz}$ $f_{vco} = 360 \text{ MHz}$ 	—	100	—	ps	9
J_{acc_pll}	PLL accumulated jitter over 1 μ s (RMS) <ul style="list-style-type: none"> $f_{vco} = 180 \text{ MHz}$ $f_{vco} = 360 \text{ MHz}$ 	—	600	—	ps	10
		—	300	—	ps	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	1
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—	—	60	MHz	2, 3
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

6.3.3.2 32kHz oscillator frequency specifications

Table 19. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvp8}	Program Phrase high-voltage time	—	7.5	18	μ s	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Flash Block high-voltage time for 128 KB	—	104	1808	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	Read 1s Block execution time • 128 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.0	ms	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	μs	1
t_{pgmchk}	Program Check execution time	—	—	80	μs	1
t_{rdsrc}	Read Resource execution time	—	—	40	μs	1
t_{pgm8}	Program Phrase execution time	—	70	150	μs	
$t_{ersblk128k}$	Erase Flash Block execution time					2
	• 128 KB data flash	—	110	925	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmse4k}$	Program Section execution time (4KB flash)	—	20	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.0	ms	
t_{rdonce}	Read Once execution time	—	—	30	μs	1
$t_{pgmonce}$	Program Once execution time	—	70	—	μs	
t_{ersall}	Erase All Blocks execution time	—	650	5600	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{swapx01}$	Swap Control execution time					
	• control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	
$t_{pgmpart64k}$	Program Partition for EEPROM execution time					
	• 64 KB FlexNVM	—	235	—	ms	
$t_{pgmpart256k}$	• 256 KB FlexNVM	—	240	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time:					
	• Control Code 0xFF	—	205	—	μs	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.6	2.5	ms	
$t_{setram128k}$	• 128 KB EEPROM backup	—	2.7	3.8	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	4.8	6.2	ms	
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	140	225	μs	3
$t_{eewr8b64k}$	Byte-write to FlexRAM execution time:					
	• 64 KB EEPROM backup	—	400	1700	μs	
$t_{eewr8b128k}$	• 128 KB EEPROM backup	—	450	1800	μs	
$t_{eewr8b256k}$	• 256 KB EEPROM backup	—	525	2000	μs	
$t_{eewr16bers}$	16-bit write to erased FlexRAM location execution time	—	140	225	μs	

Table continues on the next page...

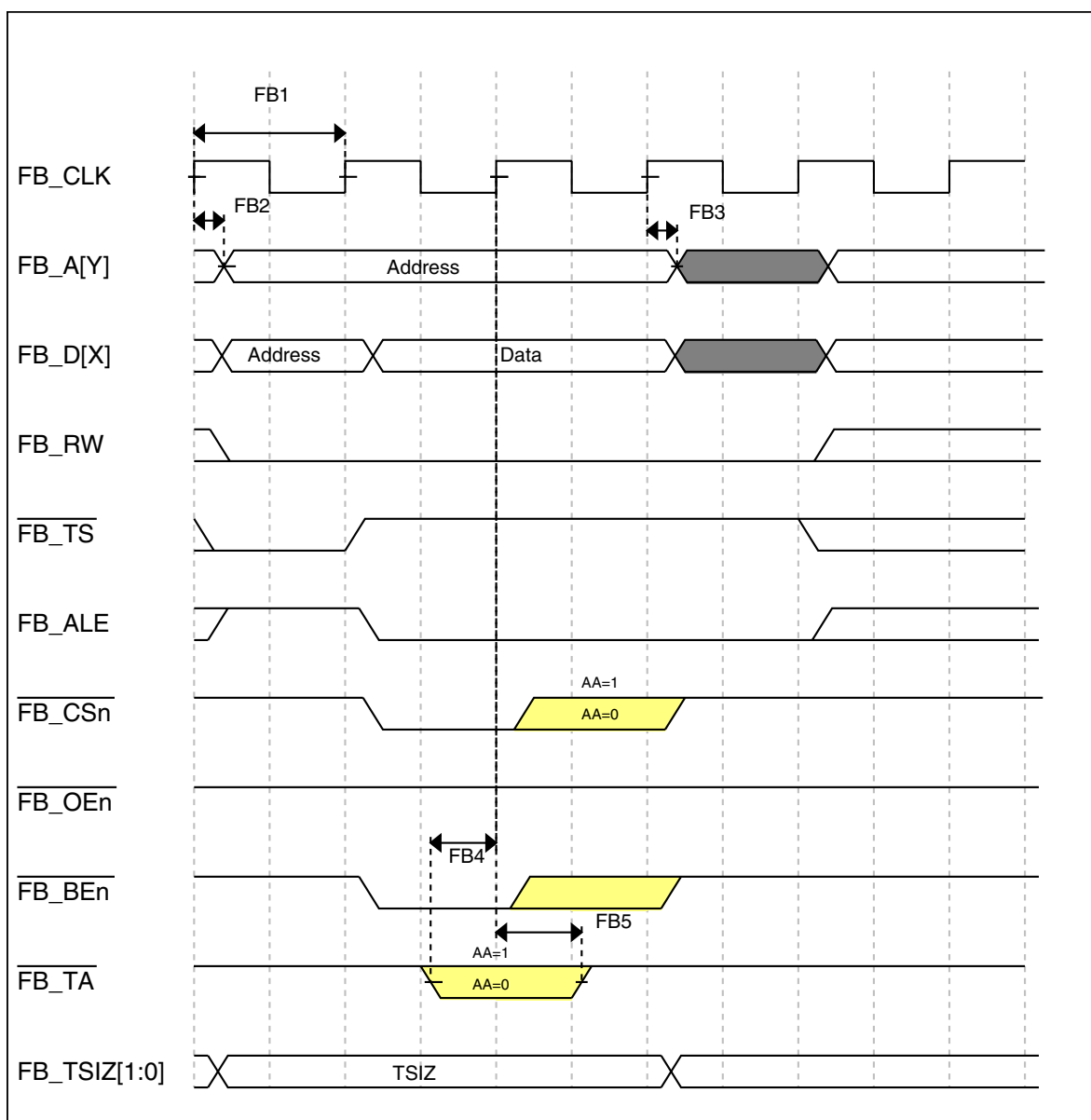


Figure 18. FlexBus write timing diagram

6.5 Security and integrity modules

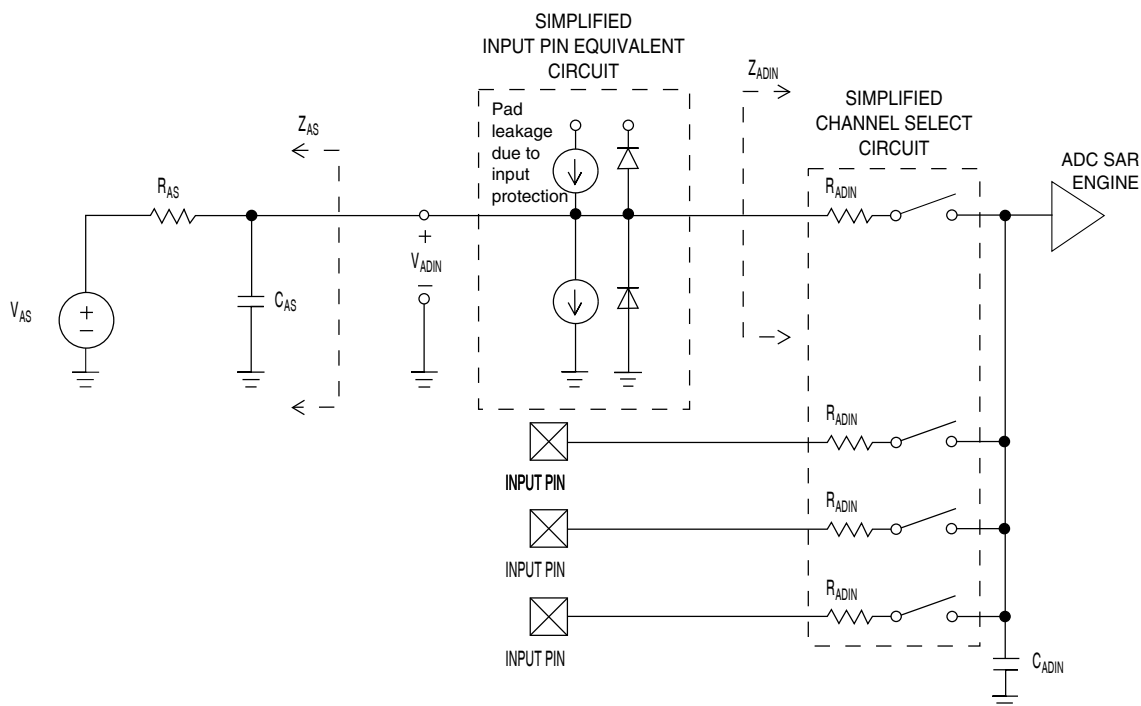
There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

Table 28. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has $< 8\text{ }\Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#)

**Figure 19. ADC input impedance equivalency diagram**

6.6.1.2 16-bit ADC electrical characteristics

Table 29. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

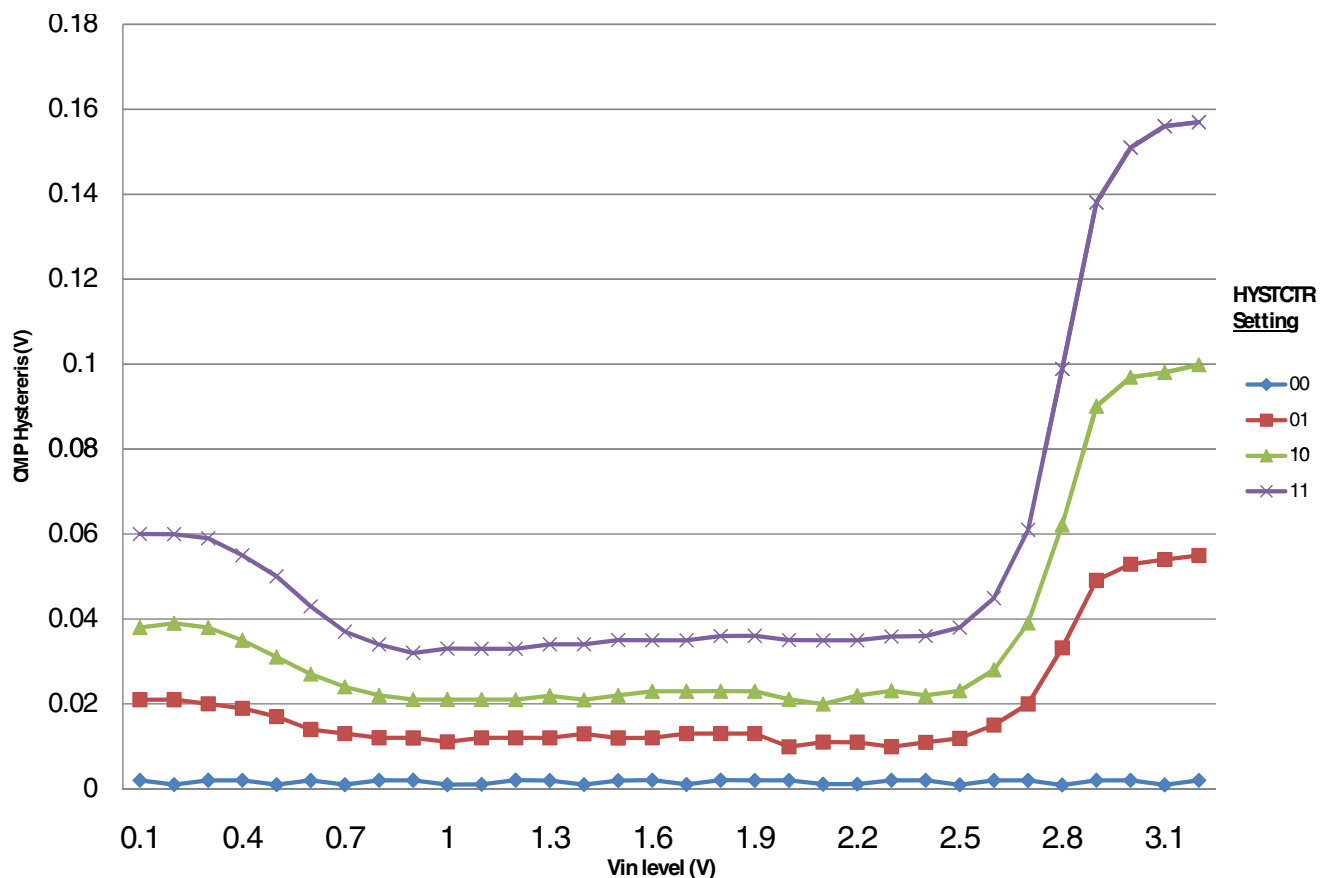


Figure 23. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

Table 36. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	μA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation <ul style="list-style-type: none"> current = + 1.0 mA current = - 1.0 mA 	— —	2 5	— —	mV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdrift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 37. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}C$	

Table 38. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See [General switching specifications](#).

6.8 Communication interfaces

6.8.12 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.12.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 50. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

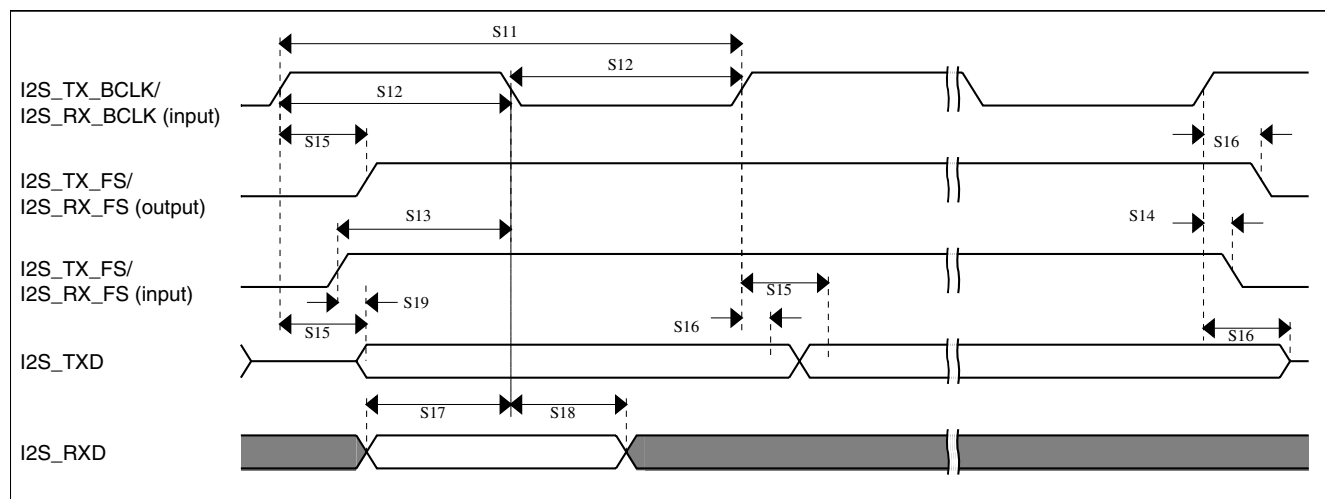


Figure 35. I2S/SAI timing — slave modes

6.8.12.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 52. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

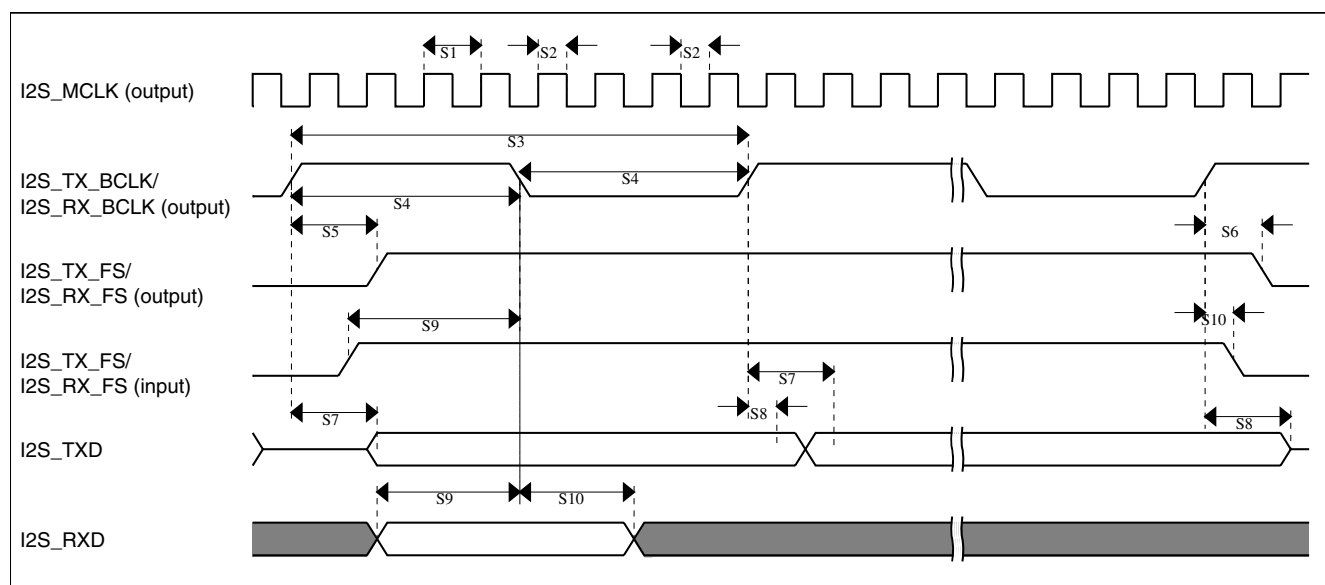


Figure 36. I2S/SAI timing — master modes

Table 53. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid <ul style="list-style-type: none"> Multiple SAI Synchronous mode All other modes 	—	24 20.6	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear