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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 150MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 100 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 48x16b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/pk60fn1m0vlq15 |

| Field | Description | Values |
|---|---|---|
| T | Temperature range (°C) | • V = –40 to 105<br>• C = –40 to 85 |
| PP | Package identifier | • LQ = 144 LQFP (20 mm x 20 mm)<br>• MD = 144 MAPBGA (13 mm x 13 mm) |
| CC | Maximum CPU frequency (MHz) | • 15 = 150 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 2.4 Example

This is an example part number:

MK60FN1M0VLQ15

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

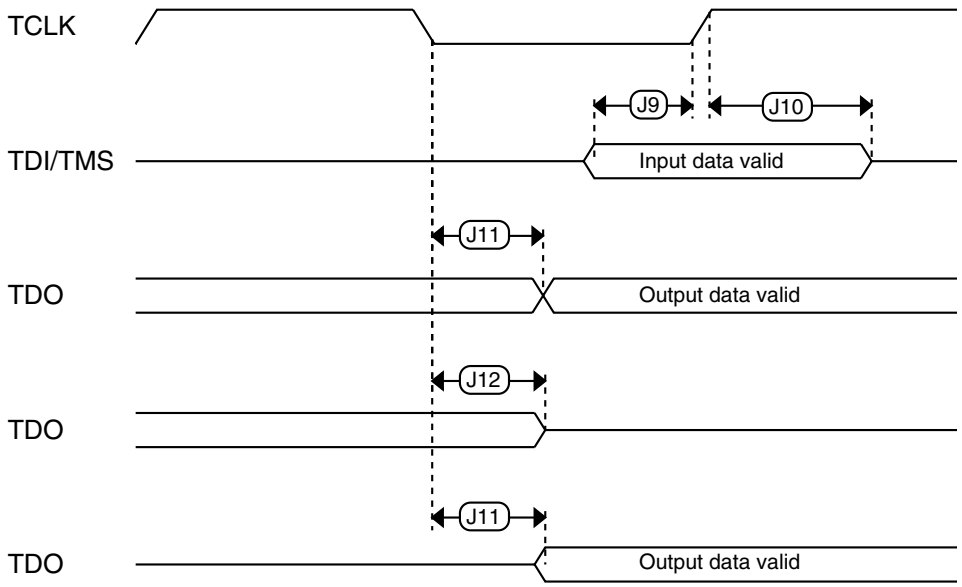


**Figure 8. Test Access Port timing**

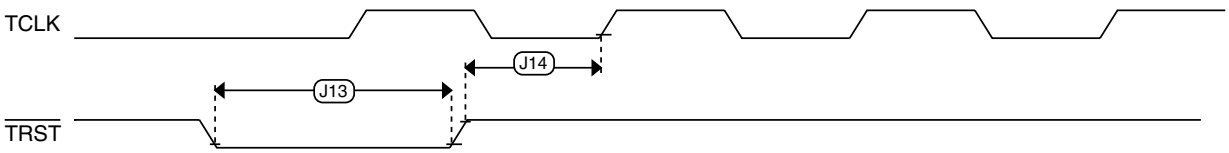


**Figure 9. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

**Table 17. Oscillator frequency specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 1000 | — | ms | 4, 5 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 500 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Frequencies less than 8 MHz are not in the PLL range.
2. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
3. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode bu default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 18. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

#### 6.3.3.2 32kHz oscillator frequency specifications

**Table 19. 32kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $v_{ec_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 20. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm8}$ | Program Phrase high-voltage time | — | 7.5 | 18 | μs | |
| $t_{hversscr}$ | Erase Flash Sector high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk128k}$ | Erase Flash Block high-voltage time for 128 KB | — | 104 | 1808 | ms | 1 |
| $t_{hversblk256k}$ | Erase Flash Block high-voltage time for 256 KB | — | 208 | 3616 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash timing specifications — commands

**Table 21. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk128k}$ | • 128 KB data flash | — | — | 0.5 | ms | |
| $t_{rd1blk256k}$ | • 256 KB program flash | — | — | 1.0 | ms | |

*Table continues on the next page...*

## Table 25. NFC specifications (continued)

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{ALH}$ | NFC_ALE hold time | $T_H + T_L$ | — | ns |
| $t_{DS}$ | Data setup time | $T_L – 1$ | — | ns |
| $t_{DH}$ | Data hold time | $T_H – 1$ | — | ns |
| $t_{WC}$ | Write cycle time | $T_H + T_L – 1$ | — | ns |
| $t_{WH}$ | $\overline{\text{NFC_WE}}$ hold time | $T_H – 1$ | — | ns |
| $t_{RR}$ | Ready to $\overline{\text{NFC_RE}}$ low | $4T_H + 3T_L + 90$ | — | ns |
| $t_{RP}$ | $\overline{\text{NFC_RE}}$ pulse width | $T_L + 1$ | — | ns |
| $t_{RC}$ | Read cycle time | $T_L + T_H – 1$ | — | ns |
| $t_{REH}$ | $\overline{\text{NFC_RE}}$ high hold time | $T_H – 1$ | — | ns |
| $t_{IS}$ | Data input setup time | 11 | — | ns |

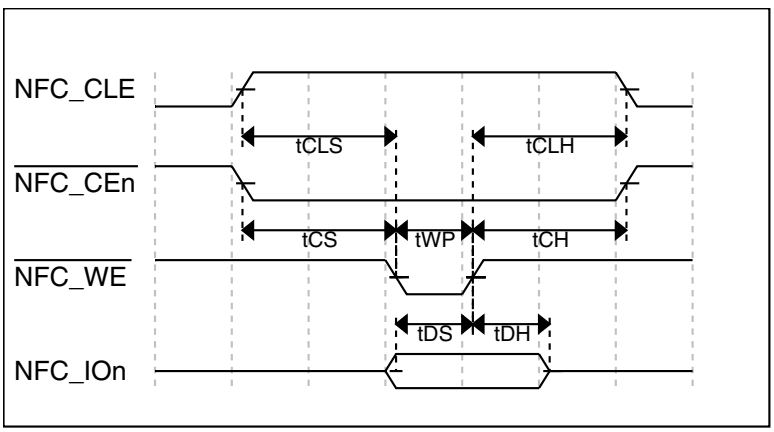


**Figure 12. Command latch cycle timing**

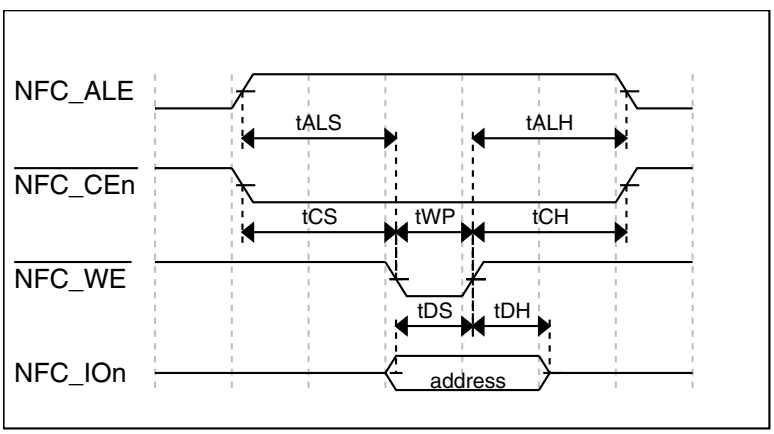


**Figure 13. Address latch cycle timing**

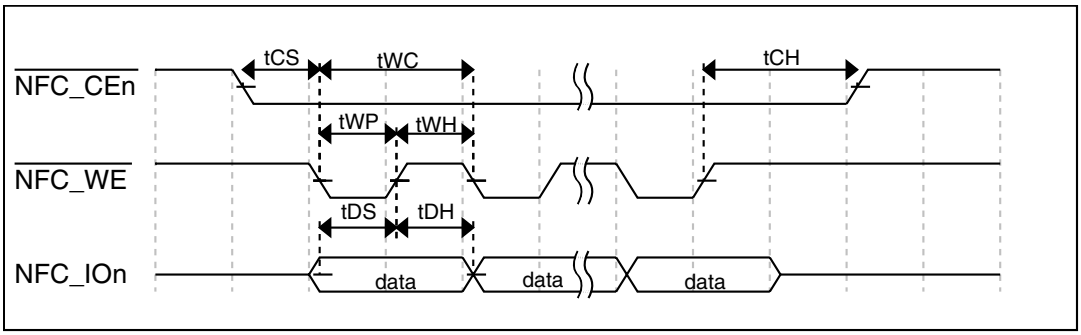


**Figure 14. Write data latch cycle timing**

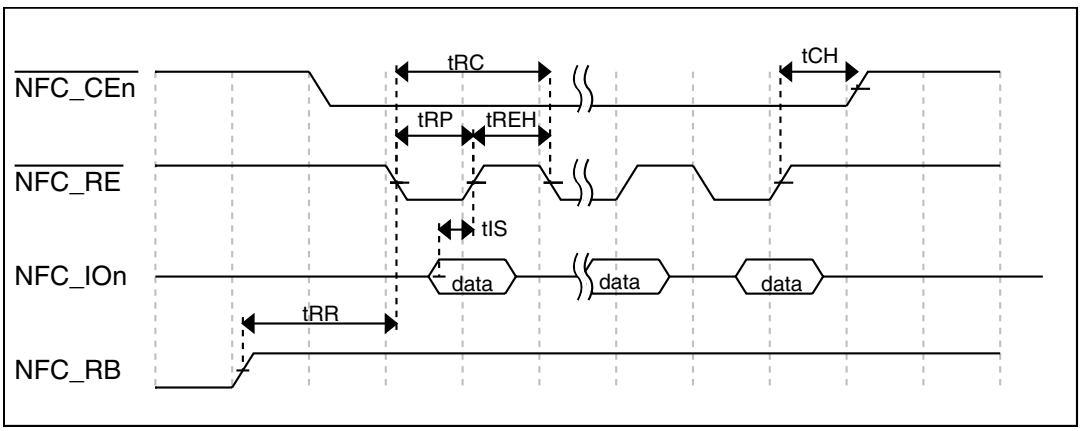


**Figure 15. Read data latch cycle timing in non-fast mode**

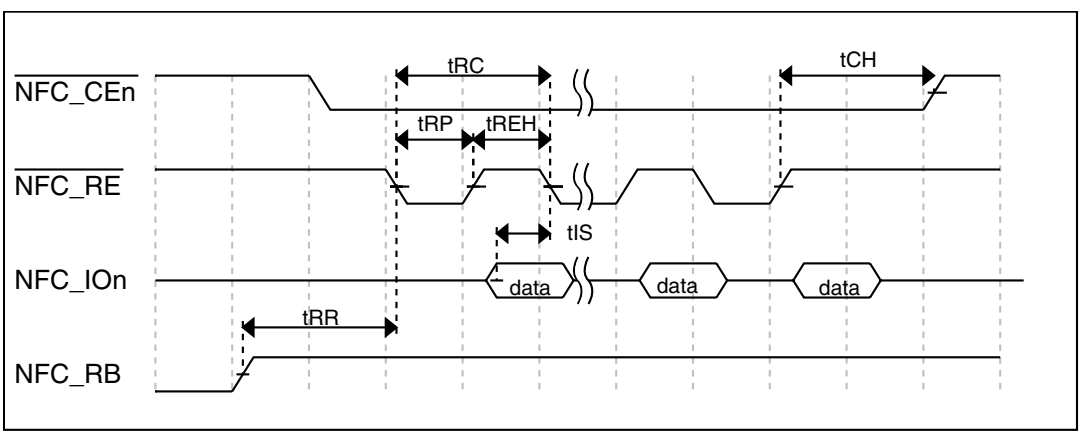


**Figure 16. Read data latch cycle timing in fast mode**

## 6.4.4 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

**Table 26. Flexbus limited voltage range switching specifications**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 20 | — | ns | |
| FB2 | Address, data, and control output valid | — | 11.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0.5 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 8.5 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

**Table 27. Flexbus full voltage range switching specifications**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 13.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 13.7 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

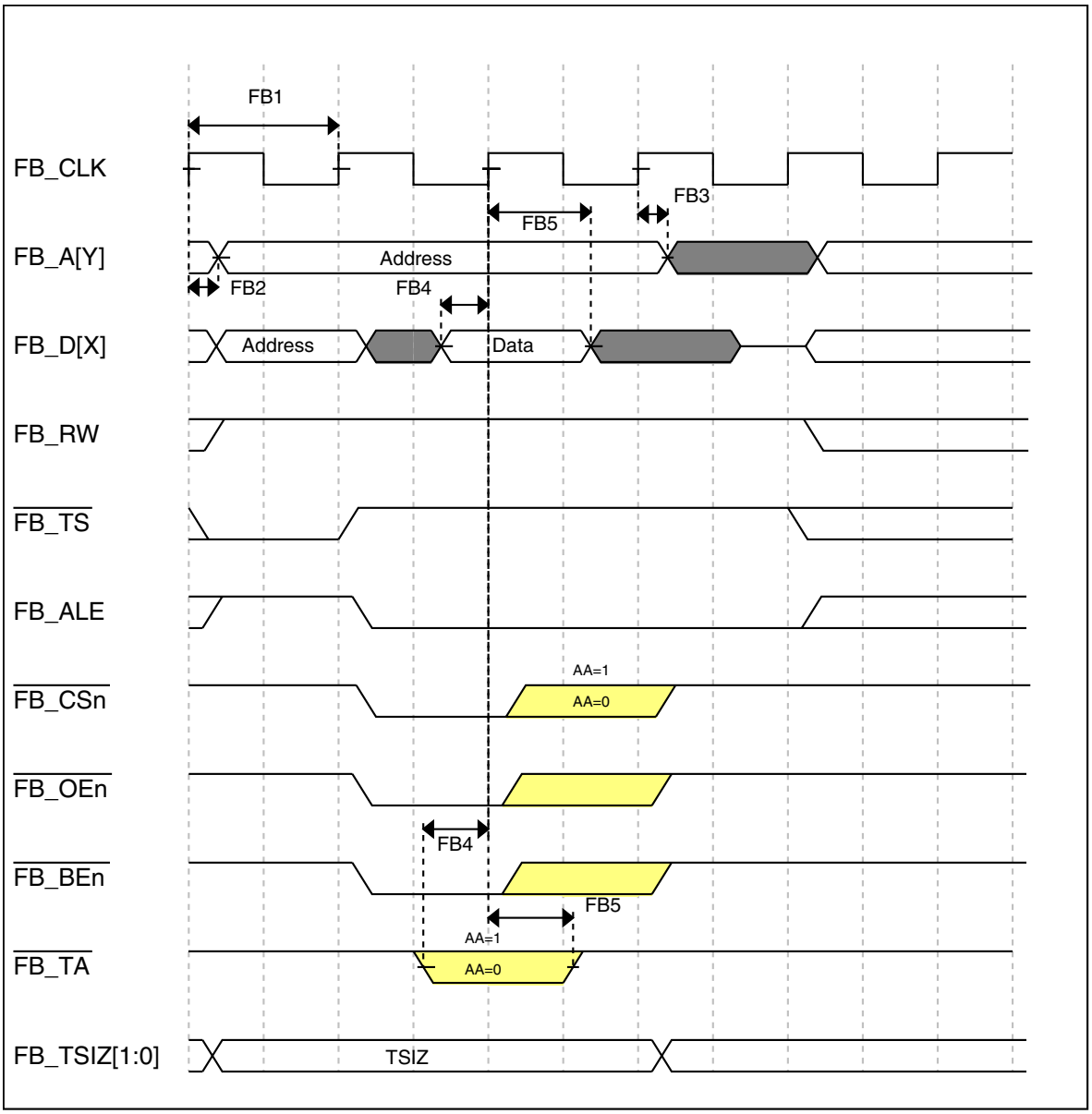


**Figure 17. FlexBus read timing diagram**

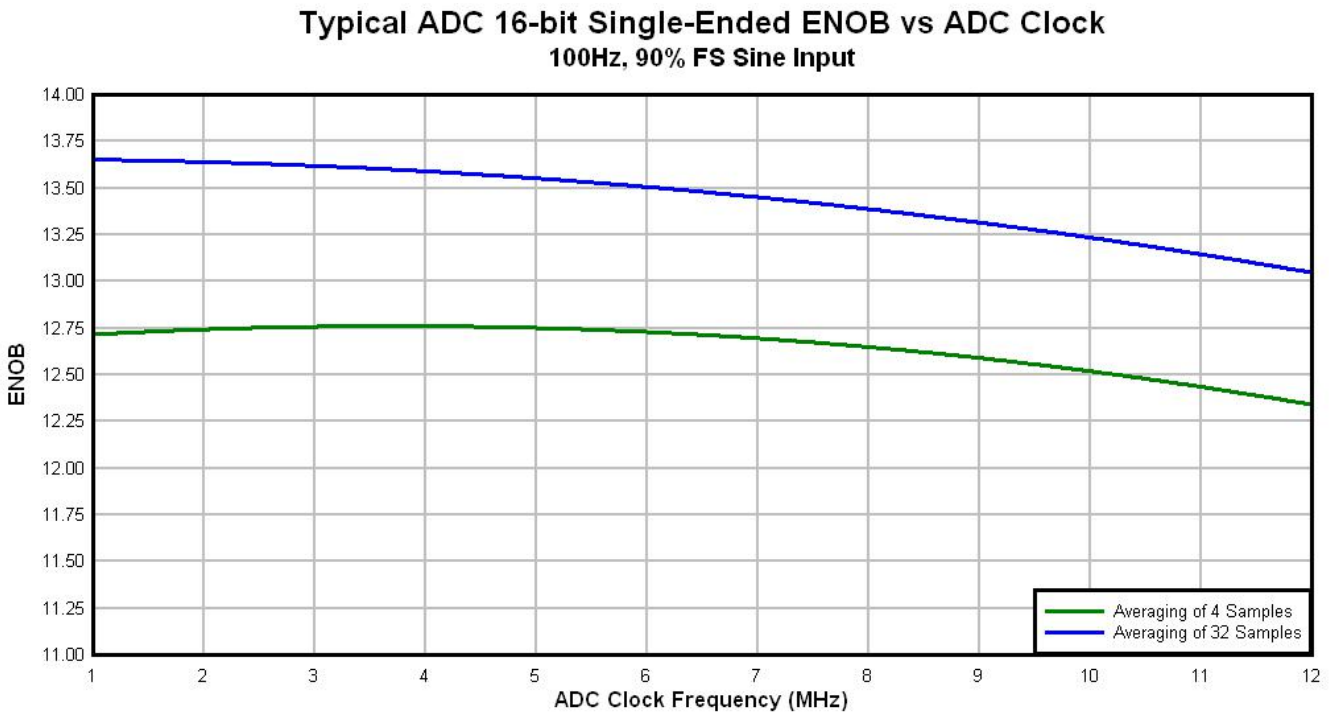


**Figure 21. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 30. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8<br>Gain = 16, 32<br>Gain = 64 | —<br>—<br>— | 128<br>64<br>32 | —<br>—<br>— | kΩ | IN+ to IN-[4] |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | μs | 6 |

*Table continues on the next page...*

## Table 32. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | μs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

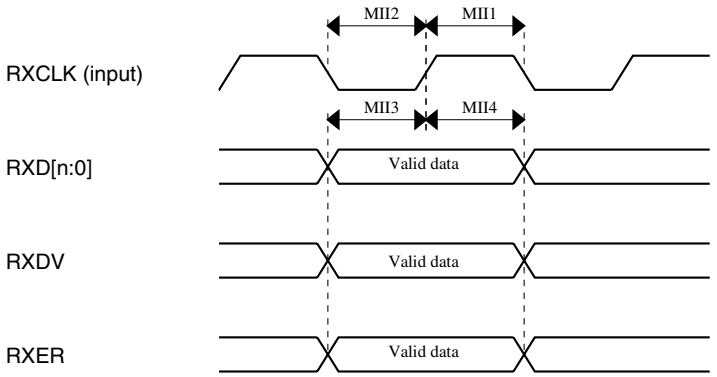


**Figure 27. MII receive signal timing diagram**

### 6.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

**Table 40. RMII signal switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

## 6.8.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

### 6.8.5 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

**Table 43. ULPI timing specifications**

| Num | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | USB_CLKIN operating frequency | — | 60 | — | MHz |
| | USB_CLKIN duty cycle | — | 50 | — | % |
| U1 | USB_CLKIN clock period | — | 16.67 | — | ns |
| U2 | Input setup (control and data) | 5 | — | — | ns |
| U3 | Input hold (control and data) | 1 | — | — | ns |
| U4 | Output valid (control and data) | — | — | 9.5 | ns |
| U5 | Output hold (control and data) | 1 | — | — | ns |

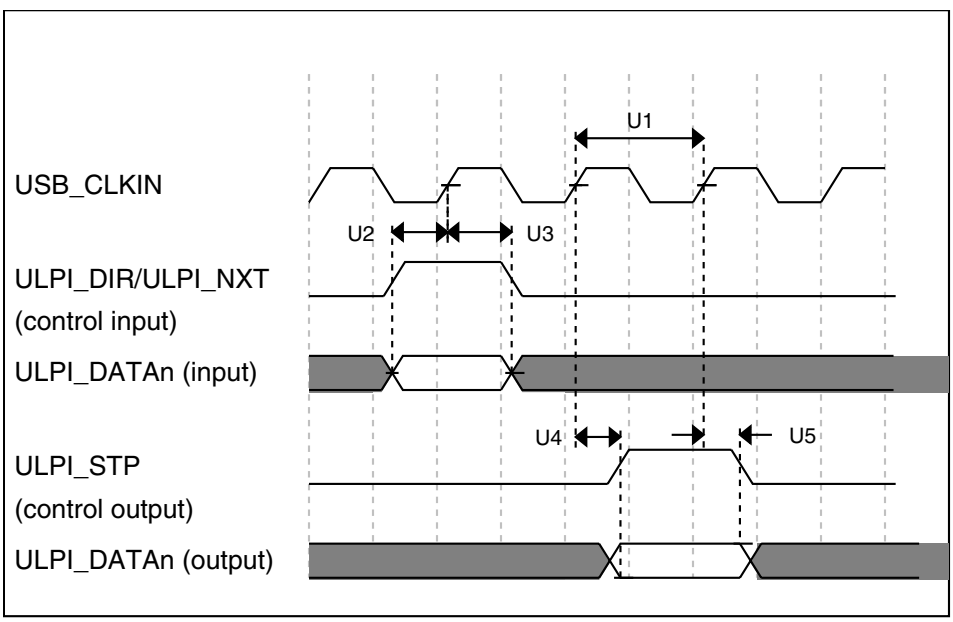


**Figure 28. ULPI timing diagram**

## Table 48. SDHC switching specifications over a limited operating voltage range (continued)

| Num | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | | **SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | |
| SD6 | $t_{OD}$ | SDHC output delay (output valid) | -5 | 6.5 | ns |
| | | **SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | |
| SD7 | $t_{ISU}$ | SDHC input setup time | 5 | — | ns |
| SD8 | $t_{IH}$ | SDHC input hold time | 0 | — | ns |

## Table 49. SDHC switching specifications over the full operating voltage range

| Num | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | | Operating voltage | 1.71 | 3.6 | V |
| | | **Card input clock** | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed) | 0 | 25 | MHz |
| | fpp | Clock frequency (MMC full speed) | 0 | 20 | MHz |
| | $f_{OD}$ | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | $t_{WL}$ | Clock low time | 7 | — | ns |
| SD3 | $t_{WH}$ | Clock high time | 7 | — | ns |
| SD4 | $t_{TLH}$ | Clock rise time | — | 3 | ns |
| SD5 | $t_{THL}$ | Clock fall time | — | 3 | ns |
| | | **SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | |
| SD6 | $t_{OD}$ | SDHC output delay (output valid) | -5 | 6.5 | ns |
| | | **SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | |
| SD7 | $t_{ISU}$ | SDHC input setup time | 5 | — | ns |
| SD8 | $t_{IH}$ | SDHC input hold time | 1.3 | — | ns |

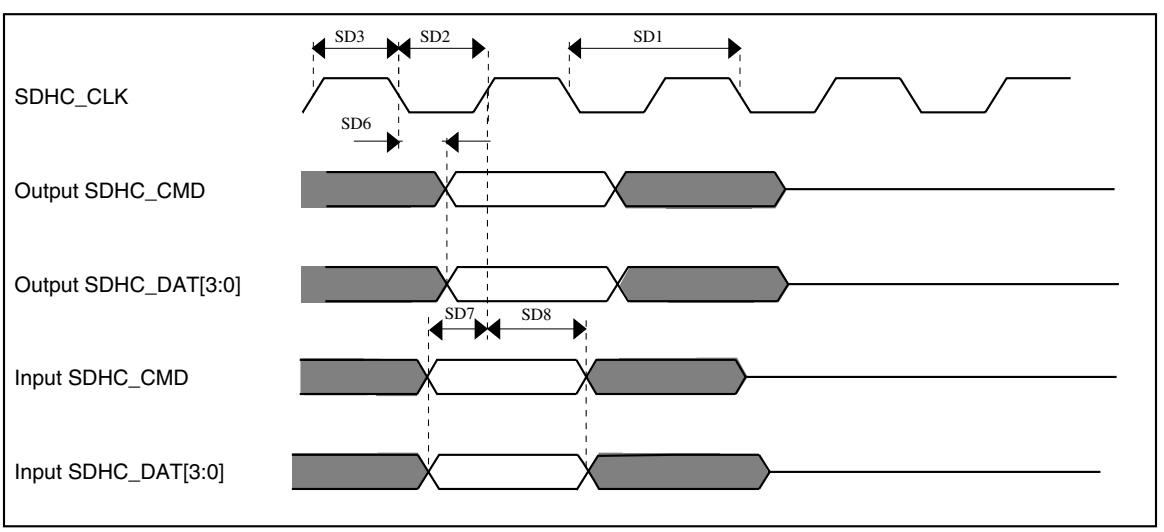


**Figure 33. SDHC timing**

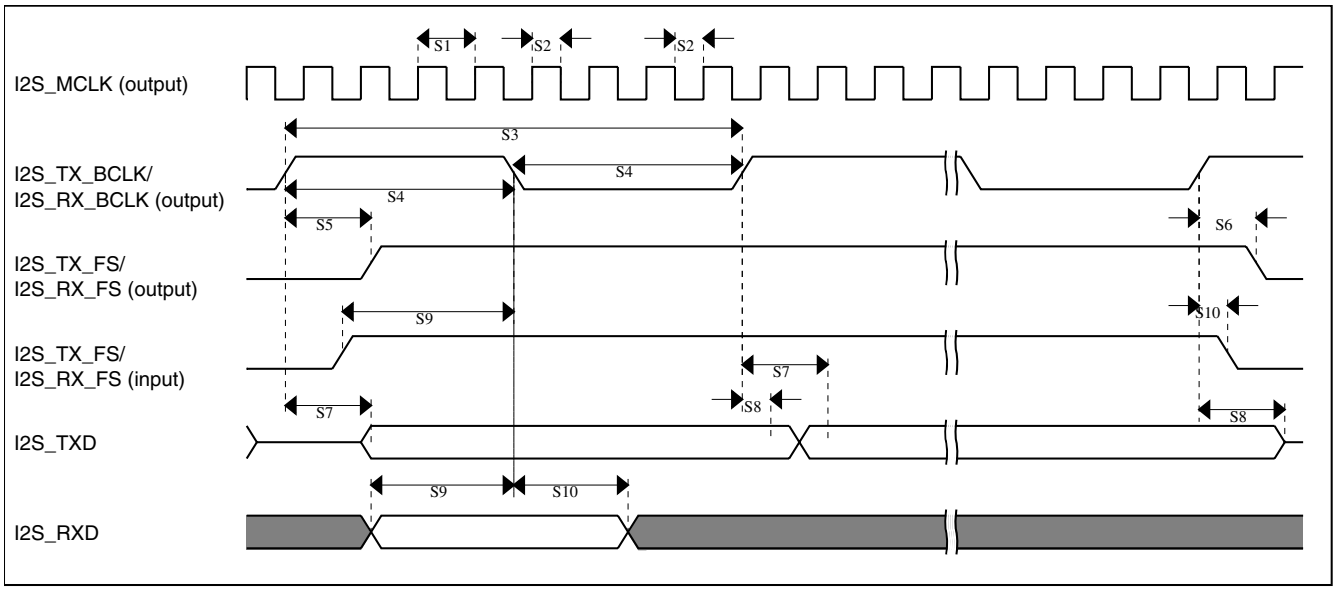


**Figure 34. I2S/SAI timing — master modes**

**Table 51. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 4.5 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid<br>• Multiple SAI Synchronous mode<br>• All other modes | <br>—<br>— | <br>21<br>15 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 4.5 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

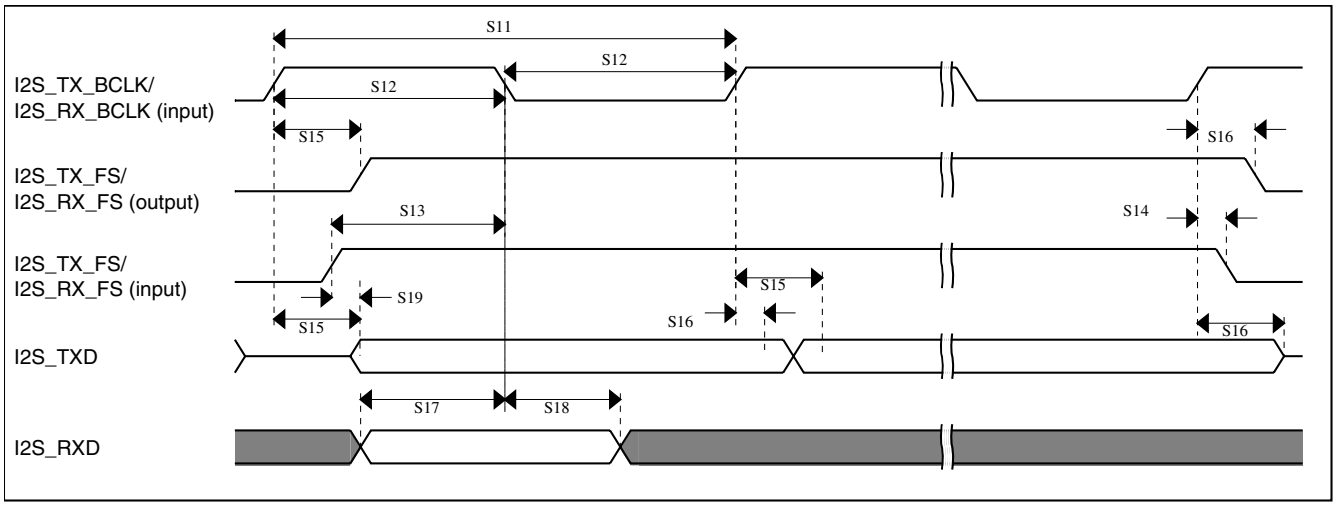


**Figure 37. I2S/SAI timing — slave modes**

### 6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 54. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | -1.6 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 45 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

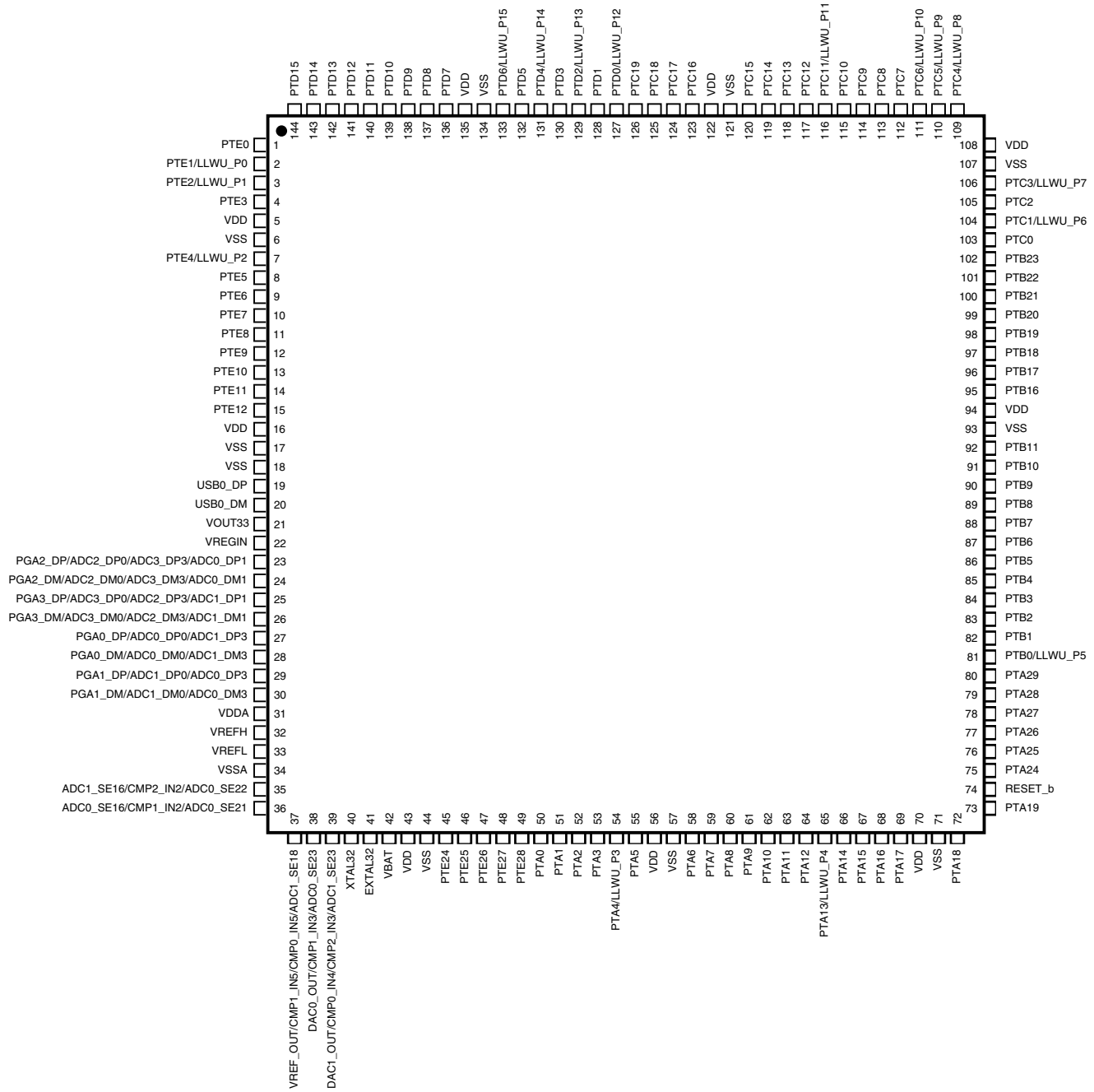


**Figure 40. K60 144 LQFP Pinout Diagram**