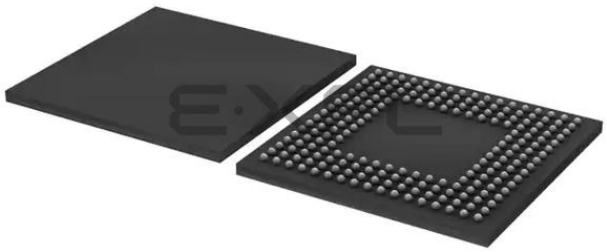

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, PCM, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	10
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3152fet208-551

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
JTAG						
JTAGSEL	U10	SUP3	DI / GPIO	I:PD	DIO1	JTAG selection. Controls which digital die TAP controller is configured in the JTAG chain along with the analog die TAP controller. Must be LOW during power-on reset.
TDI	T10	SUP3	DI / GPIO	I:PU	DIO1	JTAG data Input
TRST_N	U11	SUP3	DI / GPIO	I:PD	DIO1	JTAG TAP Controller Reset Input. Must be LOW during power-on reset.
TCK	U12	SUP3	DI / GPIO	I:PD	DIO1	JTAG clock input
TMS	U9	SUP3	DI / GPIO	I:PU	DIO1	JTAG mode select input
TDO	F14	SUP3	DO	Z	DIO2	JTAG data output
UART						
mUART_CTS_N[4][6]	P11	SUP3	DI / GPIO	I	DIO1	UART Clear-To-Send (CTS) (active LOW)
mUART_RTS_N[4][6]	R11	SUP3	DO / GPIO	O	DIO1	UART Ready-To-Send (RTS) (active LOW)
UART_RXD[4]	R10	SUP3	DI / GPIO	I	DIO1	UART serial input
UART_TXD[4]	P10	SUP3	DO / GPIO	O	DIO1	UART serial output
I²C master/slave interface						
I2C_SDA0	C10	SUP3	DIO	I	IICD	I²C-bus data line
I2C_SCL0	A9	SUP3	DIO	I	IICC	I²C-bus clock line
Serial Peripheral Interface (SPI)						
SPI_CS_OUT0[4]	D8	SUP3	DO	O	DIO4	SPI chip select output (master)
SPI_SCK[4]	C8	SUP3	DIO	I	DIO4	SPI clock input (slave) / clock output (master)
SPI_MISO[4]	A8	SUP3	DIO	I	DIO4	SPI data input (master) / data output (slave)
SPI_MOSI[4]	B8	SUP3	DIO	I	DIO4	SPI data output (master) / data input (slave)
SPI_CS_IN[4]	D9	SUP3	DI	I	DIO4	SPI chip select input (slave)
Digital power supply						
VDDI	J1; U13; A6	SUP1	Supply		CS2	Digital core supply
VDDI_AD	M14	SUP2	Supply		CS2	Core supply for digital logic on analog die - has to be connected to 1.4/1.8 V rail
VSSI	H1; U14; A7	-	Ground		CG2	Digital core ground
VSSI_AD	M15	-	Ground		CG2	Digital core ground of analog die
Peripheral power supply						
VDDE_IOA	D1; M1	SUP4	Supply		PS1	Peripheral supply NAND flash controller
VDDE_IOB	L1; U7	SUP8	Supply		PS1	Peripheral supply LCD interface / SDRAM interface

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

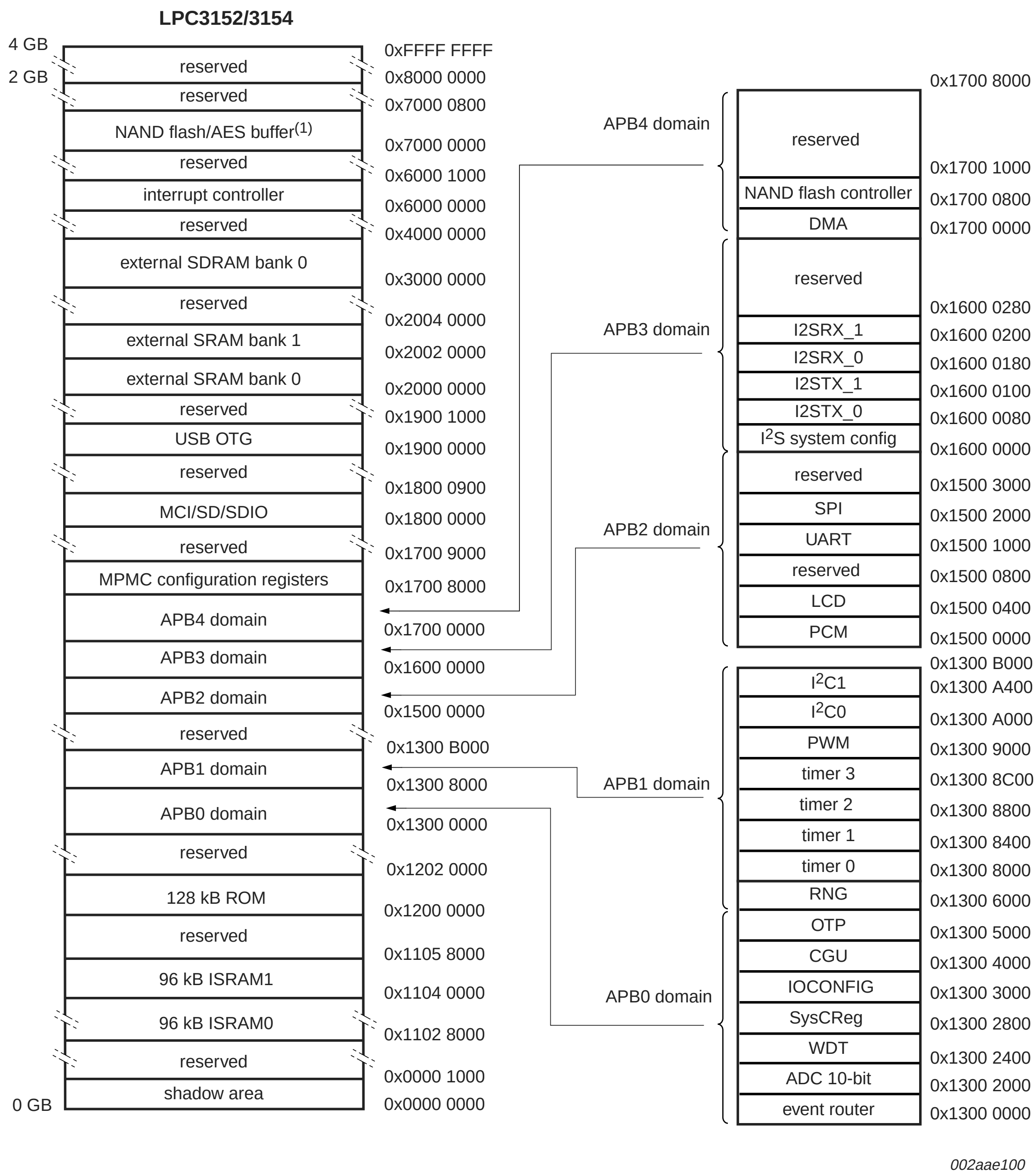
TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
I2SRX_BCK0[4]	T9	SUP3	DIO / GPIO	I	DIO1	I^2S input bitclock
I2SRX_WS0[4]	R9	SUP3	DIO / GPIO	I	DIO1	I^2S input word select
I^2S/Digital audio output						
mI2STX_DATA0[4]	T13	SUP3	DO / GPIO	O	DIO1	I^2S output serial data out
mI2STX_BCK0[4]	T12	SUP3	DO / GPIO	O	DIO1	I^2S output bitclock
mI2STX_WS0[4]	R12	SUP3	DO / GPIO	O	DIO1	I^2S output word select
mI2STX_CLK0[4]	T11	SUP3	DO / GPIO	O	DIO1	I^2S output serial clock
General Purpose IO (IOCONFIG module)						
GPIO0[8]	R13	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 0 (mode pin 0)
GPIO1[8]	T14	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 1 (mode pin 1)
GPIO2[8]	P12	SUP3	GPIO	I	DIO1	General Purpose IO pin 2 (mode pin 2/blinking LED)
GPIO3	D12	SUP3	GPIO	I	DIO1	General Purpose IO pin 3 (connect to PSU_STOP)[5]
GPIO4	D11	SUP3	GPI	I	DIO1	General Purpose Input pin 4
mGPIO5[4]	D7	SUP3	GPIO	I	DIO4	General Purpose IO pin 5
mGPIO6[4]	B7	SUP3	GPIO	I	DIO4	General Purpose IO pin 6
mGPIO7[4]	C7	SUP3	GPIO	I	DIO4	General Purpose IO pin 7
mGPIO8[4]	D6	SUP3	GPIO	I	DIO4	General Purpose IO pin 8
mGPIO9[4]	B6	SUP3	GPIO	I	DIO4	General Purpose IO pin 9
mGPIO10[4]	C6	SUP3	GPIO	I	DIO4	General Purpose IO pin 10
External Bus Interface (NAND flash controller)						
EBI_A_0_ALE[4]	C4	SUP4	DO	O	DIO4	EBI Address Latch Enable (ALE)
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI Command Latch Enable (CLE)
EBI_D_0[4]	J3	SUP4	DIO	I	DIO4	EBI Data I/O 0
EBI_D_1[4]	H3	SUP4	DIO	I	DIO4	EBI Data I/O 1
EBI_D_2[4]	H4	SUP4	DIO	I	DIO4	EBI Data I/O 2
EBI_D_3[4]	G4	SUP4	DIO	I	DIO4	EBI Data I/O 3
EBI_D_4[4]	F4	SUP4	DIO	I	DIO4	EBI Data I/O 4
EBI_D_5[4]	F3	SUP4	DIO	I	DIO4	EBI Data I/O 5
EBI_D_6[4]	E4	SUP4	DIO	I	DIO4	EBI Data I/O 6
EBI_D_7[4]	E3	SUP4	DIO	I	DIO4	EBI Data I/O 7
EBI_D_8[4]	D3	SUP4	DIO	I	DIO4	EBI Data I/O 8
EBI_D_9[4]	A3	SUP4	DIO	I	DIO4	EBI Data I/O 9
EBI_D_10[4]	C2	SUP4	DIO	I	DIO4	EBI Data I/O 10
EBI_D_11[4]	D2	SUP4	DIO	I	DIO4	EBI Data I/O 11
EBI_D_12[4]	E2	SUP4	DIO	I	DIO4	EBI Data I/O 12
EBI_D_13[4]	F2	SUP4	DIO	I	DIO4	EBI Data I/O 13

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
EBI_D_14[4]	G2	SUP4	DIO	I	DIO4	EBI Data I/O 14
EBI_D_15[4]	H2	SUP4	DIO	I	DIO4	EBI Data I/O 15
EBI_DQM_0_NOE[4]	K3	SUP4	DO	O	DIO4	EBI read enable (active LOW)
EBI_NWE[4]	K4	SUP4	DO	O	DIO4	EBI write enable (active LOW)
NAND_NCS_0[4]	L2	SUP4	DO	O	DIO4	EBI chip enable 0
NAND_NCS_1[4]	L3	SUP4	DO	O	DIO4	EBI chip enable 1
NAND_NCS_2[4]	L4	SUP4	DO	O	DIO4	EBI chip enable 2
NAND_NCS_3[4]	M2	SUP4	DO	O	DIO4	EBI chip enable 3
mNAND_RYBN0[4]	B5	SUP4	DI	I	DIO4	EBI NAND ready/busy 0
mNAND_RYBN1[4]	C5	SUP4	DI	I	DIO4	EBI NAND ready/busy 1
mNAND_RYBN2[4]	D5	SUP4	DI	I	DIO4	EBI NAND ready/busy 2
mNAND_RYBN3[4]	D4	SUP4	DI	I	DIO4	EBI NAND ready/busy 3
EBI_NCAS_BLOUT_0[4]	J2	SUP4	DO	O	DIO4	EBI lower lane byte select (7:0)
EBI_NRAS_BLOUT_1[4]	J4	SUP4	DO	O	DIO4	EBI upper lane byte select (15:8)
Secure one time programmable memory						
VPP[7]	C9	SUP1/ SUP3	Supply		PS3	Supply for polyfuse programming
Real Time Clock (RTC)						
RTC_VDD36	L15	SUP6	Supply		CS1	RTC supply connected to battery
RTC_VSS	M17	-	Ground		CG1	RTC ground
FSLOW_OUT	L16	SUP7	AO		AIO2	RTC 32.768 kHz clock output
FSLOW_IN	L17	SUP7	AI		AIO2	RTC 32.768 kHz clock input
RTC_INT	M16	SUP6	DO	O	AIO2	RTC interrupt (HIGH active)
RTC_BACKUP	K14	SUP7	Supply		CS1	RTC backup capacitor connection
RTC_CLK32	U17	SUP6	AO	O	AIO2	RTC 32 kHz clock output for on-board applications such as tuner
Power supply unit						
PSU_VBUS	J16	SUP5	Supply		CS1	PSU USB supply voltage
PSU_VOUT1	H14	SUP3	AO		CS1	PSU output1
PSU_LX1	H15	-	AIO		CS1	PSU external coil terminal for output1
PSU_LX2	G17	-	AIO		CS1	PSU external coil terminal for output2
PSU_VSS1	H16	-	Ground		CG1	PSU ground
PSU_VIN1	G16	-	AI		CS1	PSU output1 input voltage
PSU_VOUT2	G14	SUP1	AO		CS1	PSU output2
PSU_VOUT3	E17	SUP2	AO		CS1	PSU output3
PSU_VSSA	D16	-	Ground		CG1	PSU ground
PSU_VSSA_CLEAN	D17	-	Ground		CG1	PSU reference circuit ground
PSU_PLAY	C17	SUP3	AI	I	AIO2	PSU play button input (active HIGH)

6.2 Memory map



(1) AES is available on the LPC3154 only.

Fig 3. LPC3152/3154 memory map

6.2.1 Analog die memory organization

The blocks on the analog die (Audio codec, RTC, Li-ion charger, and Power Supply Unit (PSU)) and their registers are accessed through the I^2C1-bus interface as a single slave device with device address 0x0C using the following register addresses:

6.6 External Bus Interface (EBI)

The EBI module acts as multiplexer with arbitration between the NAND flash and the SDRAM/SRAM memory modules connected externally through the MPMC.

The main purpose for using the EBI module is to save external pins. However only data and address pins are multiplexed. Control signals towards and from the external memory devices are not multiplexed.

Table 8. Memory map of the external SRAM/SDRAM memory modules

Module	Maximum address space		Data width	Device size
External SRAM0	0x2000 0000	0x2000 FFFF	8 bit	64 kB
	0x2000 0000	0x2001 FFFF	16 bit	128 kB
External SRAM1	0x2002 0000	0x2002 FFFF	8 bit	64 kB
	0x2002 0000	0x2003 FFFF	16 bit	128 kB
External SDRAM0	0x3000 0000	0x37FF FFFF	16 bit	128 MB

6.7 Internal ROM Memory

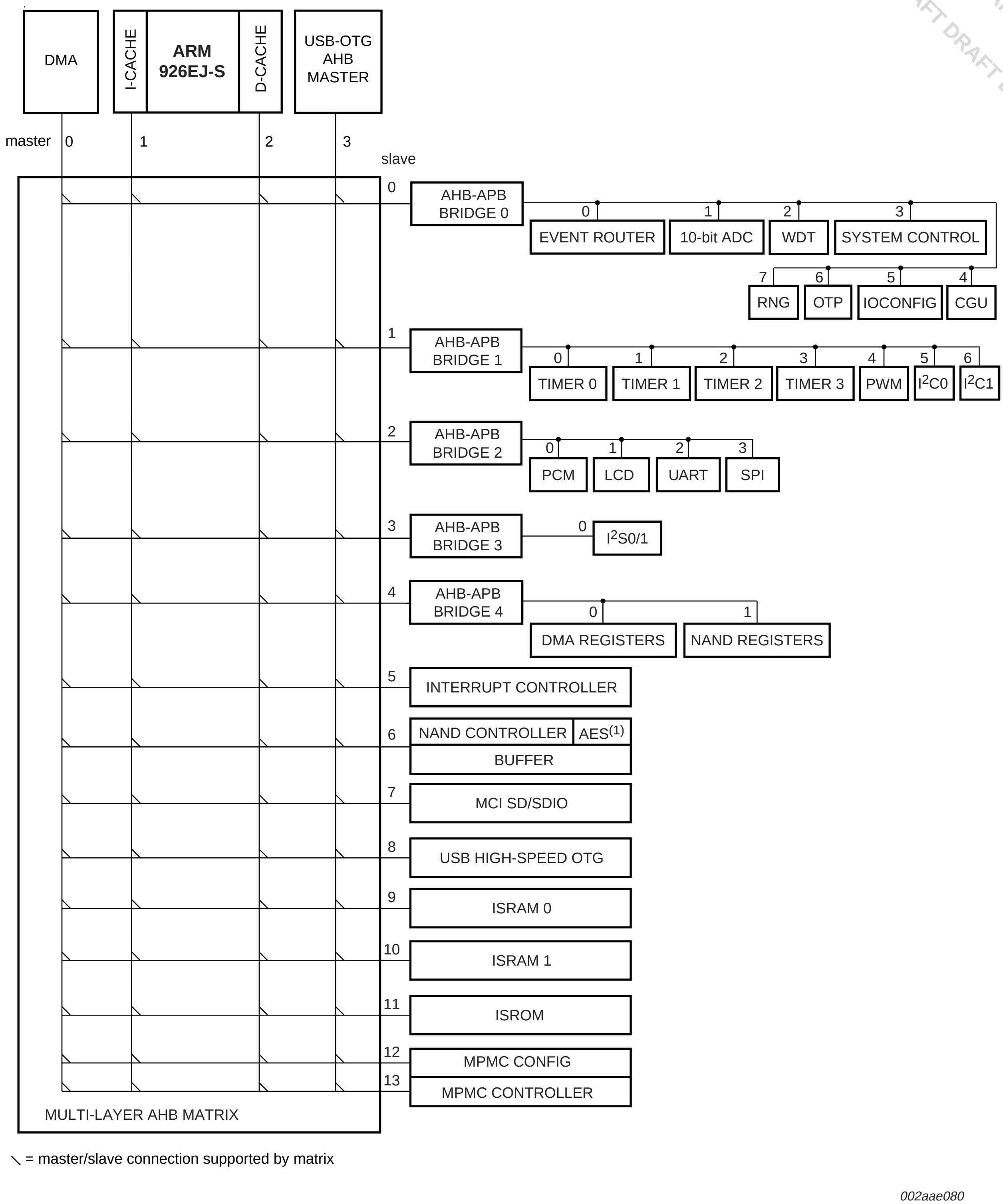
The internal ROM memory is used to store the boot code of the LPC3152/3154. After a reset, the ARM processor will start its code execution from this memory.

The LPC3154 ROM memory has the following features:

- Supports secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports SHA1 hash checking on the boot image.
- Supports un-secure boot from UART and USB (DFU class) interfaces during development. Once the AES key is programmed in the OTP, only secure boot is allowed through UART and USB.
- Supports secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The LPC3152 ROM memory has the following features:

- Supports non-secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Supports non-secure booting from UART and USB (DFU class) interfaces during development.
- Supports non-secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.



(1) AES decryption engine is available on LPC3154 only.

Fig 5. LPC3152/3154 AHB multi-layer matrix connections

This module has the following features:

The SPI/SSI-bus is a 5-wire interface, and it is suitable for low, medium, and high data rate transfers.

This module has the following features:

- Supports Motorola SPI frame format with a word size of 8/16 bits.
- Texas Instruments SSI (Synchronous Serial Interface) frame format with a word size of 4 bit to 16 bit.
- Receive FIFO and transmit FIFO of 64 half-words each.
- Serial clock rate master mode maximum 45 MHz.
- Serial clock rate slave mode maximum 25 MHz.
- Support for single data access DMA.
- Full-duplex operation.
- Supports up to three slaves.
- Supports maskable interrupts.
- Supports DMA transfers.

6.24 Universal Asynchronous Receiver Transmitter (UART)

The UART module supports the industry standard serial interface.

This module has the following features:

- Programmable baud rate with a maximum of 1049 kBd.
- Programmable data length (5 bit to 8 bit).
- Implements only asynchronous UART.
- Transmit break character length indication.
- Programmable one to two stops bits in transmission.
- Odd/even/force parity check/generation.
- Frame error, overrun error and break detection.
- Automatic hardware flow control.
- Independent control of transmit, receive, line status, data set interrupts, and FIFOs.
- SIR-IrDA encoder/decoder (from 2400 to 115 kBd).
- Supports maskable interrupts.
- Supports DMA transfers.

6.25 Pulse Code Modulation (PCM) interface

The PCM interface supports the PCM and IOM interfaces.

This module has the following features:

- Four-wire serial interface.
- Can function in both Master and Slave modes.
- Supports:
  - MP PCM (Multi-Protocol PCM): Configurable directional per slot.

Table 11. Pin descriptions of multiplexed pins

Pin name	Default signal	Alternate signal	Description
mLCD_DB_3	LCD_DB_3	EBI_A_3	**LCD_DB_3 —** LCD bidirectional data line 3. **EBI_A_3 —** EBI address line 3.
mLCD_DB_4	LCD_DB_4	EBI_A_4	**LCD_DB_4 —** LCD bidirectional data line 4. **EBI_A_4 —** EBI address line 4.
mLCD_DB_5	LCD_DB_5	EBI_A_5	**LCD_DB_5 —** LCD bidirectional data line 5. **EBI_A_5 —** EBI address line 5.
mLCD_DB_6	LCD_DB_6	EBI_A_6	**LCD_DB_6 —** LCD bidirectional data line 6. **EBI_A_6 —** EBI address line 6.
mLCD_DB_7	LCD_DB_7	EBI_A_7	**LCD_DB_7 —** LCD bidirectional data line 7. **EBI_A_7 —** EBI address line 7.
mLCD_DB_8	LCD_DB_8	EBI_A_8	**LCD_DB_8 —** LCD bidirectional data line 8. **EBI_A_8 —** EBI address line 8.
mLCD_DB_9	LCD_DB_9	EBI_A_9	**LCD_DB_9 —** LCD bidirectional data line 9. **EBI_A_9 —** EBI address line 9.
mLCD_DB_10	LCD_DB_10	EBI_A_10	**LCD_DB_10 —** LCD bidirectional data line 10. **EBI_A_10 —** EBI address line 10.
mLCD_DB_11	LCD_DB_11	EBI_A_11	**LCD_DB_11 —** LCD bidirectional data line 11. **EBI_A_11 —** EBI address line 11.
mLCD_DB_12	LCD_DB_12	EBI_A_12	**LCD_DB_12 —** LCD bidirectional data line 12. **EBI_A_12 —** EBI address line 12.
mLCD_DB_13	LCD_DB_13	EBI_A_13	**LCD_DB_13 —** LCD bidirectional data line 13. **EBI_A_13 —** EBI address line 13.
mLCD_DB_14	LCD_DB_14	EBI_A_14	**LCD_DB_14 —** LCD bidirectional data line 14. **EBI_A_14 —** EBI address line 14.
mLCD_DB_15	LCD_DB_15	EBI_A_15	**LCD_DB_15 —** LCD bidirectional data line 15. **EBI_A_15 —** EBI address line 15.
Storage related pin multiplexing			
mGPIO5	GPIO5	MCI_CLK	**GPIO5 —** General Purpose I/O pin 5. **MCI_CLK —** MCI card clock.
mGPIO6	GPIO6	MCI_CMD	**GPIO_6 —** General Purpose I/O pin 6. **MCI_CMD —** MCI card command input/output.
mGPIO7	GPIO7	MCI_DAT_0	**GPIO7 —** General Purpose I/O pin 7. **MCI_DAT_0 —** MCI card data input/output line 0.
mGPIO8	GPIO8	MCI_DAT_1	**GPIO8 —** General Purpose I/O pin 8. **MCI_DAT_1 —** MCI card data input/output line 1.
mGPIO9	GPIO9	MCI_DAT_2	**GPIO9 —** General Purpose I/O pin 9. **MCI_DAT_2 —** MCI card data input/output line 2.
mGPIO10	GPIO10	MCI_DAT_3	**GPIO10 —** General Purpose I/O pin 10. **MCI_DAT_3 —** MCI card data input/output line 3.

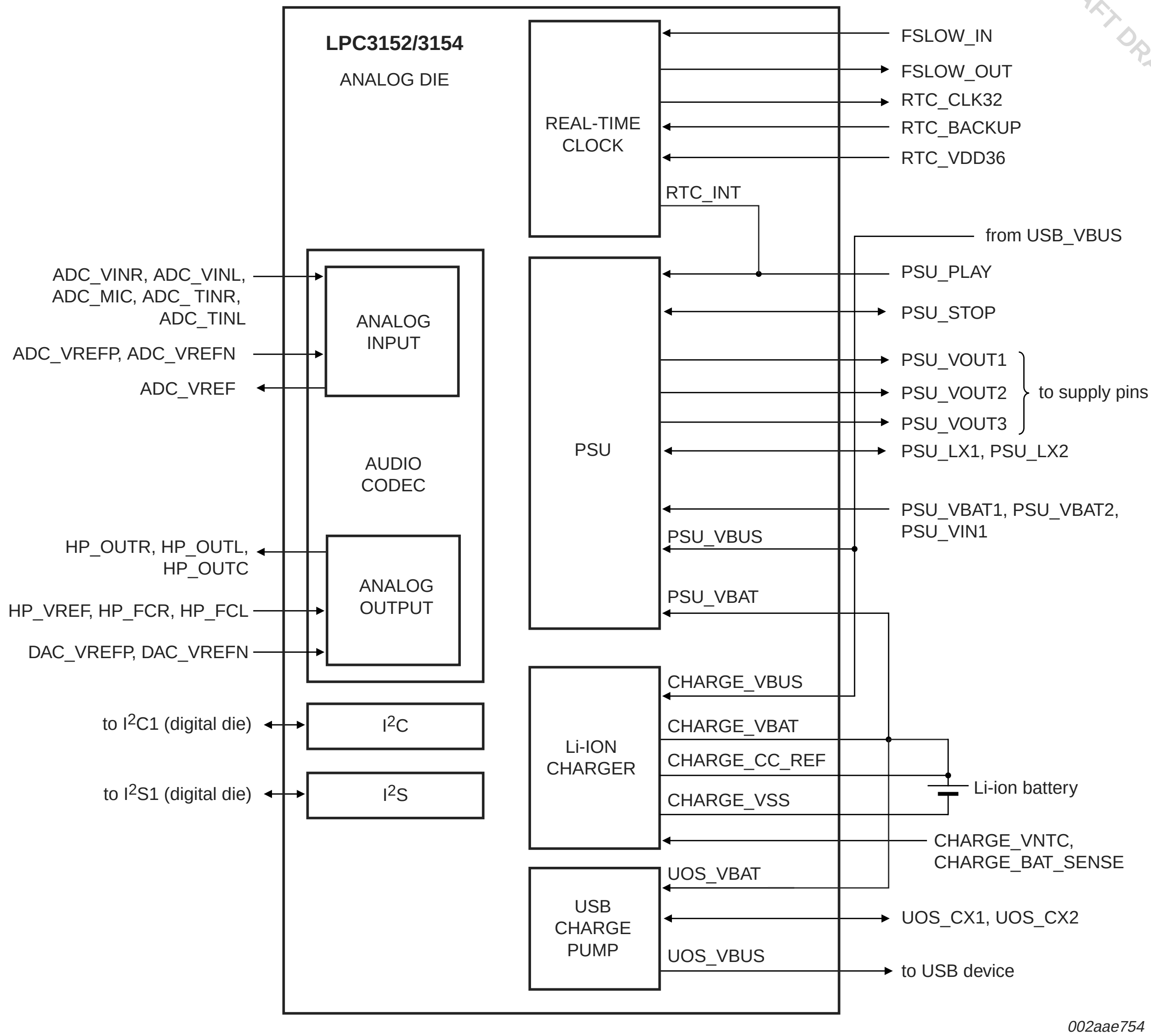


Fig 11. Block diagram of the analog die

7.2 Audio codec

7.2.1 Stereo Digital-to-Analog Converter (SDAC)

The Stereo Digital-to-Analog Converter converts a digital audio signal into an analog audio signal. The output of this module is connected to the input of the class AB headphone amplifier.

This module has the following features:

- Stereo Digital-to-Analog converter with support for 24-bit audio samples.
- Supports sample rates from 8 kHz up to 96 kHz.
- Filter implementations have a 24-bit data path with 16-bit coefficients.
- Full FIR filter implementation for all of the up-sampling filters.

- The nominal charge current is programmed with an external program-resistor. This allows the charge current to be adapted to the USB enumeration.
- Uses a widespread method to charge a Li-ion battery with the following stages:
  - Trickle charging with a small current for an (almost) empty battery.
  - Fast charging in Constant Current mode (CC mode) to the maximum battery voltage of 4.2 V ± 1%.
  - Switch from CC mode to Constant Voltage charging (CV mode) keeping the battery voltage at 4.2 V and monitoring the current for ending the charge process.
- Short circuit resistant.
- Charger state can be observed through a register.

7.4 USB charge pump (host mode)

The USB charge pump uses the Li-ion battery to provide a low-power USB VBUS signal for the USB controller in host mode.

7.5 Power Supply Unit (PSU)

The integrated PSU allows the system to run directly from the battery voltage or the USB power supply voltage USB_VBUS. It converts the battery voltage or the USB_VBUS voltage into the supply voltages required for both the digital and analog blocks in the rest of the system.

8. Limiting values

Table 12. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
All digital I/O pins							
V_i	input voltage			–0.5	-	+3.6	V
V_o	output voltage			–0.5	-	+3.6	V
I_o	output current	VDDE_IOC = 3.3 V		-	4	-	mA
Temperature values							
T_j	junction temperature			–40	25	125	°C
T_{stg}	storage temperature		[2]	–65	-	+150	°C
T_{amb}	ambient temperature			–40	+25	+85	°C
Electrostatic handling							
V_{ESD}	electrostatic discharge voltage	human body model	[3]	–500	-	+500	V
		machine model		–100	-	+100	V
		charged device model		-	500	-	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Dependent on package type.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

9.1 Digital die

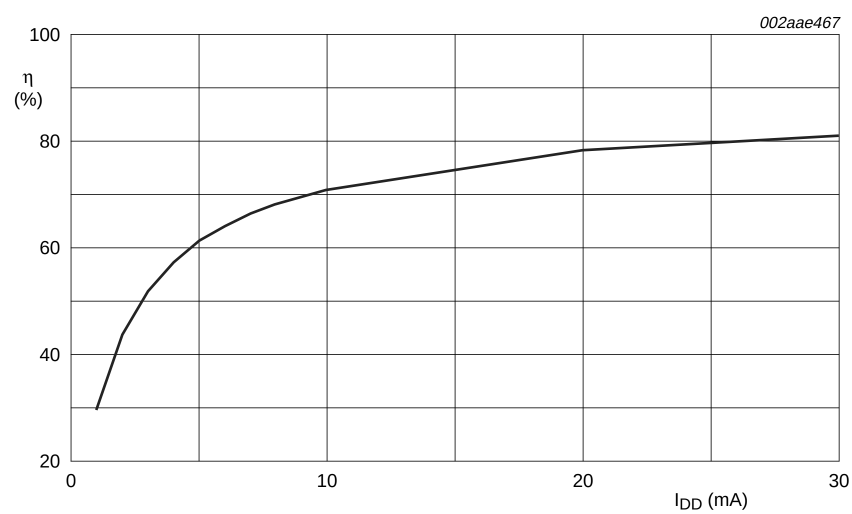
Table 13: Static characteristics
T_{amb} = –40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pins						
$V_{DD(IO)}$	input/output supply voltage	NAND flash controller pads (SUP4) and LCD interface (SUP8); 1.8 V mode	1.65	1.8	1.95	V
		NAND flash controller pads (SUP4) and LCD interface (SUP8); 3.3 V mode	2.5	3.3	3.6	V
		other peripherals (SUP 3)	2.7	3.3	3.6	V
$V_{DD(CORE)}$	core supply voltage	(SUP1)	1.1	1.2	1.3	V

Table 18. Efficiency of output on PSU_VOUT1 (PSU_VOUT1 programmed to 2.86 V)

I_{BAT} / mA on pin PSU_VBAT	V_{BAT} / V	I_{DD} / mA (SUP3)	V_{DD} / V (SUP4)	Efficiency / %
2	3.602	1	2.8676	39.80566352
2.8	3.6016	2	2.864	56.80015231
3.598	-	3	2.8605	66.22816876
4.396	3.601	4	2.8569	72.18953182
5.195	3.6006	5	2.8533	76.27057345
5.994	3.6003	6	2.8498	79.23374865
6.793	3.5999	7	2.8462	81.47256753
7.59	3.5995	8	2.8426	83.23802841
8.388	3.5992	9	2.83991	84.63671469
9.231	3.5988	10	2.8542	85.9167695
13.32	3.597	15	2.8549	89.37941277
17.368	3.595	20	2.837	90.87420537
25.59	3.591	30	2.8198	92.056375145

9.2.1.2 PSU_VOUT2 efficiency



SUP1 = 1.07 V.

SUP2: V_{DD} = 1.398 V, I_{DD} = 0 mA.

SUP3: V_{DD} = 2.912 V, I_{DD} = 0 mA.

PSU_VOUT2 = 1.07 V.

Fig 17. Efficiency PSU_VOUT2

10. Dynamic characteristics

10.1 Digital die

10.1.1 LCD controller

10.1.1.1 Intel 8080 mode

Table 21. Dynamic characteristics: LCD controller in Intel 8080 mode

C_L = 25 pF, T_{amb} = –40 °C to +85 °C, unless otherwise specified; $V_{DD(IO)}$ = 1.8 V and 3.3 V (SUP8).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(A)}$	address set-up time			-	1 × LCDCLK	-	ns
$t_{h(A)}$	address hold time			-	2 × LCDCLK	-	ns
$t_{cy(a)}$	access cycle time		[1]	-	5 × LCDCLK	-	ns
$t_{w(en)W}$	write enable pulse width		[1]	-	2 × LCDCLK	-	ns
$t_{w(en)R}$	read enable pulse width		[1]	-	2 × LCDCLK	-	ns
t_r	rise time			2	-	5	ns
t_f	fall time			2	-	5	ns
$t_{su(D)}$	data input set-up time			<tbd>	-	-	ns
$t_{h(D)}$	data input hold time			<tbd>	-	-	ns
$t_{d(QV)}$	data output valid delay time			-	–1 × LCDCLK	-	ns
$t_{dis(Q)}$	data output disable time			-	2 × LCDCLK	-	ns

[1] Timing is determined by the LCD Interface Control Register fields: INVERT_CS = 1; MI = 0; PS = 0; INVERT_E_RD = 0. See the *LPC315x user manual*.

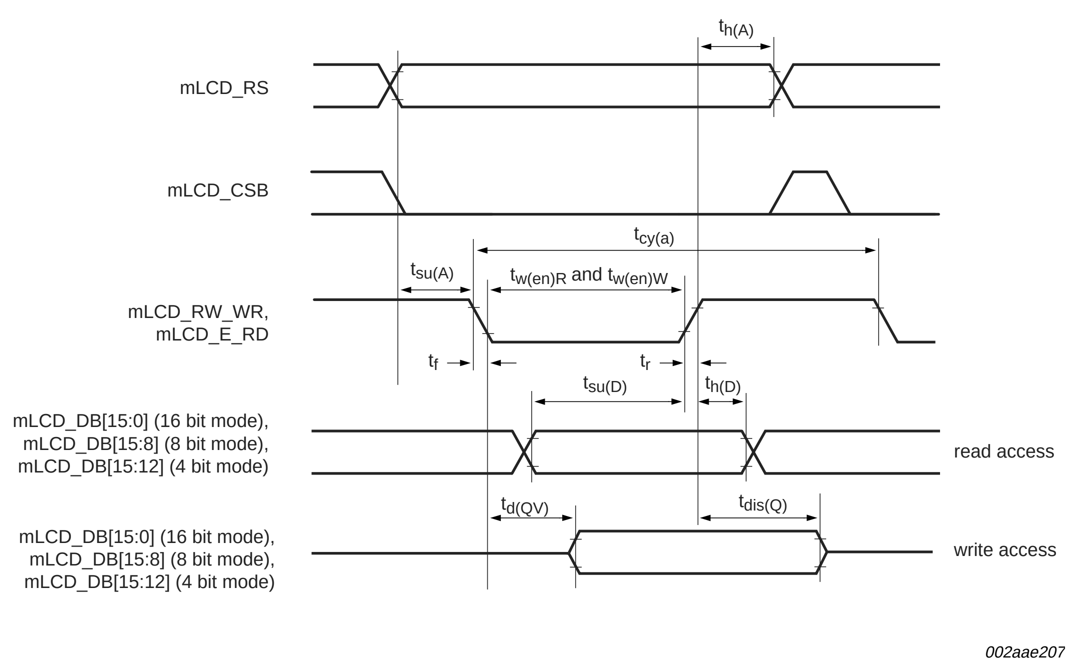


Fig 18. LCD timing (Intel 8080 mode)

10.1.1.2 Motorola 6800 mode

Table 22. Dynamic characteristics: LCD controller in Motorola 6800 mode

C_L = 25 pF, T_{amb} = −40 °C to +85 °C, unless otherwise specified; $V_{DD(IO)}$ = 1.8 V and 3.3 V (SUP8).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(A)}$	address set-up time		-	1 × LCDCLK	-	ns
$t_{h(A)}$	address hold time		-	2 × LCDCLK	-	ns
$t_{cy(a)}$	access cycle time	[1]	-	5 × LCDCLK	-	ns
t_r	rise time		2	-	5	ns
t_f	fall time		2	-	5	ns
$t_{su(D)}$	data input set-up time		<tbd>	-	-	ns
$t_{h(D)}$	data input hold time		<tbd>	-	-	ns
$t_{d(QV)}$	data output valid delay time		-	−1 × LCDCLK	-	ns
$t_{dis(Q)}$	data output disable time		-	2 × LCDCLK	-	ns
$t_{w(en)}$	enable pulse width	read cycle	-	2 × LCDCLK	-	ns
		write cycle	-	2 × LCDCLK	-	ns

[1] Timing is derived from the LCD Interface Control Register fields: INVERT_CS = 1; MI = 1; PS = 0; INVERT_E_RD = 0. See the *LPC315x user manual*.

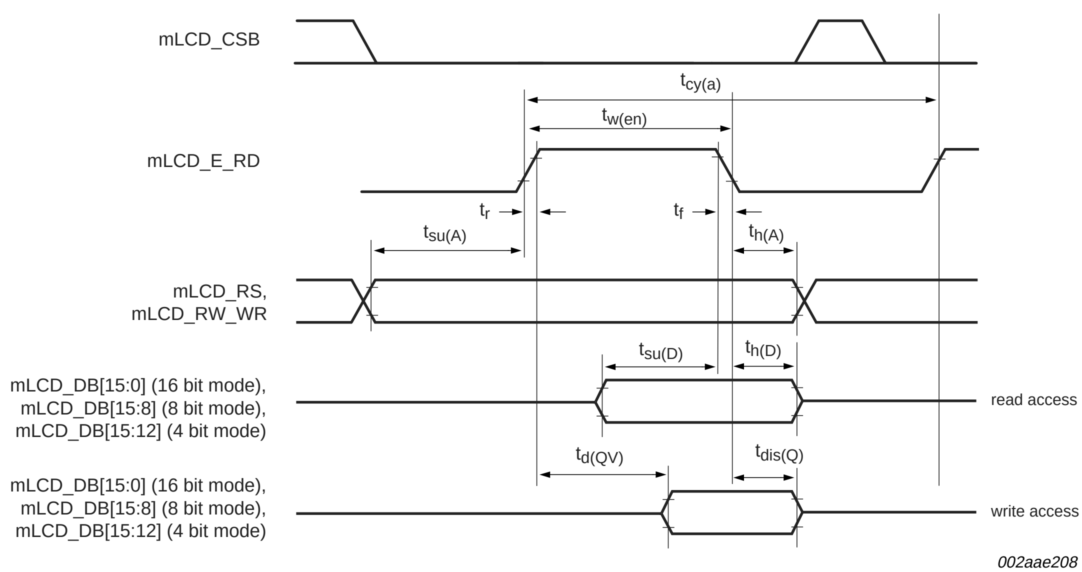
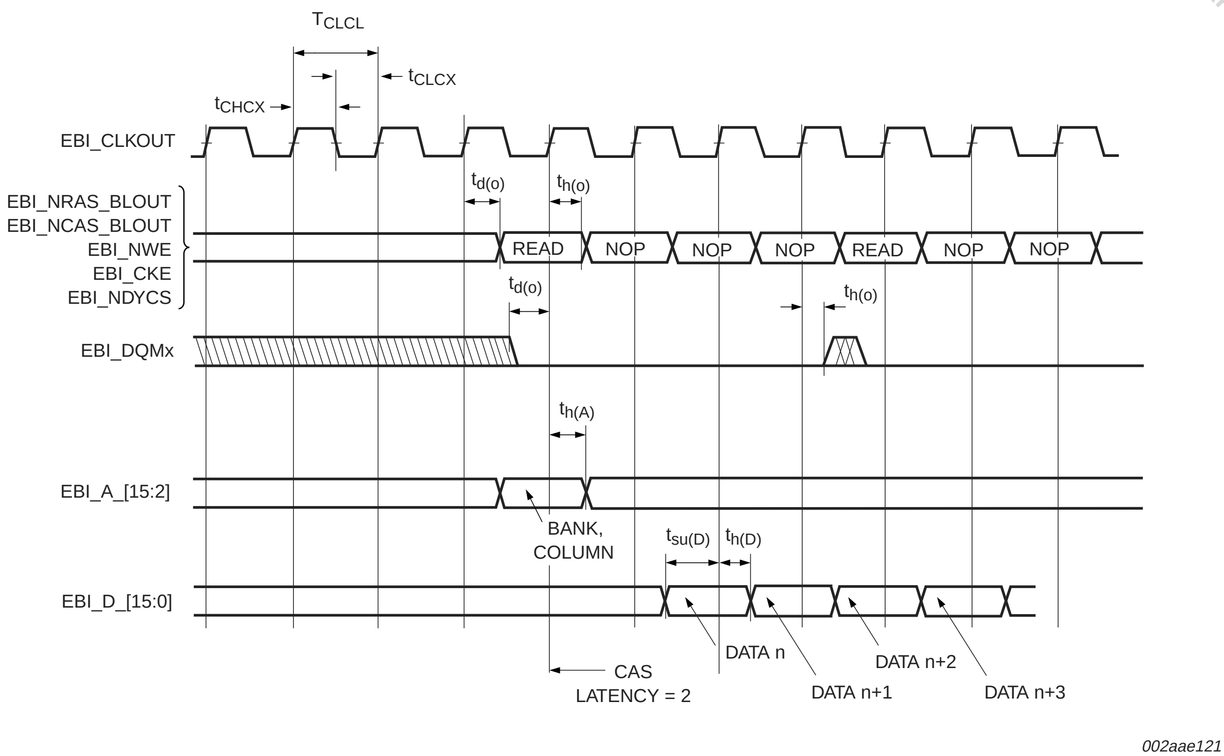


Fig 19. LCD timing (Motorola 6800 mode)



EBI_CKE is HIGH.

Fig 23. SDRAM burst read timing

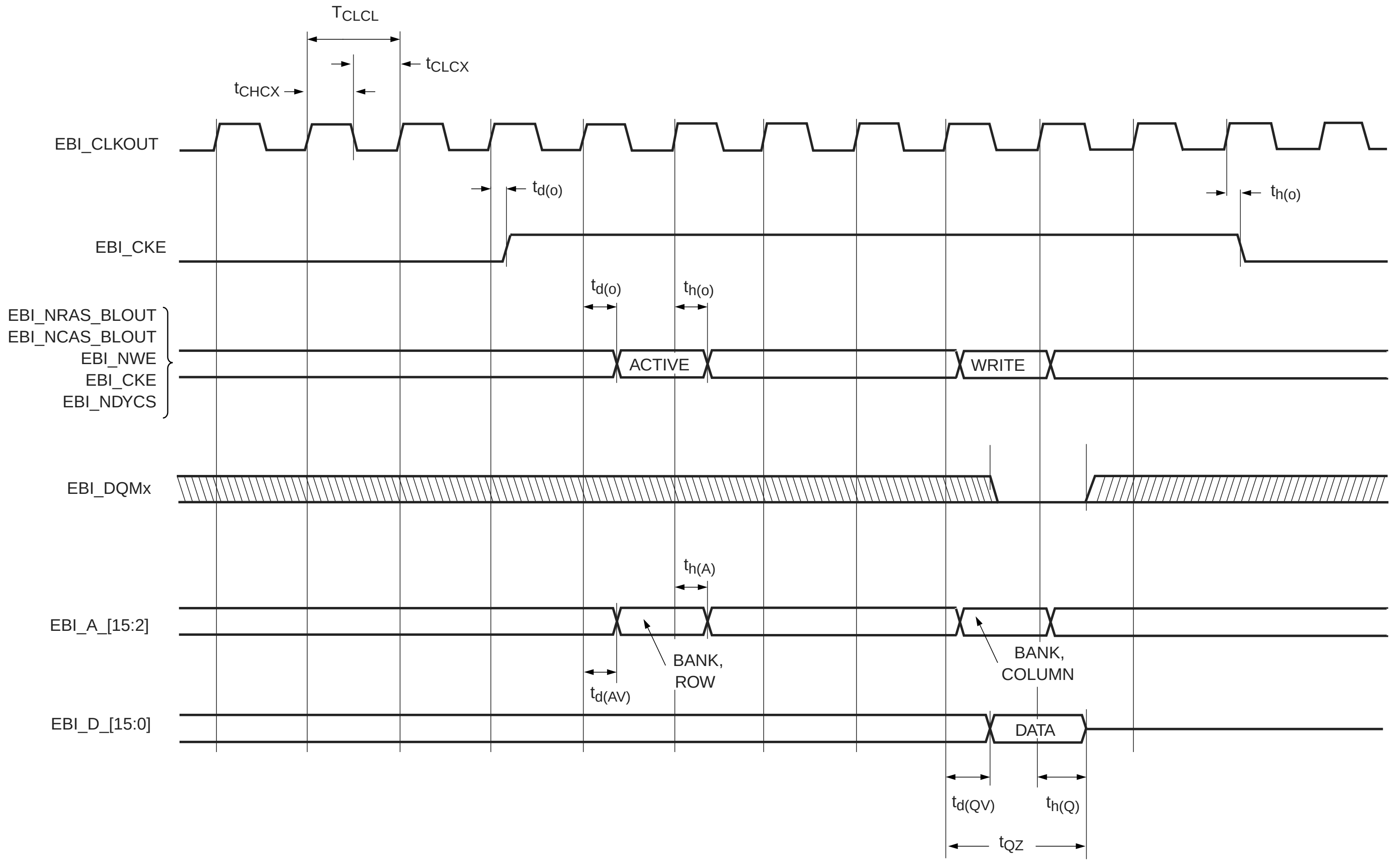


Fig 24. SDRAM bank activate and write timing

10.2.1 Crystal oscillator

Table 27: Dynamic characteristics: crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency		10	12	25	MHz
δ_{clk}	clock duty cycle		45	50	55	%
C_{xtal}	crystal capacitance	input; on pin FFAST_IN	-	-	2	pF
		output; on pin FFAST_OUT	-	-	0.74	pF
$t_{startup}$	start-up time		-	500	-	µs
P_{drive}	drive power		100	-	500	µW

10.2.2 SPI

Table 28. Dynamic characteristics of SPI pins
T_{amb} = −40 °C to +85 °C for industrial applications

Symbol	Parameter	Min	Typ	Max	Unit
SPI master					
T_{SPICYC}	SPI cycle time	22.2	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	11.09	-	11.14	ns
$t_{SPICLKL}$	SPICLK LOW time	11.09	-	11.14	ns
t_{SPIDSU}	SPI data set-up time	<tbd>	<tbd>	<tbd>	ns
t_{SPIDH}	SPI data hold time	<tbd>	<tbd>	<tbd>	ns
t_{SPIQV}	SPI data output valid time	-	-	14	ns
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns
SPI slave					
T_{SPICYC}	SPI cycle time	<tbd>	40	<tbd>	ns
$t_{SPICLKH}$	SPICLK HIGH time	<tbd>	20	<tbd>	ns
$t_{SPICLKL}$	SPICLK LOW time	<tbd>	20	<tbd>	ns
t_{SPIDSU}	SPI data set-up time	<tbd>	<tbd>	<tbd>	ns
t_{SPIDH}	SPI data hold time	<tbd>	<tbd>	<tbd>	ns
t_{SPIQV}	SPI data output valid time	<tbd>	<tbd>	14	ns
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagrams.

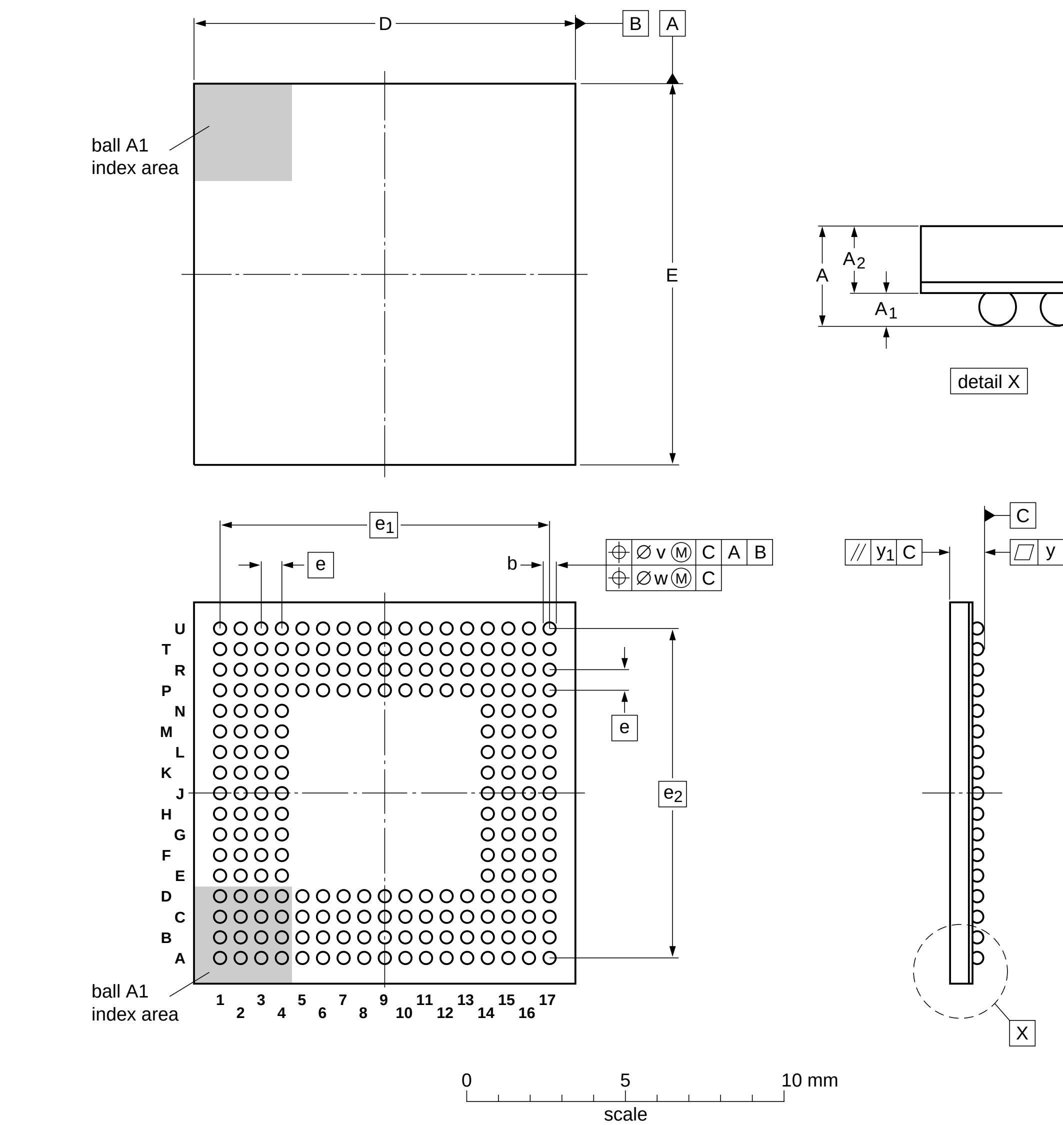
12. Marking

Table 37. LPC3152/3154 Marking

Line	Marking	Description
A	LPC3152/3154	BASIC_TYPE

13. Package outline

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 12 x 12 x 0.7 mm **SOT930-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.35 0.25	0.80 0.65	0.45 0.35	12.1 11.9	12.1 11.9	0.65	10.4	10.4	0.15	0.05	0.08	0.1

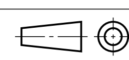
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT930-1		- - -				~~05-12-08~~ 06-01-03

Fig 35. LPC3152/3154 TFBGA208 package outline

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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