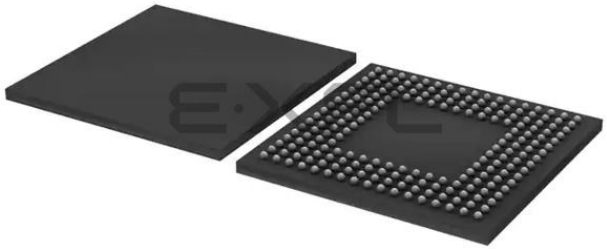

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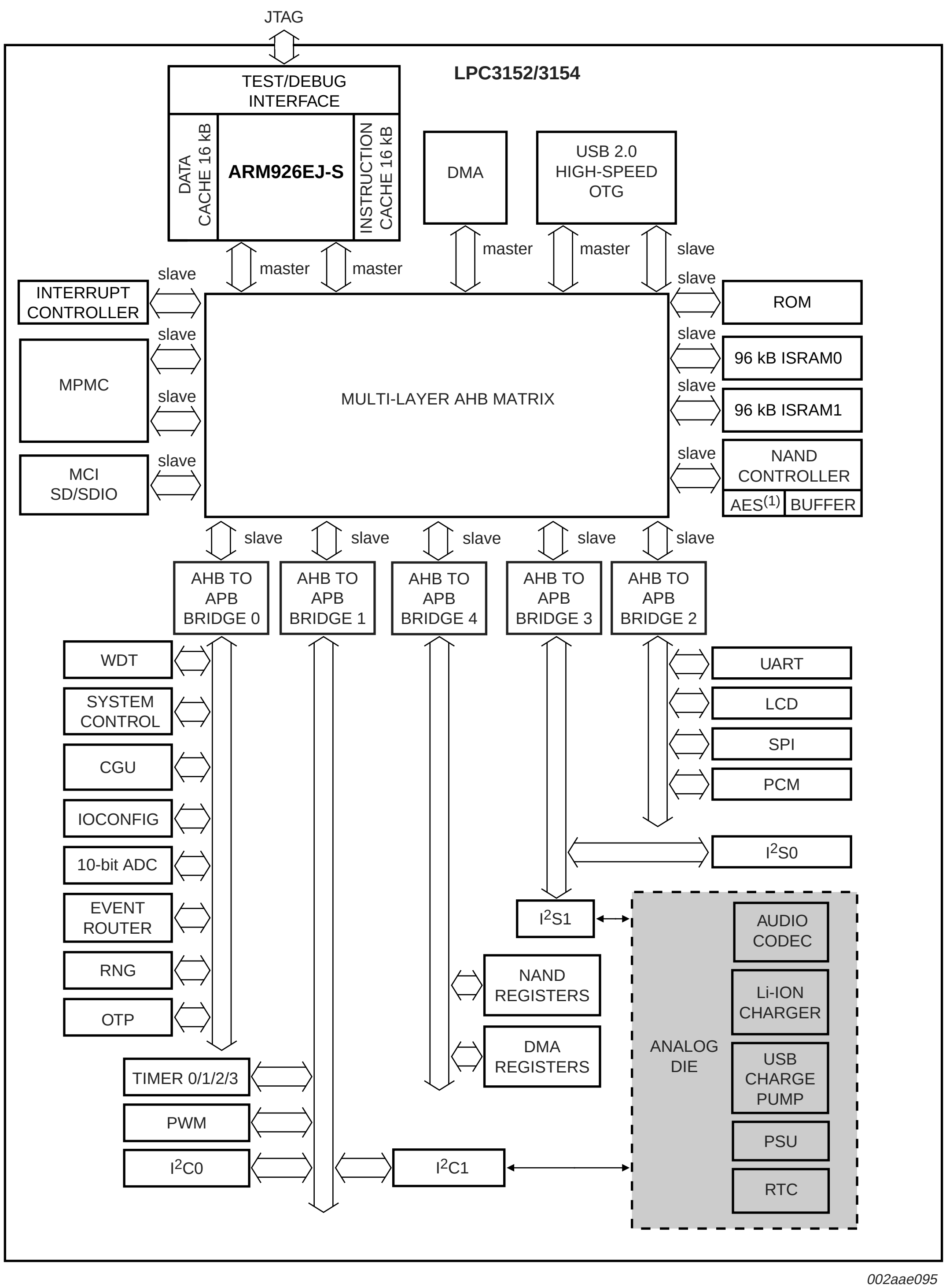
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, PCM, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	10
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3154fet208-551

4. Block diagram



(1) AES decryption engine available in LPC3154 only.

Fig 1. LPC3152/3154 block diagram

Table 3. Pin allocation table *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	I2SRX_WS0	10	UART_RXD	11	mUART_RTS_N	12	mI2STX_WS0
13	GPIO0	14	ADC_VINR	15	ADC_MIC	16	ADC_VREFN
17	UOS_CX1		-		-		-
Row T							
1	USB_DP	2	USB_GNDA	3	USB_VDDA33_DRV	4	mLCD_DB_12
5	mLCD_DB_7	6	mLCD_DB_2	7	mLCD_DB_0	8	mLCD_RW_WR
9	I2SRX_BCK0	10	TDI	11	mI2STX_CLK0	12	mI2STX_BCK0
13	mI2STX_DATA0	14	GPIO1	15	ADC_VINL	16	ADC_VREF
17	ADC_VREFP		-		-		-
Row U							
1	n.c.	2	mLCD_DB_14	3	mLCD_DB_13	4	mLCD_DB_11
5	mLCD_DB_8	6	mLCD_DB_4	7	VDDE_IOB	8	VSSE_IOB
9	TMS	10	JTAGSEL	11	TRST_N	12	TCK
13	VDDI	14	VSSI	15	VDDE_IOC	16	VSSE_IOC
17	RTC_CLK32		-		-		-

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
Clock generation unit						
FFAST_IN	A10	SUP1	AI		AIO2	12 MHz oscillator clock input
FFAST_OUT	B10	SUP1	AO		AIO2	12 MHz oscillator clock output
VDDA12	B11	SUP1	Supply		PS3	12 MHz oscillator/PLLs analog supply
VSSA12	C11	-	Ground		CG1	12 MHz oscillator/PLLs analog ground
RSTIN_N	E15	SUP3	DI	I:PU	DIO2	System reset input (active LOW)
CLOCK_OUT	M4	SUP4	DO	O	DIO4	Clock output
10-bit ADC						
ADC10B_VDDA33	B13	SUP3	Supply		PS3	10-bit ADC analog supply
ADC10B_GNDA	A13	-	Ground		CG1	10-bit ADC analog ground
ADC10B_GPA0	B12	SUP3	AI		AIO1	10-bit ADC analog input
ADC10B_GPA1	C13	SUP3	AI		AIO1	10-bit ADC analog input
ADC10B_GPA2	C12	SUP3	AI		AIO1	10-bit ADC analog input
Audio ADC						
ADC_MIC	R15	-	AI		AIO2	ADC microphone input
ADC_VINL	T15	-	AI		AIO2	ADC line input left
ADC_VINR	R14	-	AI		AIO2	ADC line input right
ADC_TINL	P13	-	AI		AIO2	ADC tuner input left
ADC_TINR	P14	-	AI		AIO2	ADC tuner input right
ADC_VREF	T16	-	AO		AIO2	ADC reference voltage output

Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
VDDE_IOC	U15; A15; A4;	SUP3	Supply		PS1	Peripheral supply
VDDE_IOD	G15	SUP3	Supply		PS2	Analog die peripheral supply
VSSE_IOA	E1; N1	-	Ground		PG1	Peripheral ground NAND flash controller
VSSE_IOB	K1; U8	-	Ground		PG1	Peripheral ground LCD interface / SDRAM interface
VSSE_IOC	U16; A14; A5;	-	Ground		PG1	Peripheral ground
VSSE_IOD	L14	-	Ground		PG2	Analog die peripheral ground
LCD interface						
mLCD_CSB[4]	R8	SUP8	DO	O	DIO4	LCD chip select (active LOW)
mLCD_E_RD[4]	P7	SUP8	DO	O	DIO4	LCD: 6800 enable, 8080 read enable (active HIGH)
mLCD_RS[4]	R7	SUP8	DO	O	DIO4	LCD: instruction register (LOW)/ data register (HIGH) select
mLCD_RW_WR[4]	T8	SUP8	DO	O	DIO4	LCD: 6800 read/write select,8080 write enable (active HIGH)
mLCD_DB_0[4]	T7	SUP8	DIO	O	DIO4	LCD Data 0
mLCD_DB_1[4]	P8	SUP8	DIO	O	DIO4	LCD Data 1
mLCD_DB_2[4]	T6	SUP8	DIO	O	DIO4	LCD Data 2
mLCD_DB_3[4]	R6	SUP8	DIO	O	DIO4	LCD Data 3
mLCD_DB_4[4]	U6	SUP8	DIO	O	DIO4	LCD Data 4
mLCD_DB_5[4]	P6	SUP8	DIO	O	DIO4	LCD Data 5
mLCD_DB_6[4]	R5	SUP8	DIO	O	DIO4	LCD Data 6
mLCD_DB_7[4]	T5	SUP8	DIO	O	DIO4	LCD Data 7
mLCD_DB_8[4]	U5	SUP8	DIO	O	DIO4	LCD Data 8 / 8-bit Data 0
mLCD_DB_9[4]	P5	SUP8	DIO	O	DIO4	LCD Data 9 / 8-bit Data 1
mLCD_DB_10[4]	P4	SUP8	DIO	O	DIO4	LCD Data 10 / 8-bit Data 2
mLCD_DB_11[4]	U4	SUP8	DIO	O	DIO4	LCD Data 11 / 8-bit Data 3
mLCD_DB_12[4]	T4	SUP8	DIO	O	DIO4	LCD Data 12 / 8-bit Data 4 / 4-bit Data 0
mLCD_DB_13[4]	U3	SUP8	DIO	O	DIO4	LCD Data 13 / 8-bit Data 5 / 4-bit Data 1 / serial clock output
mLCD_DB_14[4]	U2	SUP8	DIO	O	DIO4	LCD Data 14 / 8-bit Data 6 / 4-bit Data 2 / serial data input
mLCD_DB_15[4]	R4	SUP8	DIO	O	DIO4	LCD Data 15 / 8-bit Data 7 / 4-bit Data 3 / serial data output
I^2S/Digital audio input						
I2SRX_DATA0[4]	P9	SUP3	DI / GPIO	I	DIO1	I^2S input serial data receive

6.6 External Bus Interface (EBI)

The EBI module acts as multiplexer with arbitration between the NAND flash and the SDRAM/SRAM memory modules connected externally through the MPMC.

The main purpose for using the EBI module is to save external pins. However only data and address pins are multiplexed. Control signals towards and from the external memory devices are not multiplexed.

Table 8. Memory map of the external SRAM/SDRAM memory modules

Module	Maximum address space		Data width	Device size
External SRAM0	0x2000 0000	0x2000 FFFF	8 bit	64 kB
	0x2000 0000	0x2001 FFFF	16 bit	128 kB
External SRAM1	0x2002 0000	0x2002 FFFF	8 bit	64 kB
	0x2002 0000	0x2003 FFFF	16 bit	128 kB
External SDRAM0	0x3000 0000	0x37FF FFFF	16 bit	128 MB

6.7 Internal ROM Memory

The internal ROM memory is used to store the boot code of the LPC3152/3154. After a reset, the ARM processor will start its code execution from this memory.

The LPC3154 ROM memory has the following features:

- Supports secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports SHA1 hash checking on the boot image.
- Supports un-secure boot from UART and USB (DFU class) interfaces during development. Once the AES key is programmed in the OTP, only secure boot is allowed through UART and USB.
- Supports secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The LPC3152 ROM memory has the following features:

- Supports non-secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Supports non-secure booting from UART and USB (DFU class) interfaces during development.
- Supports non-secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The boot ROM determines the boot mode based on the reset state of the GPIO0, GPIO1, and GPIO2 pins. To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be low during power-on reset, see *UM10315 JTAG chapter* for details.

Table 9 shows the various boot modes supported on the LPC3152/3154. If the boot process fails (e.g. due to tampering with security), the boot code drives pin GPIO3 HIGH. It is recommended to connect the GPIO3 pin to PSU_STOP, so that the LPC3152/3154 will be powered down and further access prevented when the boot ROM detects an error.

Table 9. LPC3152/3154 boot modes

Boot mode	GPIO0	GPIO1	GPIO2	Description
NAND	0	0	0	Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode.
SPI	0	0	1	Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode.
DFU	0	1	0	Device boots via USB using DFU class specification.
SD/MMC	0	1	1	Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode.
Reserved 0	1	0	0	Reserved for testing.
NOR flash	1	0	1	Boot from parallel NOR flash connected to EBI_NSTCS_1.[1]
UART	1	1	0	Boot ROM tries to download boot image from UART ((115200 – 8 – n –1) assuming 12 MHz FFAST clock).
Test	1	1	1	Boot ROM is testing ISRAM using memory pattern test and basic functionality of the analog audio block. Switches to UART boot mode on receiving three ASCI dots ("...") on UART.

[1] For security reasons this mode is disabled when JTAG security feature is used.

6.8 Internal RAM memory

The ISRAM (Internal Static Memory Controller) module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI-flash, NAND flash and SD/MMC cards.

This module has the following features:

- Capacity of 192 kB
- Implemented as two independent 96 kB memory banks

Within most clock domains, the output clocks are again grouped into one or more subdomains. All output clocks within one subdomain are either all generated by the same fractional divider or they are connected directly to the base clock. Therefore all output clocks within one subdomain have the same frequency and all output clocks within one clock domain are synchronous because they originate from the same base clock

The CGU reference clock is generated by the external crystal. Furthermore the CGU has several Phase Locked Loop (PLL) circuits to generate clock signals that can be used for system clocks and/or audio clocks. All clock sources, except the output of the PLLs, can be used as reference input for the PLLs.

This module has the following features:

- Advanced features to optimize the system for low power:
  - All output clocks can be disabled individually for flexible power optimization
  - Some modules have automatic clock gating: they are only active when (bus) access to the module is required.
  - Variable clock scaling for automatic power optimization of the AHB bus (high clock frequency when the bus is active, low clock frequency when the bus is idle).
  - Clock wake-up feature: module clocks can be programmed to be activated automatically on the basis of an event detected by the Event Router (see also Section 6.19). For example, all clocks (including the ARM /bus clocks) are off and activated automatically when a button is pressed.
- Supports three clock sources:
  - Reference clock generated by the oscillator with an external crystal.
  - Pins I2SRX_BCK0, I2SRX_WS0 are used to input external clock signals (used for generating audio frequencies in I^2S receive / I^2S transmit slave mode, see also Section 6.4).
- Two PLLs:
  - System PLL generates programmable system clock frequency from its reference input.
  - Audio PLL generates programmable audio clock frequency (typically 256 $\times$ fs) from its reference input.

    Remark: Both the System PLL and the audio PLL generate their frequencies based on their (individual) reference clocks. The reference clocks can be programmed to the oscillator clock or one of the external clock signals.
- Highly flexible switchbox to distribute the signals from the clock sources to the module clocks.
  - Each clock generated by the CGU is derived from one of the base clocks and optionally divided by a fractional divider.
  - Each base clock can be programmed to have any one of the clock sources as an input clock.
  - Fractional dividers can be used to divide a base clock by a fractional number to a lower clock frequency.
  - Fractional dividers support clock stretching to obtain a (near) 50% duty cycle output clock.
- Register interface to reset all modules under software control.

Table 11. Pin descriptions of multiplexed pins

Pin name	Default signal	Alternate signal	Description
NAND flash related pin multiplexing			
mNAND_RYBN0	NAND_RYBN0	MCI_DAT_4	**NAND_RYBN0 —** NAND flash controller Read/Not busy signal 0. **MCI_DAT_4 —** MCI card data input/output line 4.
mNAND_RYBN1	NAND_RYBN1	MCI_DAT_5	**NAND_RYBN1 —** NAND flash controller Read/Not busy signal 1. **MCI_DAT_5 —** MCI card data input/output line 5.
mNAND_RYBN2	NAND_RYBN2	MCI_DAT_6	**NAND_RYBN2 —** NAND flash controller Read/Not busy signal 2. **MCI_DAT_6 —** MCI card data input/output line 6.
mNAND_RYBN3	NAND_RYBN3	MCI_DAT_7	**NAND_RYBN3 —** NAND flash controller Read/Not busy signal 3. **MCI_DAT_7 —** MCI card data input/output line 7.
Audio related pin multiplexing			
mI2STX_DATA0	I2STX_DATA0	PCM_DA	**I2STX_DATA0 —** I2S interface 0 transmit data signal. **PCM_DA —** PCM serial data line A.
mI2STX_BCK0	I2STX_BCK0	PCM_FSC	**I2STX_BCK0 —** I2S interface 0 transmit bitclock signal. **PCM_FSC —** PCM frame synchronization signal.
mI2STX_WS0	I2STX_WS0	PCM_DCLK	**I2STX_WS0 —** I2S interface 0 transmit word select signal. **PCM_DCLK —** PCM data clock output.
mI2STX_CLK0	I2STX_CLK0	PCM_DB	**I2STX_CLK0 —** I2S interface 0 transmit clock signal. **PCM_DB —** PCM serial data line B.
UART related pin multiplexing			
mUART_CTS_N	UART_CTS_N	SPI_CS_OUT1	**UART_CTS_N —** UART modem control Clear-to-Send signal. **SPI_CS_OUT1 —** SPI chip select out for slave 1 (used in master mode).
mUART_RTS_N	UART_RTS_N	SPI_CS_OUT2	**UART_RTS_N —** UART modem control Request-to-Send signal. **SPI_CS_OUT2 —** SPI chip select out for slave 2 (used in master mode).

6.28.2 Multiplexing between LCD and MPMC

The multiplexing between the LCD interface and MPMC allows for the following two modes of operation:

- MPMC-mode: SDRAM and bus-based LCD or SRAM.
- LCD-mode: Dedicated LCD-Interface.

The external NAND flash is accessible in both modes.

The block diagram Figure 9 gives a high level overview of the modules in the chip that are involved in the pin interface multiplexing between the EBI, NAND flash controller, MPMC, and RAM-based LCD interface.

The $I^2S0/1$ module has the following features:

- Receive input supports master mode and slave mode.
- Transmit output supports master mode.
- Supports LSB justified words of 16, 18, 20 and 24 bits.
- Supports a configurable number of bit clock periods per word select period (up to 128 bit clock periods).
- Supports DMA transfers.
- Transmit FIFO or receive FIFO of 4 stereo samples.
- Supports single 16-bit transfers to/from the left or right FIFO.
- Supports single 24-bit transfers to/from the left or right FIFO.
- Supports 32-bit interleaved transfers, with the lower 16 bits representing the left audio sample and the higher 16 bits representing the right audio sample.
- Supports two 16-bit samples audio samples combined in a 32-bit word (2 left or 2 right samples) to reduce bus load.
- Provides maskable interrupts for audio status.
(FIFO underrun/overrun/full/half_full/not empty for left and right channel separately).

7. Functional description of the analog die blocks

7.1 Analog die

The analog die part of the LPC3152/3154 contains the audio codec, the Real-Time Clock (RTC), the Power Supply Unit (PSU), the Li-ion charger, and the USB charge pump.

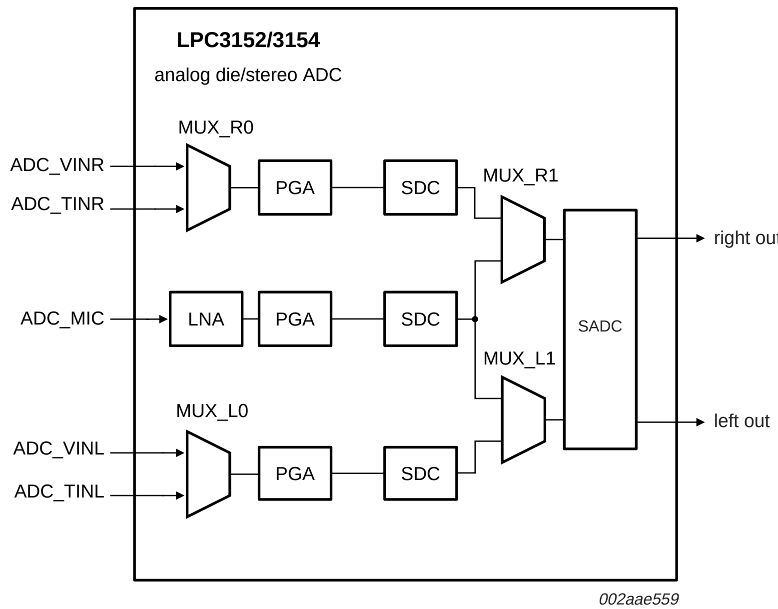


Fig 12. Stereo ADC for audio

This module has the following features:

- Three input options: line-in (stereo), tuner-in (stereo), microphone-in (mono).
- Low-Noise Amplifier (LNA) with a fixed 30 dB gain for the microphone input.
- Programmable Gain Amplifier (PGA). Gain can be set in steps of 3 dB up to 24 dB.
- Single-to-Differential Converter (SDC).
- SADC (switched cap).
- Supported audio sample frequencies are 8 kHz to 55 kHz.
- Oversampling rate 128 times the sample frequency.
- High dynamic range.
- Digital dB-linear volume control in 0.5 dB steps.
- DC blocking filter (optional).
- Soft start-up.
- Mute and overflow detection.

7.3 Li-ion charger

The built-in charger allows a Li-ion battery to be charged from the power supplied by a USB connection or by an AC adapter.

This module has the following features:

- Monitors for battery voltage, charge current, battery temperature feedback (NTC), and chip temperature (programmable temperature limits).
- Maximum charge current 250 mA.

Table 13: Static characteristics

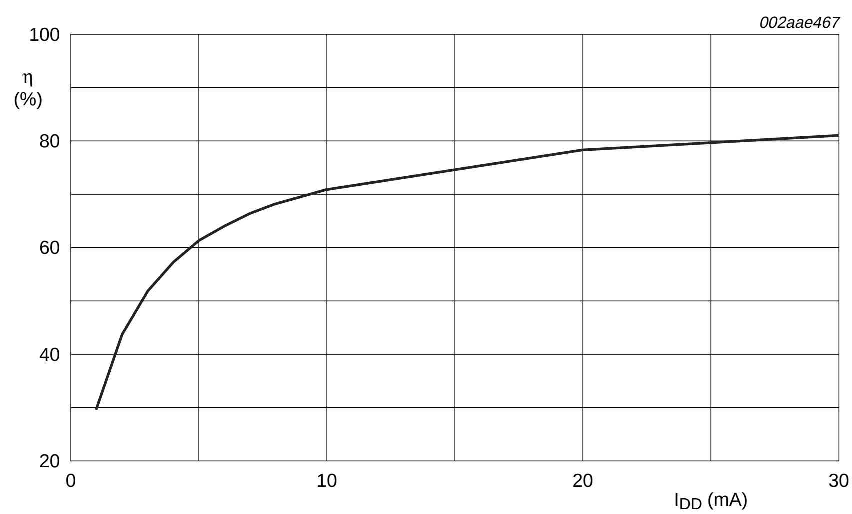
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		SUP4; SUP8; 3.3 V mode	[1]	<tbd>	50	<tbd>	µA
		SUP3	[1]	<tbd>	50	<tbd>	µA
C_i	input capacitance	excluding bonding pad capacitance		-	-	<tbd>	pF
Output pins and I/O pins configured as output							
V_O	output voltage			<tbd>	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	SUP4; SUP8; I_{OH} = 6 mA:					
		1.8 V mode		<tbd>	<tbd>	<tbd>	V
		3.3 V mode		$V_{DD(IO)}$ − 0.26	<tbd>	<tbd>	V
		SUP3; I_{OH} = 6 mA		$V_{DD(IO)}$ − 0.26	-	-	V
		SUP3; I_{OH} = 30 mA		$V_{DD(IO)}$ − 0.38	-	-	V
V_{OL}	LOW-level output voltage	SUP4; SUP8 outputs; I_{OL} = 4 mA					
		1.8 V mode		<tbd>	<tbd>	<tbd>	V
		3.3 V mode	[1]	<tbd>	0.65	<tbd>	V
		SUP3; I_{OL} = 4 mA		-	-	<tbd>	V
I_{OH}	HIGH-level output current	V_{DD} = VDDE_IOx (x = A, B, C); V_{OH} = V_{DD} − 0.4 V		<tbd>	-	-	mA
		V_{DD} = VDDE_IOx (x = A, B, C); V_{OH} = V_{DD} − 0.4 V		<tbd>	-	-	mA
I_{OL}	LOW-level output current	V_{DD} = VDDE_IOx (x = A, B, C); V_{OL} = 0.4 V		<tbd>	-	-	mA
		V_{DD} = VDDE_IOx (x = A, B, C); V_{OL} = 0.4 V		<tbd>	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down		-	-	0.064	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = VDDE_IOx (x = A, B, C); V_{OH} = 0 V		-	-	<tbd>	mA
		V_{DD} = VDDE_IOx (x = A, B, C); V_{OH} = 0 V		-	-	<tbd>	mA
I_{OLS}	LOW-level short-circuit output current	V_{DD} = VDDE_IOx (x = A, B, C); V_{OL} = V_{DD}		-	-	<tbd>	mA
		V_{DD} = VDDE_IOx (x = A, B, C); V_{OL} = V_{DD}		-	-	<tbd>	mA
Z_o	output impedance	V_{DD} = VDDE_IOx (x = A, B, C)					
		1.8 V mode	[1]	<tbd>	45	<tbd>	Ω
		3.3 V mode	[1]	<tbd>	35	<tbd>	Ω

Table 18. Efficiency of output on PSU_VOUT1 (PSU_VOUT1 programmed to 2.86 V)

I_{BAT} / mA on pin PSU_VBAT	V_{BAT} / V	I_{DD} / mA (SUP3)	V_{DD} / V (SUP4)	Efficiency / %
2	3.602	1	2.8676	39.80566352
2.8	3.6016	2	2.864	56.80015231
3.598	-	3	2.8605	66.22816876
4.396	3.601	4	2.8569	72.18953182
5.195	3.6006	5	2.8533	76.27057345
5.994	3.6003	6	2.8498	79.23374865
6.793	3.5999	7	2.8462	81.47256753
7.59	3.5995	8	2.8426	83.23802841
8.388	3.5992	9	2.83991	84.63671469
9.231	3.5988	10	2.8542	85.9167695
13.32	3.597	15	2.8549	89.37941277
17.368	3.595	20	2.837	90.87420537
25.59	3.591	30	2.8198	92.056375145

9.2.1.2 PSU_VOUT2 efficiency



SUP1 = 1.07 V.

SUP2: V_{DD} = 1.398 V, I_{DD} = 0 mA.

SUP3: V_{DD} = 2.912 V, I_{DD} = 0 mA.

PSU_VOUT2 = 1.07 V.

Fig 17. Efficiency PSU_VOUT2

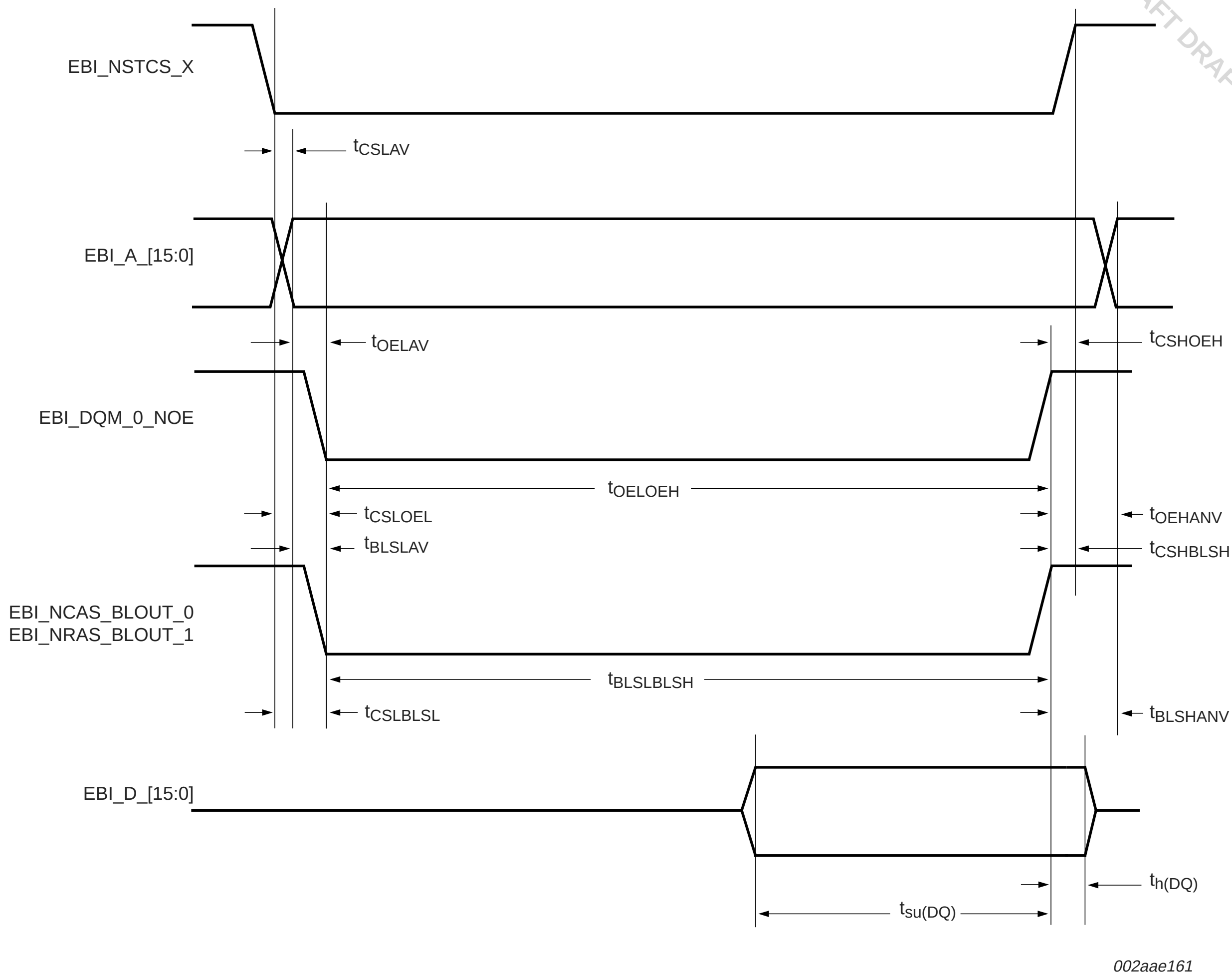


Fig 21. External memory read access to static memory

10.2.1 Crystal oscillator

Table 27: Dynamic characteristics: crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency		10	12	25	MHz
δ_{clk}	clock duty cycle		45	50	55	%
C_{xtal}	crystal capacitance	input; on pin FFAST_IN	-	-	2	pF
		output; on pin FFAST_OUT	-	-	0.74	pF
$t_{startup}$	start-up time		-	500	-	µs
P_{drive}	drive power		100	-	500	µW

10.2.2 SPI

Table 28. Dynamic characteristics of SPI pins
T_{amb} = −40 °C to +85 °C for industrial applications

Symbol	Parameter	Min	Typ	Max	Unit
SPI master					
T_{SPICYC}	SPI cycle time	22.2	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	11.09	-	11.14	ns
$t_{SPICLKL}$	SPICLK LOW time	11.09	-	11.14	ns
t_{SPIDSU}	SPI data set-up time	<tbd>	<tbd>	<tbd>	ns
t_{SPIDH}	SPI data hold time	<tbd>	<tbd>	<tbd>	ns
t_{SPIQV}	SPI data output valid time	-	-	14	ns
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns
SPI slave					
T_{SPICYC}	SPI cycle time	<tbd>	40	<tbd>	ns
$t_{SPICLKH}$	SPICLK HIGH time	<tbd>	20	<tbd>	ns
$t_{SPICLKL}$	SPICLK LOW time	<tbd>	20	<tbd>	ns
t_{SPIDSU}	SPI data set-up time	<tbd>	<tbd>	<tbd>	ns
t_{SPIDH}	SPI data hold time	<tbd>	<tbd>	<tbd>	ns
t_{SPIQV}	SPI data output valid time	<tbd>	<tbd>	14	ns
t_{SPIOH}	SPI output data hold time	9.9	-	-	ns

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagrams.

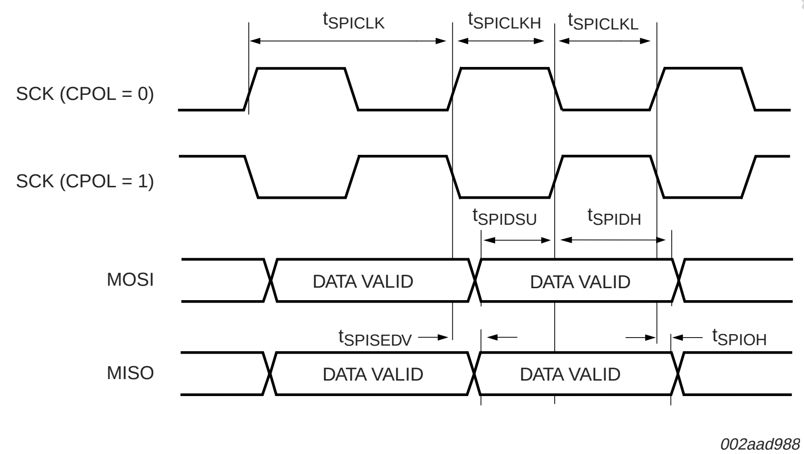


Fig 28. SPI slave timing (CPHA = 1)

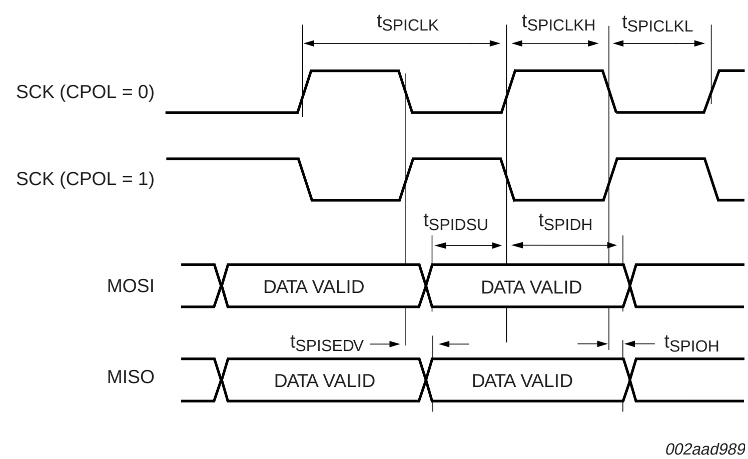


Fig 29. SPI slave timing (CPHA = 0)

10.2.2.1 Texas Instruments synchronous serial mode (SSP mode)

Table 29. Dynamic characteristic: SPI interface (SSP mode)
T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ (SUP3) over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 30	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagram.

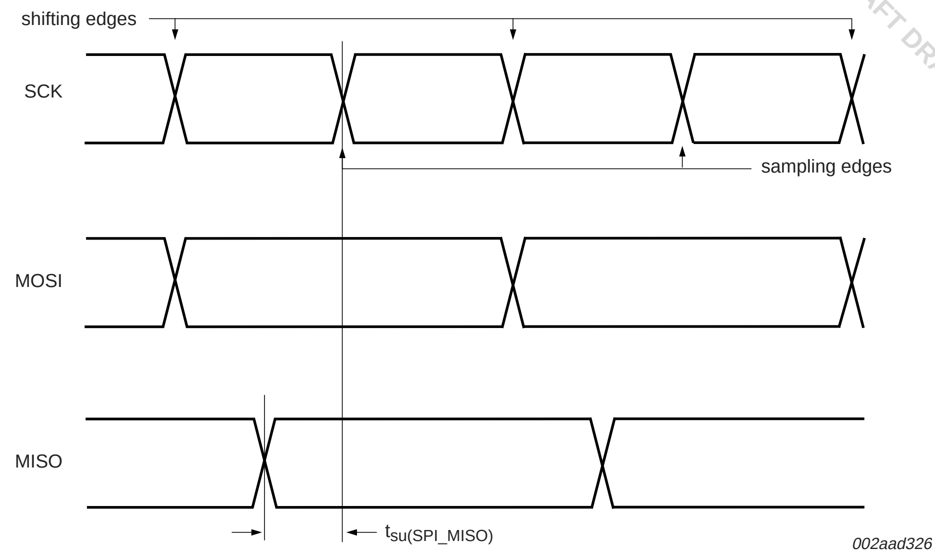


Fig 30. MISO line set-up time in SSP Master mode

10.2.3 I²S-interface

Table 30. Dynamic characteristics: I²S-interface pins
T_{amb} = −40 °C to +85 °C for industrial applications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
common to input and output						
$T_{cy(clk)}$	clock cycle time		<tbd>	<tbd>	<tbd>	ns
t_f	fall time		3.5	<tbd>	<tbd>	ns
t_r	rise time		3.5	<tbd>	<tbd>	ns
output						
t_{WH}	pulse width HIGH		<tbd>	<tbd>	<tbd>	ns
t_{WL}	pulse width LOW		<tbd>	<tbd>	<tbd>	ns
$t_{v(Q)}$	data output valid time	on pin I2STX_DATAx[1]	<tbd>	<tbd>	<tbd>	ns
		on pin I2STX_WSx[1]	<tbd>	<tbd>	<tbd>	ns
input						
$t_{su(D)}$	data input set-up time	on pin I2SRX_DATAx[1]	<tbd>	<tbd>	<tbd>	ns
		on pin I2SRX_WSx[1]	<tbd>	<tbd>	<tbd>	ns
$t_{h(D)}$	data input hold time	on pin I2SRX_DATAx[1]	<tbd>	<tbd>	<tbd>	ns
		on pin I2SRX_WSx[1]	<tbd>	<tbd>	<tbd>	ns

[1] x = 0 or 1.

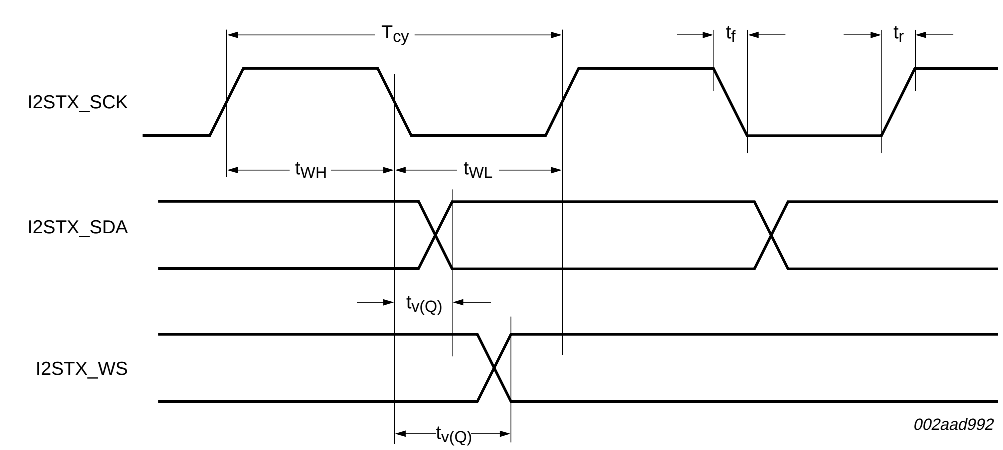


Fig 31. I²S-bus timing (output)

10.3 Analog die/audio system

Table 34. Dynamic characteristics of Class AB amplifier
T_{amb} = –40 °C to +85 °C unless otherwise specified. $V_{DD(ADC)}$ = 3.3 V on pin ADC_VDDA33.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_o	output voltage	HP unloaded		-	800	-	mV(RMS)
P_o	output power	per channel; RL=16 Ω				23.5	mW
(THD+N)/S	Total harmonic distortion plus noise-to-signal ratio	at 0 dBFS; f_{in} = 1 kHz; RL=16 Ω	[1]	-	–60	-	dB
		at –60 dBFS; f_{in} = 1 kHz; RL=16 Ω		-	–40	–30	dBA
S/N	Signal-to-noise ratio		[1]	-	100	-	dBA
PSRR	power supply ripple rejection			-	6	-	dB
$\alpha_{ct(ch)}$	channel crosstalk	RL=16 Ω; between left channel and right channel		-	–55	-	dB

[1] Measured with 20 kHz block filter.

Table 35: Dynamic characteristic for analog in
T_{amb} = –40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B	Bandwidth		-	-	20	kHz
Tuner						
(THD+N)/S	Total harmonic distortion plus noise-to-signal ratio	at 0 dBFS; f_{in} = 1 kHz; Line input level = 1 V; PGA setting +12 dB; external resistor of 36 kΩ	-	–83	–80	dB
		at 0 dBFS; f_{in} = 1 kHz; Line input level = 1 V, PGA setting 0 dB	-	-70	-	dB
		at –60 dBFS; A-weighted; f_{in} = 1 kHz; Line input level = 1mV, PGA setting 0dB	-	–34	–30	dBA
S/N	Signal-to-noise ratio	A-weighted; line input = 1 V, PGA setting 0 dB	90	94	-	dBA
Z_i	input impedance	line in (tuner mode)	-	12	-	kΩ
Microphone						
THD	total harmonic distortion	V_i = 20 mV; f_{in} = 1 kHz	-	–70	–60	dB
		V_i = 0.3 mV; f_{in} = 1 kHz	-	–90	–80	dB
Z_i	input impedance	microphone mode	-	5	-	kΩ

Table 38: Abbreviations *…continued*

Acronym	Description
Timer	Timer module
UART	Universal Asynchronous Receiver Transmitter
USB 2.0 HS OTG	Universal Serial Bus 2.0 High-Speed On-The-Go

16. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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