Microchip Technology - A3P1000-1FG144M Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg144m

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based military ProASIC3/EL devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The military ProASIC3/EL family device architecture mitigates the need for ASIC migration at higher volumes. This makes the military ProASIC3/EL family a cost-effective ASIC replacement.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of military ProASIC3/EL flash-based FPGAs. Once it is programmed, the flash cell configuration element of military ProASIC3/EL FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The military ProASIC3/EL family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary military ProASIC3/EL architecture provides granularity comparable to standard-cell ASICs. The military ProASIC3/EL device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the military ProASIC3/EL core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Very Thin Quad Flat Pack (VQ100)	A3P250	100	10.0	35.3	29.4	27.1	C/W
Plastic Quad Flat Pack (PQ208)*	A3P1000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	A3P1000	144	6.3	31.6	26.2	24.2	C/W
	A3P1000	256	6.6	28.1	24.4	22.7	C/W
	A3P1000	484	8.0	23.3	19.0	16.7	C/W
	A3PE600L	484	9.5	27.5	21.9	20.2	C/W
	A3PE3000L	484	4.7	20.6	15.7	14.0	C/W
	A3PE3000L	896	2.4	13.6	10.4	9.4	C/W

* *Embedded heatspreader*

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, VCC = 1.14 V) Applicable to A3PE600L and A3PE3000L Only**

	Junction Temperature						
Array Voltage VCC (V)	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.14	0.85	0.86	0.89	0.92	0.96	0.97	1.00
1.2	0.82	0.83	0.86	0.88	0.92	0.93	0.96
1.26	0.79	0.80	0.83	0.85	0.89	0.90	0.93
1.30	0.77	0.78	0.81	0.83	0.86	0.88	0.90
1.35	0.74	0.75	0.78	0.80	0.84	0.85	0.88
1.40	0.72	0.73	0.75	0.77	0.81	0.82	0.85
1.425	0.71	0.71	0.74	0.76	0.79	0.80	0.83
1.5	0.67	0.68	0.70	0.72	0.75	0.76	0.79
1.575	0.65	0.66	0.68	0.70	0.73	0.74	0.76

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, VCC = 1.425 V) Applicable to A3P250 and A3P1000 Devices Only**

	Junction Temperature						
Array Voltage VCC (V)	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.425	0.80	0.82	0.87	0.89	0.94	0.96	1.00
1.5	0.76	0.78	0.82	0.84	0.89	0.91	0.95
1.575	0.73	0.75	0.79	0.82	0.86	0.87	0.91

Table 2-18 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only**

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) [2]	Dynamic Power PAC10 (µW/MHz) [3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	141.97
3.3 V LVCMOS Wide Range	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.82
LVPECL	–	3.3	19.54	167.55

Notes:

1. *Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Table 2-19 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only**

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) [2]	Dynamic Power PAC10 (µW/MHz) [3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	125.97
3.3 V LVCMOS – Wide Range	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Table 2-28 • Summary of Maximum and Minimum DC Input Levels Applicable to Military Conditions

DC I/O Standard	Military[1]	
	I_{IL}[2]	I_{IH}[3]
	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	15	15
3.3 V LVCMOS Wide Range	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS[4]	15	15
1.2 V LVCMOS Wide Range[4]	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1. *Military temperature range: –55°C to 125°C.*
2. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Applicable to Military A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.*

Table 2-48 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

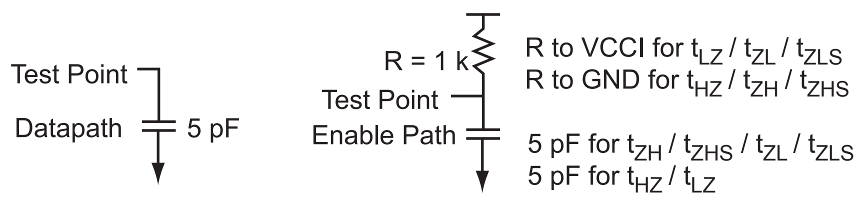

Figure 2-7 • **AC Loading**

Table 2-49 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

Note: **Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Table 2-60 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	103	109	15	15
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	132	127	15	15

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 125°C junction temperature.*
5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.*
6. *Software default selection highlighted in gray.*

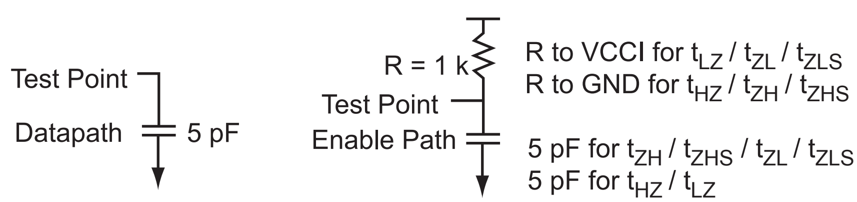

Figure 2-8 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-82 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	35	44	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	45	51	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	91	74	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	91	74	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-83 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	45	51	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	91	74	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	91	74	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-92 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	–1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	–1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-93 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	–1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	–1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS Wide Range

***Table 2-110* • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Operating at 1.2 V Core Voltage**

1.2 V LVCMOS Wide Range[1]	Equiv. Software Default Drive Strength Option[2]	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}[3]	I_{IH}[4]
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[5]	Max. mA[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	TBD	TBD	15	15

Notes:

1. *Applicable to A3PE600L and A3PE3000L devices only.*
2. *Note that 1.2 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
3. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
5. *Currents are measured at 100°C junction temperature and maximum voltage.*
6. *Currents are measured at 125°C junction temperature.*
7. *Software default selection highlighted in gray.*

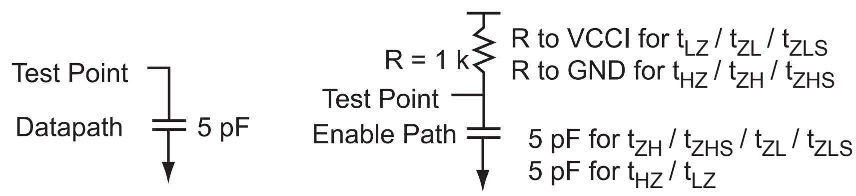

***Figure 2-13* • AC Loading**

***Table 2-111* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.2	0.6	–	5

Note: **Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Table 2-123 • 3.3 V GTL
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 0.8 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.97	0.04	2.11	0.40	1.86	1.97	–	–	3.32	3.43	ns
–1	0.52	1.68	0.03	1.79	0.34	1.58	1.68	–	–	2.83	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-140* • Minimum and Maximum DC Input and Output Levels**

HSTL Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA [3]**	**Max. mA [3]**	**µA [4]**	**µA [4]**
15 mA [5]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	66	55	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

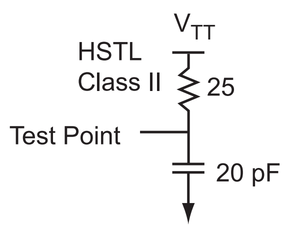

***Figure 2-20* • AC Loading**

***Table 2-141* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

***Table 2-142* • HSTL Class II**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	3.00	0.05	2.76	0.52	3.05	2.69	–	–	5.25	4.89	ns
–1	0.68	2.55	0.05	2.34	0.44	2.59	2.28	–	–	4.47	4.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-143* • HSTL Class II**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.86	0.04	2.52	0.40	2.89	2.57	–	–	4.36	4.04	ns
–1	0.52	2.44	0.03	2.14	0.34	2.46	2.19	–	–	3.71	3.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-144* • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	83	87	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

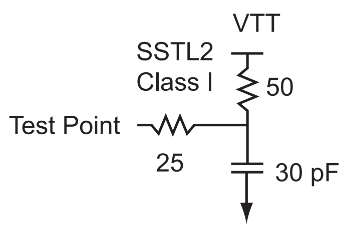

***Figure 2-21* • AC Loading**

***Table 2-145* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

***Table 2-146* • SSTL2 Class I**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.11	0.05	2.09	0.52	2.14	1.83	–	–	2.14	1.83	ns
–1	0.68	1.80	0.05	1.78	0.44	1.82	1.55	–	–	1.82	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-160 **• Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0	–	2.925	V
IIH [2,3]	Input High Leakage Current	–	–	10	µA
IIL [2,4]	Input Low Leakage Current	–	–	10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350	–	mV

Notes:

1. *IOL/IOH is defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 125°C junction temperature.*
3. *IIH is the input leakage current per IO pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

Table 2-161 **• AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = $V_{trip.}$ See Table 2-29 on page 2-25 for a complete table of trip points.*

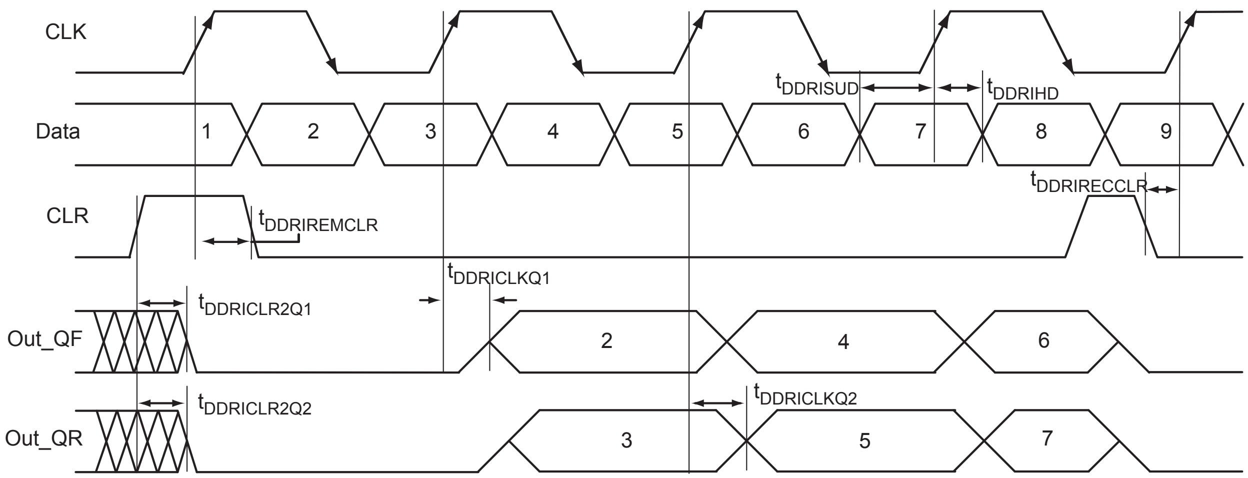

***Figure 2-34* • Input DDR Timing Diagram**

Timing Characteristics

***Table 2-182* • Input DDR Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.38	0.45	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.54	0.63	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.39	0.46	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.34	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.64	0.75	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.79	0.93	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.31	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160	160	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

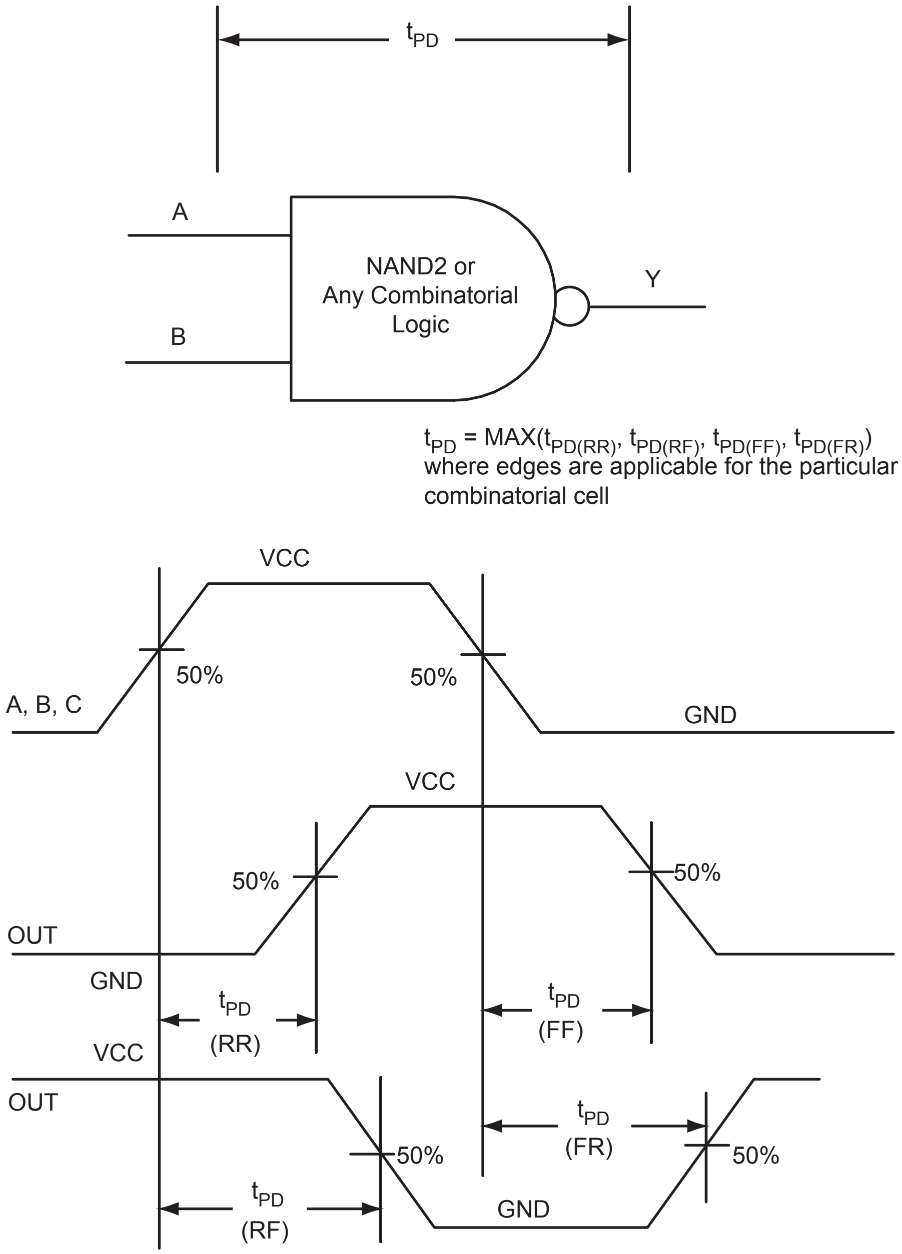

Figure 2-38 • **Timing Model and Waveforms**

Table 2-199 **• A3P250 Global Resource**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.97	1.24	1.14	1.46	ns
t_{RCKH}	Input High Delay for Global Clock	0.94	1.27	1.11	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.32		0.38	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-200 **• A3P1000 Global Resource**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.18	1.44	1.39	1.70	ns
t_{RCKH}	Input High Delay for Global Clock	1.17	1.48	1.37	1.74	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.32		0.37	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-201* • Military ProASIC3/EL CCC/PLL Specification**
For Devices Operating at 1.2 V DC Core Voltage: Applicable to A3PE600L and A3PE3000L Only

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2.3]		360		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4]			100	MHz
Input cycle-to-cycle jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			25	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1,2]	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 [1,2]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1,2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max. Peak-to-Peak Period Jitter[6,7]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.60%
50 MHz to 160 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.2 V.*
3. *When the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero online help associated with the core for more information.*
4. *Maximum value obtained for a –1 speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
6. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14V, VQ/PQ/TQ type of packages, 20 pF load.*
7. *Switching I/Os are placed outside of the PLL bank.*

Embedded FlashROM Characteristics

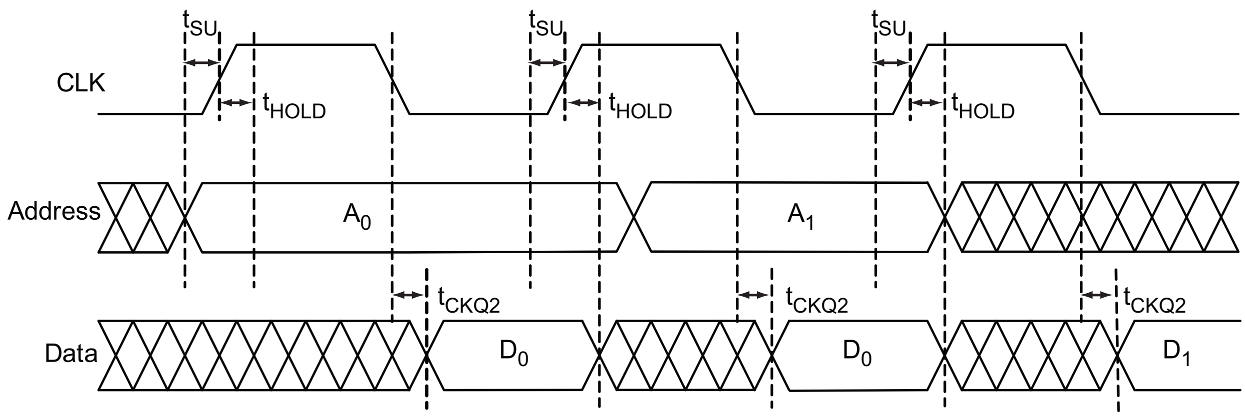

Figure 2-55 • Timing Diagram

Timing Characteristics

Table 2-217 **• Embedded FlashROM Access Time Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L**

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.74	0.87	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.18	19.02	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-218 **• Embedded FlashROM Access Time Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L**

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.58	0.68	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	12.77	15.01	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-219 **• Embedded FlashROM Access Time Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000**

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.64	0.75	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	19.54	22.97	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

FG484	
Pin Number	A3PE600L Function
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	VCC
Y9	VCC
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC
AA15	NC

FG484	
Pin Number	A3PE600L Function
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND

FG896	
Pin Number	A3PE3000L Function
W20	VCC
W21	VCCIB3
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	VCC
Y12	VCC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VCC
Y19	VCC
Y20	VCC
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3