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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fgg144m

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • Power Supply State Per Mode

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
Static and Active	On	On	On	On	On/off/floating

Table 2-9 • Quiescent Supply Current (IDD) Characteristics, Flash*Freeze Mode*

	Core Voltage	A3PE600L	A3PE3000L	Units
Nominal (25°C)	1.2 V	0.55	2.75	mA
	1.5 V	0.83	4.2	mA
Typical maximum (25°C)	1.2 V	9	17	mA
	1.5 V	12	20	mA
Military maximum (125°C)	1.2 V	65	165	mA
	1.5 V	85	185	mA

Note: * IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Values do not include I/O static contribution (PDC6 and PDC7).

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, Sleep Mode (VCC = 0 V)*

	Core Voltage	A3PE600L	A3PE3000L	Units
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Note: * $IDD = N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in Table 2-22 on page 2-14 (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, Shutdown Mode*

	Core Voltage	A3P250	A3P1000	A3PE600L	A3PE3000L	Units
Nominal (25°C)	1.2 V / 1.5 V	N/A		0		µA
Military (125°C)	1.2 V / 1.5 V	N/A		0		µA

Note: *This is applicable to A3PE600L and A3PE3000L only for cold-sparable I/O devices. Not available on A3P250 or A3P1000.

Power per I/O Pin

**Table 2-14 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μ W/MHz) ²
Single-Ended			
3.3 V LVTT/LVCMOS	3.3	–	16.34
3.3 V LVTT/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range	3.3	–	16.34
3.3 V LVCMOS – Schmitt trigger Wide Range	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger	1.2	–	0.53
1.2 V LVCMOS Wide Range	1.2	–	0.60
1.2 V LVCMOS Schmitt trigger Wide Range	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	0.79
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. PDC6 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCCI.

Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings–1 Speed Grade, Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst Case VCC = 1.425 V,

Worst Case VCCI

Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZL_S} (ns)	t_{ZH_S} (ns)
3.3 V LVTTL / 3.3 V LVC MOS	12 mA	12 mA	High	5	–	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56
3.3 V LVC MOS Wide Range ³	100 μ A	12 mA	High	5	–	0.54	2.94	0.04	1.42	0.39	2.94	2.22	4.03	4.66	6.12	5.40
2.5 V LVC MOS	12 mA	12 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.8 V LVC MOS	8 mA	8 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.5 V LVC MOS	4 mA	4 mA	High	5	–	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32
3.3 V PCI	Per PCI spec.	–	High	10	25 ⁴	0.54	2.16	0.04	0.80	0.39	2.20	1.60	2.61	3.01	4.29	3.69
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25 ⁴	0.54	2.16	0.04	0.78	0.39	2.20	1.60	2.61	3.01	4.29	3.69

Notes:

1. Note that 3.3 V LVC MOS wide range is applicable to 100 μ A drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software. Software default load is higher.
3. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Detailed I/O DC Characteristics

Table 2-35 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF

1.5 V DC Core Voltage
Table 2-52 • 3.3 V LVTTL / 3.3 V LVC MOS Low Slew

 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $VCC = 1.425 \text{ V}$, Worst-Case $VCCI = 3.0 \text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	5.90	0.04	1.45	2.09	0.40	5.98	4.73	2.52	2.24	7.45	6.19	ns
	-1	0.52	5.02	0.03	1.23	1.78	0.34	5.09	4.02	2.15	1.90	6.34	5.27	ns
8 mA	Std.	0.61	4.80	0.04	1.45	2.09	0.40	4.86	4.02	2.87	2.85	6.32	5.49	ns
	-1	0.52	4.08	0.03	1.23	1.78	0.34	4.13	3.42	2.44	2.43	5.38	4.67	ns
12 mA	Std.	0.61	4.02	0.04	1.45	2.09	0.40	4.06	3.49	3.09	3.23	5.53	4.96	ns
	-1	0.52	3.42	0.03	1.23	1.78	0.34	3.46	2.97	2.63	2.75	4.70	4.22	ns
16 mA	Std.	0.61	3.79	0.04	1.45	2.09	0.40	3.84	3.38	3.14	3.34	5.30	4.84	ns
	-1	0.52	3.23	0.03	1.23	1.78	0.34	3.26	2.87	2.67	2.84	4.51	4.12	ns
24 mA	Std.	0.61	3.67	0.04	1.45	2.09	0.40	3.72	3.39	3.20	3.74	5.18	4.86	ns
	-1	0.52	3.13	0.03	1.23	1.78	0.34	3.16	2.88	2.72	3.18	4.41	4.13	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-53 • 3.3 V LVTTL / 3.3 V LVC MOS High Slew

 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $VCC = 1.425 \text{ V}$, Worst-Case $VCCI = 3.0 \text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	3.26	0.04	1.45	2.09	0.40	3.30	2.48	2.52	2.38	4.76	3.95	ns
	-1	0.52	2.77	0.03	1.23	1.78	0.34	2.80	2.11	2.15	2.03	4.05	3.36	ns
8 mA	Std.	0.61	2.66	0.04	1.45	2.09	0.40	2.68	1.97	2.87	3.00	4.15	3.43	ns
	-1	0.52	2.26	0.03	1.23	1.78	0.34	2.28	1.67	2.44	2.55	3.53	2.92	ns
12 mA	Std.	0.61	2.32	0.04	1.45	2.09	0.40	2.33	1.72	3.09	3.40	3.80	3.18	ns
	-1	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71	ns
16 mA	Std.	0.61	2.26	0.04	1.45	2.09	0.40	2.28	1.67	3.15	3.51	3.74	3.14	ns
	-1	0.52	1.92	0.03	1.23	1.78	0.34	1.94	1.42	2.68	2.98	3.18	2.67	ns
24 mA	Std.	0.61	2.28	0.04	1.45	2.09	0.40	2.30	1.61	3.21	3.90	3.77	3.07	ns
	-1	0.52	1.94	0.03	1.23	1.78	0.34	1.96	1.37	2.73	3.32	3.20	2.61	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-78 • 2.5 V LVC MOS Low Slew

**Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	7.07	0.05	1.44	0.45	7.20	6.32	2.95	2.43	9.66	8.78	ns
	-1	0.54	6.02	0.04	1.23	0.39	6.13	5.38	2.51	2.06	8.22	7.47	ns
6 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	-1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
8 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	-1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
12 mA	Std.	0.63	5.05	0.05	1.44	0.45	5.15	4.79	3.63	3.66	7.61	7.25	ns
	-1	0.54	4.30	0.04	1.23	0.39	4.38	4.07	3.09	3.11	6.47	6.17	ns
16 mA	Std.	0.63	4.78	0.05	1.44	0.45	4.86	4.65	3.70	3.78	7.32	7.10	ns
	-1	0.54	4.06	0.04	1.23	0.39	4.14	3.95	3.14	3.22	6.23	6.04	ns
24 mA	Std.	0.63	4.71	0.05	1.44	0.45	4.73	4.71	3.78	4.26	7.19	7.17	ns
	-1	0.54	4.01	0.04	1.23	0.39	4.03	4.01	3.21	3.62	6.12	6.10	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-79 • 2.5 V LVC MOS High Slew

**Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.63	0.05	1.44	0.45	3.70	3.34	2.94	2.53	6.16	5.80	ns
	-1	0.54	3.09	0.04	1.23	0.39	3.15	2.84	2.51	2.16	5.24	4.94	ns
6 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	-1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
8 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	-1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
12 mA	Std.	0.63	2.65	0.05	1.44	0.45	2.70	2.23	3.63	3.78	5.16	4.69	ns
	-1	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99	ns
16 mA	Std.	0.63	2.59	0.05	1.44	0.45	2.64	2.16	3.70	3.90	5.10	4.62	ns
	-1	0.54	2.21	0.04	1.23	0.39	2.25	1.83	3.15	3.32	4.34	3.93	ns
24 mA	Std.	0.63	2.61	0.05	1.44	0.45	2.66	2.08	3.78	4.40	5.12	4.54	ns
	-1	0.54	2.22	0.04	1.23	0.39	2.26	1.77	3.22	3.74	4.35	3.87	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-80 • 2.5 V LVC MOS Low Slew

**Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	6.45	0.05	1.43	0.45	6.56	5.71	2.48	2.19	9.02	8.17	ns
	-1	0.54	5.48	0.04	1.21	0.39	5.58	4.86	2.11	1.86	7.68	6.95	ns
6 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	-1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
8 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	-1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
12 mA	Std.	0.63	4.48	0.05	1.43	0.45	4.56	4.35	3.11	3.31	7.02	6.81	ns
	-1	0.54	3.81	0.04	1.21	0.39	3.88	3.70	2.65	2.82	5.97	5.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-81 • 2.5 V LVC MOS High Slew

**Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.18	0.05	1.43	0.45	3.23	2.92	2.48	2.28	5.69	5.38	ns
	-1	0.54	2.70	0.04	1.21	0.39	2.75	2.48	2.11	1.94	4.84	4.58	ns
6 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	-1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
8 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	-1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
12 mA	Std.	0.63	2.28	0.05	1.43	0.45	2.32	1.90	3.11	3.42	4.78	4.36	ns
	-1	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.5 V DC Core Voltage
Table 2-88 • 1.8 V LVC MOS Low Slew

 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $VCC = 1.425 \text{ V}$, Worst-Case $VCCI = 1.7 \text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	-1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	-1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	-1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	-1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	-1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	-1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-89 • 1.8 V LVC MOS High Slew

 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $VCC = 1.425 \text{ V}$, Worst-Case $VCCI = 1.7 \text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	-1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	-1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	-1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.61	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	-1	0.52	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	-1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	-1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-96 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVC MOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < \text{VIN} < \text{VIL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $\text{VIH} < \text{VIN} < \text{VCCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

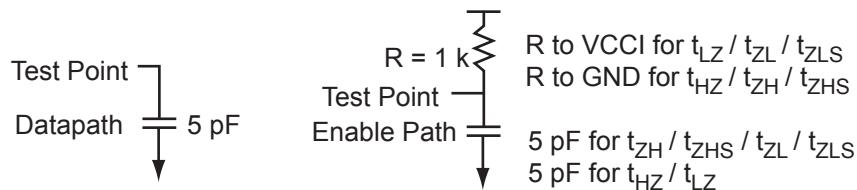


Figure 2-11 • AC Loading

Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C _{LOAD} (pF)
0	1.5	0.75	-	5

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Table 2-102 • 1.5 V LVC MOS Low Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	9.78	0.05	1.44	0.45	9.96	8.57	3.74	2.91	12.42	11.03	ns
	-1	0.54	8.32	0.04	1.23	0.39	8.47	7.29	3.18	2.47	10.56	9.38	ns
4 mA	Std.	0.63	8.44	0.05	1.44	0.45	8.60	7.59	4.12	3.60	11.06	10.05	ns
	-1	0.54	7.18	0.04	1.23	0.39	7.32	6.46	3.51	3.06	9.41	8.55	ns
6 mA	Std.	0.63	7.95	0.05	1.44	0.45	8.10	7.39	4.21	3.78	10.56	9.85	ns
	-1	0.54	6.77	0.04	1.23	0.39	6.89	6.29	3.58	3.21	8.98	8.38	ns
8 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	-1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns
12 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	-1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-103 • 1.5 V LVC MOS High Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.98	0.05	1.58	0.45	4.06	3.80	3.73	3.04	6.52	6.26	ns
	-1	0.54	3.39	0.04	1.35	0.39	3.45	3.23	3.17	2.59	5.54	5.32	ns
4 mA	Std.	0.63	3.47	0.05	1.58	0.45	3.53	3.15	4.11	3.74	5.99	5.61	ns
	-1	0.54	2.95	0.04	1.35	0.39	3.01	2.68	3.50	3.18	5.10	4.77	ns
6 mA	Std.	0.63	3.37	0.05	1.58	0.45	3.43	3.02	4.20	3.92	5.89	5.48	ns
	-1	0.54	2.87	0.04	1.35	0.39	2.92	2.57	3.57	3.33	5.01	4.66	ns
8 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	-1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns
12 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	-1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-123 • 3.3 V GTL

 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425 \text{ V}$,

 Worst-Case $V_{CCI} = 3.0 \text{ V}$, $V_{REF} = 0.8 \text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.97	0.04	2.11	0.40	1.86	1.97	—	—	3.32	3.43	ns
-1	0.52	1.68	0.03	1.79	0.34	1.58	1.68	—	—	2.83	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-132 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
33 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.6	-	33	33	169	124	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3 \text{ V} < \text{VIN} < \text{VIL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $\text{VIH} < \text{VIN} < \text{VCCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.

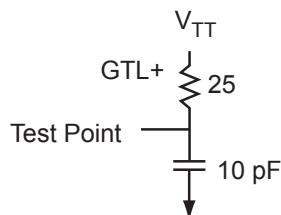


Figure 2-18 • AC Loading

Table 2-133 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-134 • 2.5 V GTL+

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V,

Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.80	2.19	0.05	2.27	0.52	2.22	2.08	—	—	4.43	4.28	ns
-1	0.68	1.86	0.05	1.93	0.44	1.89	1.77	—	—	3.77	3.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-135 • 2.5 V GTL+

Military-Case Conditions: $T_J = 125^\circ\text{C}$, VCC = 1.425 V,

Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.61	2.05	0.04	2.04	0.40	2.07	1.99	—	—	3.53	3.46	ns
-1	0.52	1.75	0.03	1.73	0.34	1.76	1.69	—	—	3.00	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

FIFO

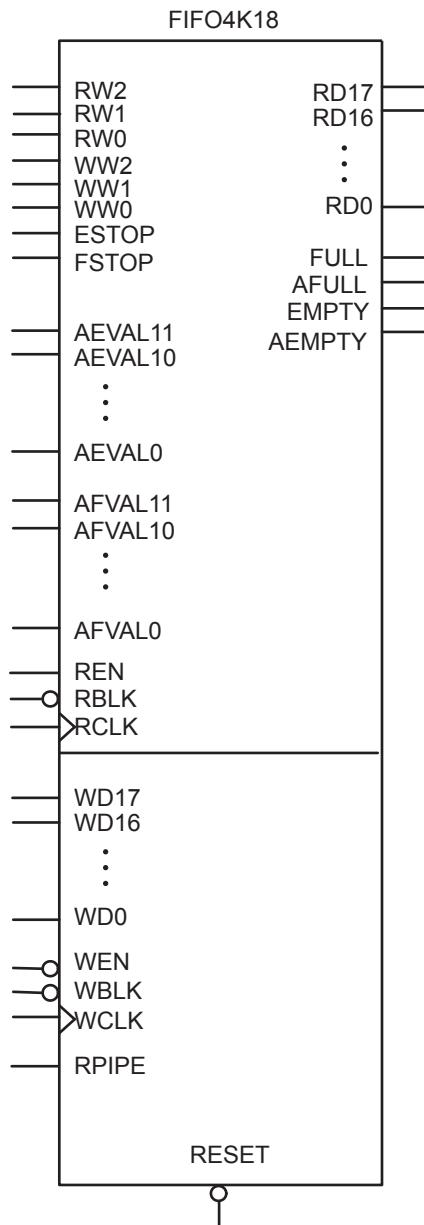


Figure 2-49 • FIFO Model

FG144	
Pin Number	A3P1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484		FG484		FG484	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
E18	GBA2/IO36PDB2V0	G9	IO09NDB0V1	H22	NC
E19	IO42NDB2V0	G10	IO09PDB0V1	J1	IO123NDB7V0
E20	GND	G11	IO13PDB0V2	J2	IO123PDB7V0
E21	NC	G12	IO21PDB1V0	J3	NC
E22	NC	G13	IO25PDB1V0	J4	IO124PDB7V0
F1	NC	G14	IO27NDB1V0	J5	IO125PDB7V0
F2	IO131NDB7V1	G15	GNDQ	J6	IO126PDB7V0
F3	IO131PDB7V1	G16	VCOMPLB	J7	IO130NDB7V1
F4	IO133NDB7V1	G17	GBB2/IO37PDB2V0	J8	VCCIB7
F5	IO134NDB7V1	G18	IO39PDB2V0	J9	GND
F6	VMV7	G19	IO39NDB2V0	J10	VCC
F7	VCCPLA	G20	IO43PDB2V0	J11	VCC
F8	GAC0/IO02NDB0V0	G21	IO43NDB2V0	J12	VCC
F9	GAC1/IO02PDB0V0	G22	NC	J13	VCC
F10	IO15NDB0V2	H1	NC	J14	GND
F11	IO15PDB0V2	H2	NC	J15	VCCIB2
F12	IO20PDB1V0	H3	VCC	J16	IO38NDB2V0
F13	IO25NDB1V0	H4	IO128NDB7V1	J17	IO40NDB2V0
F14	IO27PDB1V0	H5	IO129NDB7V1	J18	IO40PDB2V0
F15	GBC0/IO33NDB1V1	H6	IO132NDB7V1	J19	IO45PDB2V1
F16	VCCPLB	H7	IO130PDB7V1	J20	NC
F17	VMV2	H8	VMV0	J21	IO48PDB2V1
F18	IO36NDB2V0	H9	VCCIB0	J22	IO46PDB2V1
F19	IO42PDB2V0	H10	VCCIB0	K1	IO121NDB7V0
F20	NC	H11	IO13NDB0V2	K2	IO121PDB7V0
F21	NC	H12	IO21NDB1V0	K3	NC
F22	NC	H13	VCCIB1	K4	IO124NDB7V0
G1	IO127NDB7V1	H14	VCCIB1	K5	IO125NDB7V0
G2	IO127PDB7V1	H15	VMV1	K6	IO126NDB7V0
G3	NC	H16	GBC2/IO38PDB2V0	K7	GFC1/IO120PPB7V0
G4	IO128PDB7V1	H17	IO37NDB2V0	K8	VCCIB7
G5	IO129PDB7V1	H18	IO41NDB2V0	K9	VCC
G6	GAC2/IO132PDB7V1	H19	IO41PDB2V0	K10	GND
G7	VCOMPLA	H20	VCC	K11	GND
G8	GNDQ	H21	NC	K12	GND

FG484	
Pin Number	A3PE600L Function
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO50PPB2V1
K17	IO44NDB2V1
K18	IO44PDB2V1
K19	IO49NPB2V1
K20	IO45NDB2V1
K21	IO48NDB2V1
K22	IO46NDB2V1
L1	NC
L2	IO122PDB7V0
L3	IO122NDB7V0
L4	GFB0/IO119NPB7V0
L5	GFA0/IO118NDB6V1
L6	GFB1/IO119PPB7V0
L7	VCOMPLF
L8	GFC0/IO120NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO50NPB2V1
L16	GCB1/IO51PPB2V1
L17	GCA0/IO52NPB3V0
L18	VCOMPLC
L19	GCB0/IO51NPB2V1
L20	IO49PPB2V1
L21	IO47NDB2V1
L22	IO47PDB2V1
M1	NC
M2	IO114NDB6V1
M3	IO117NDB6V1

FG484	
Pin Number	A3PE600L Function
M4	GFA2/IO117PDB6V1
M5	GFA1/IO118PDB6V1
M6	VCCPLF
M7	IO116NDB6V1
M8	GFB2/IO116PDB6V1
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO54PPB3V0
M16	GCA1/IO52PPB3V0
M17	GCC2/IO55PPB3V0
M18	VCCPLC
M19	GCA2/IO53PDB3V0
M20	IO53NDB3V0
M21	IO56PDB3V0
M22	NC
N1	IO114PDB6V1
N2	IO111NDB6V1
N3	NC
N4	GFC2/IO115PDB6V1
N5	IO113PPB6V1
N6	IO112PDB6V1
N7	IO112NDB6V1
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO54NPB3V0

FG484	
Pin Number	A3PE600L Function
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NDB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0

FG484	
Pin Number	A3PE600L Function
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC

FG484	
Pin Number	A3PE600L Function
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0

FG484	
Pin Number	A3PE600L Function
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC

FG484	
Pin Number	A3P1000 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0

FG484	
Pin Number	A3P1000 Function
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND

FG484	
Pin Number	A3P1000 Function
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0

FG484	
Pin Number	A3PE3000L Function
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2
H19	IO100PDB2V2
H20	VCC
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ

FG484	
Pin Number	A3PE3000L Function
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	VCOMPLF
L8	GFC0/IO275NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3

FG484	
Pin Number	A3PE3000L Function
L17	GCA0/IO114NPB3V0
L18	VCOMPLC
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	VCCPLF
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	VCCPLC
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3

FG484	
Pin Number	A3PE3000L Function
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO116NPB3V0
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3

FG484	
Pin Number	A3PE3000L Function
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1

FG484	
Pin Number	A3PE3000L Function
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

Revision	Changes	Page
Revision 5 (September 2014)	Updated FG896 package in the "I/Os Per Package ¹ " table (SAR34171).	I-II
	Removed reference to JTAG interface operated at 3.3 V from "Advanced Architecture" section (SAR 34686).	1-4
	Fixed table note (1) in Table 2-1 (SAR 47815).	2-1
	Deleted ambient temp row and modified notes in Table 2-2 (SAR 59413).	2-2
	Removed "5 V-tolerant input buffer and push-pull output buffer" from "2.5 V LVCMOS" section (SAR 24916).	2-49
	Removed table notes referencing +/-5% and 350mV differential voltage from Table 2-160 (SAR 34810).	2-86
	DDR frequency added to Table 2-182, Table 2-183, Table 2-184, Table 2-186, Table 2-187, Table 2-188 (SAR 56034).	2-105– 2-109
	Table note (3) added to Table 2-201 and Table 2-202 to clarify delay increments (SAR 34821).	2-123
	Terminology clarified in Table 2-203, Table 2-204, Table 2-205, Table 2-206, Table 2-207, Table 2-208, Table 2-209, Table 2-210, Table 2-211, Table 2-212, Table 2-213, Table 2-214, Table 2-215, Table 2-216, Figure 2-44, Figure 2-45, Figure 2-46, Figure 2-47, Figure 2-48, and Figure 2-50 (SAR 38237).	2-129 - 2-145
	Revised statement in "VMVx I/O Supply Voltage (quiet)" section per (SAR 38324).	3-1
Revision 4 (April 2014)	Libero IDE revised to SoC throughout (SAR 40287).	N/A
	Added FG256 under A3P1000 in Table 1 • Military ProASIC3/EL Low-Power Devices, in "I/Os Per Package ¹ ", "Temperature Grade Offerings", "FG256" section, and Table 2-5 • Package Thermal Resistivities (SAR 56384). Added Note for Speed Grade in "Military ProASIC3/EL Ordering Information" section. Also added missing details for FG484 for A3P1000 to Table 2-5 • Package Thermal Resistivities (SAR 56384).	I, III, 2-6 and 4-9
	Added details related to Speed Grade 2 to the "Military ProASIC3/EL Ordering Information" section and the "Speed Grade and Temperature Grade Matrix" section (SAR 56384).	III
Revision 3 (Sept 2012)	Changed Actel references to Microsemi.	NA
	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
Revision 2 (June 2012)	The FG484 package was added for A3P1000 in Table 1 • Military ProASIC3/EL Low-Power Devices, the I/Os Per Package ¹ table, and the "Temperature Grade Offerings" table (SAR 39010).	I, II, III
	The "FG484" pin table for A3P1000 has been added (SAR 39010).	4-19