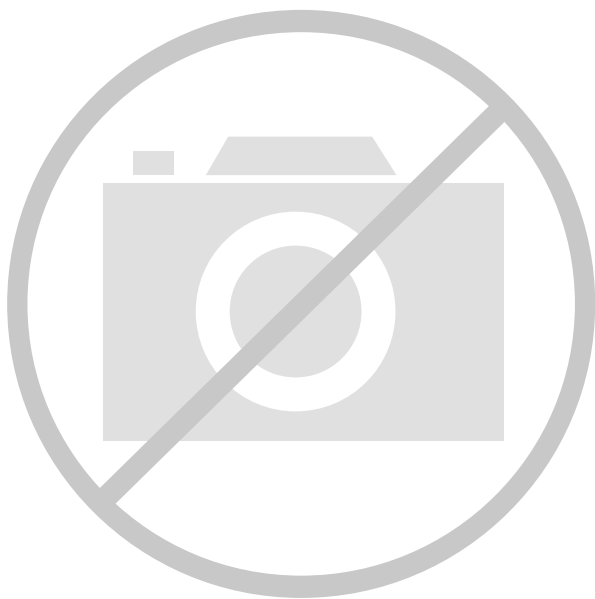




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fgg256m

User Nonvolatile FlashROM

Military ProASIC3/EL devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

FlashROM is written using the standard military ProASIC3/EL IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Microsemi military ProASIC3/EL development software solutions, Libero SoC has extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Military ProASIC3/EL devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Military ProASIC3 devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the military ProASIC3 family contains six CCCs, located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

Military ProASIC3EL devices also contain six CCCs; however, all six are equipped with a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

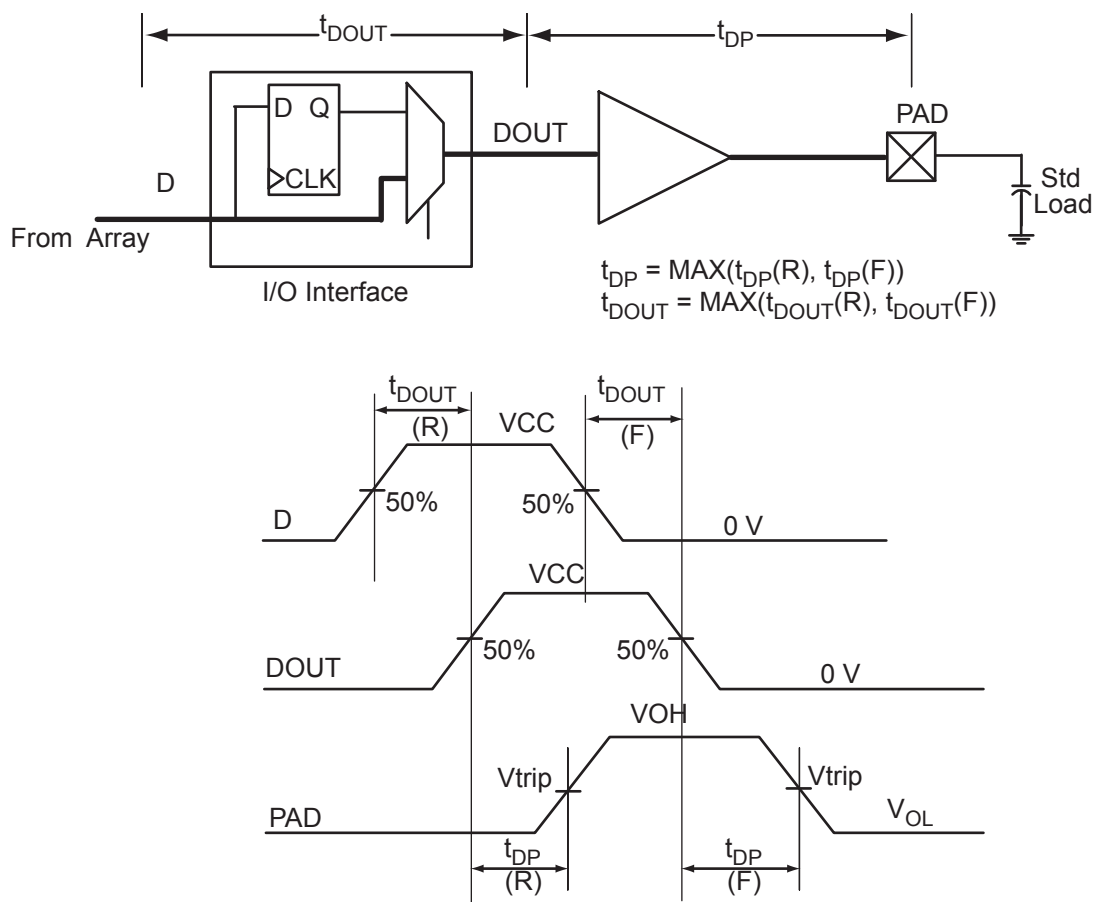


Figure 2-5 • Output Buffer Model and Delays (example)

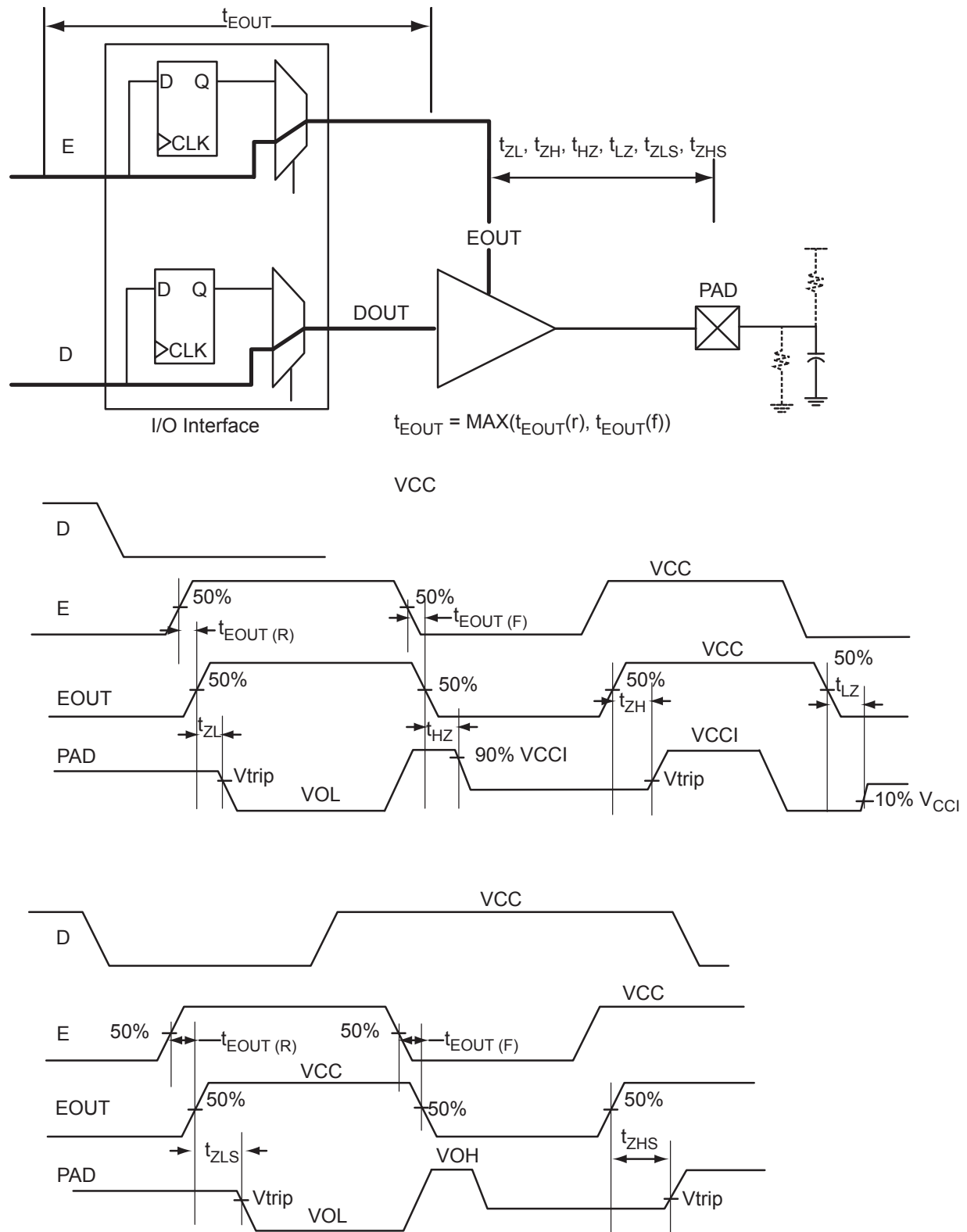


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Military Conditions—Software Default Settings
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	VIL		VIH		VOL	VOH	I _{OL} ²	I _{OH} ²
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ^{1,3}	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS ^{4,5}	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{1,4,5}	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA ⁶	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA ⁶	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA ⁶	15 mA ⁶	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

- Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- Currents are measured at 125°C junction temperature.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
- Applicable to A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Output drive strength is below JEDEC specification.
- Output slew rate can be extracted using the IBIS Models.

**Table 2-28 • Summary of Maximum and Minimum DC Input Levels
Applicable to Military Conditions**

DC I/O Standard	Military ¹	
	I_{IL} ²	I_{IH} ³
	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	15	15
3.3 V LVCMOS Wide Range	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS ⁴	15	15
1.2 V LVCMOS Wide Range ⁴	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1. Military temperature range: $-55^{\circ}C$ to $125^{\circ}C$.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3 V < V_{IN} < V_{IL}$.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. Applicable to Military A3PE600L and A3PE3000L devices operating at $V_{CCI} \geq V_{CC}$.

1.5 V DC Core Voltage

Table 2-64 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.61	8.94	0.04	1.90	2.87	0.40	8.92	7.06	3.69	3.20	10.39	8.53	ns
		–1	0.52	7.61	0.03	1.61	2.44	0.34	7.59	6.01	3.14	2.72	8.84	7.25	ns
100 μA	8 mA	Std.	0.61	7.24	0.04	1.90	2.87	0.40	7.22	5.99	4.23	4.15	8.68	7.45	ns
		–1	0.52	6.16	0.03	1.61	2.44	0.34	6.14	5.10	3.60	3.53	7.39	6.34	ns
100 μA	12 mA	Std.	0.61	6.03	0.04	1.90	2.87	0.40	6.01	5.19	4.58	4.74	7.47	6.65	ns
		–1	0.52	5.13	0.03	1.61	2.44	0.34	5.11	4.41	3.89	4.03	6.36	5.66	ns
100 μA	16 mA	Std.	0.61	5.68	0.04	1.90	2.87	0.40	5.66	5.01	4.65	4.91	7.13	6.47	ns
		–1	0.52	4.83	0.03	1.61	2.44	0.34	4.82	4.26	3.95	4.18	6.06	5.51	ns
100 μA	24 mA	Std.	0.61	5.50	0.04	1.90	2.87	0.40	5.48	5.03	4.74	5.53	6.95	6.49	ns
		–1	0.52	4.68	0.03	1.61	2.44	0.34	4.66	4.28	4.04	4.70	5.91	5.52	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-65 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.61	4.86	0.04	1.90	2.87	0.40	4.84	3.65	3.69	3.43	6.31	5.12	ns
		–1	0.52	4.14	0.03	1.61	2.44	0.34	4.12	3.11	3.14	2.91	5.37	4.35	ns
100 μA	8 mA	Std.	0.61	3.93	0.04	1.90	2.87	0.40	3.91	2.87	4.23	4.38	5.37	4.33	ns
		–1	0.52	3.34	0.03	1.61	2.44	0.34	3.33	2.44	3.60	3.72	4.57	3.68	ns
100 μA	12 mA	Std.	0.61	3.40	0.04	1.90	2.87	0.40	3.38	2.49	4.58	4.99	4.85	3.95	ns
		–1	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36	ns
100 μA	16 mA	Std.	0.61	3.31	0.04	1.90	2.87	0.40	3.29	2.42	4.66	5.16	4.76	3.89	ns
		–1	0.52	2.82	0.03	1.61	2.44	0.34	2.80	2.06	3.96	4.39	4.05	3.31	ns
100 μA	24 mA	Std.	0.61	3.35	0.04	1.90	2.87	0.40	3.33	2.32	4.76	5.78	4.80	3.79	ns
		–1	0.52	2.85	0.03	1.61	2.44	0.34	2.83	1.98	4.05	4.92	4.08	3.22	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-106 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

1.2 V LVCMOS ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ²	IIH ³
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. ⁴ mA	Max. ⁴ mA	μA ⁵	μA ⁵
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	15	15

Notes:

1. Applicable to A3PE600L and A3PE3000L devices only.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 125°C junction temperature.
6. Software default selection highlighted in gray.

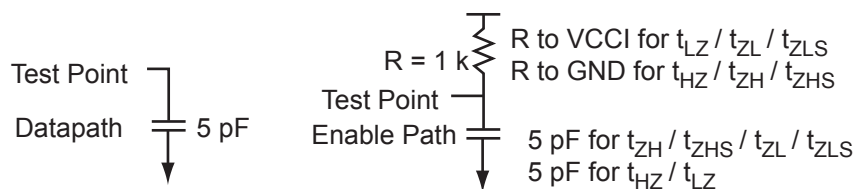


Figure 2-12 • AC Loading

Table 2-107 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C _{LOAD} (pF)
0	1.2	0.6	—	5

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Table 2-147 • SSTL2 Class I

Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$,

Worst-Case $V_{CCI} = 2.3\text{ V}$, $V_{REF} = 1.25\text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.98	0.04	1.85	0.40	1.99	1.71	—	—	1.99	1.71	ns
–1	0.52	1.68	0.03	1.58	0.34	1.69	1.46	—	—	1.69	1.46	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

SSTL2 Class II

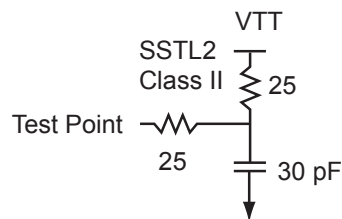
Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-148 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
18 mA	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.35	$V_{CCI} - 0.43$	18	18	169	124	15	15

Notes:

- I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 125°C junction temperature.


Figure 2-22 • AC Loading
Table 2-149 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.2$	$V_{REF} + 0.2$	1.25	1.25	1.25	30

Note: *Measuring point = V_{trip} . See [Table 2-29 on page 2-25](#) for a complete table of trip points.

Timing Characteristics

Table 2-150 • SSTL2 Class II

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,

Worst-Case $V_{CCI} = 2.3\text{ V}$, $V_{REF} = 1.25\text{ V}$

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.15	0.05	2.09	0.52	2.18	1.75	—	—	2.18	1.75	ns
–1	0.68	1.83	0.05	1.78	0.44	1.86	1.49	—	—	1.86	1.49	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-167 • LVPECL

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.80	1.78	0.05	2.16	ns
–1	0.68	1.51	0.05	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.5 V DC Core Voltage

Table 2-168 • LVPECL

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.61	1.65	0.04	1.89	ns
–1	0.52	1.40	0.03	1.61	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-169 • LVPECL

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.98	0.05	1.54	ns
–1	0.54	1.68	0.04	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

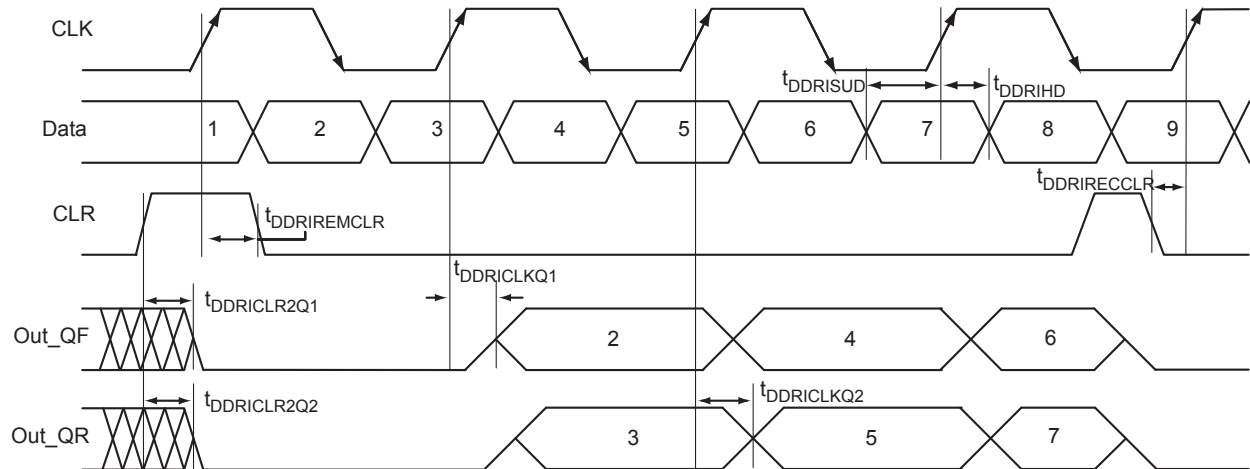


Figure 2-34 • Input DDR Timing Diagram

Timing Characteristics

Table 2-182 • Input DDR Propagation Delays

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.38	0.45	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.54	0.63	ns
t_{DDRISUD1}	Data Setup for Input DDR (fall)	0.39	0.46	ns
t_{DDRISUD2}	Data Setup for Input DDR (rise)	0.34	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (fall)	0.00	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.64	0.75	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.79	0.93	ns
t_{DDRIMCLR}	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.31	0.36	ns
t_{DDRWCCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	160	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Output DDR Module

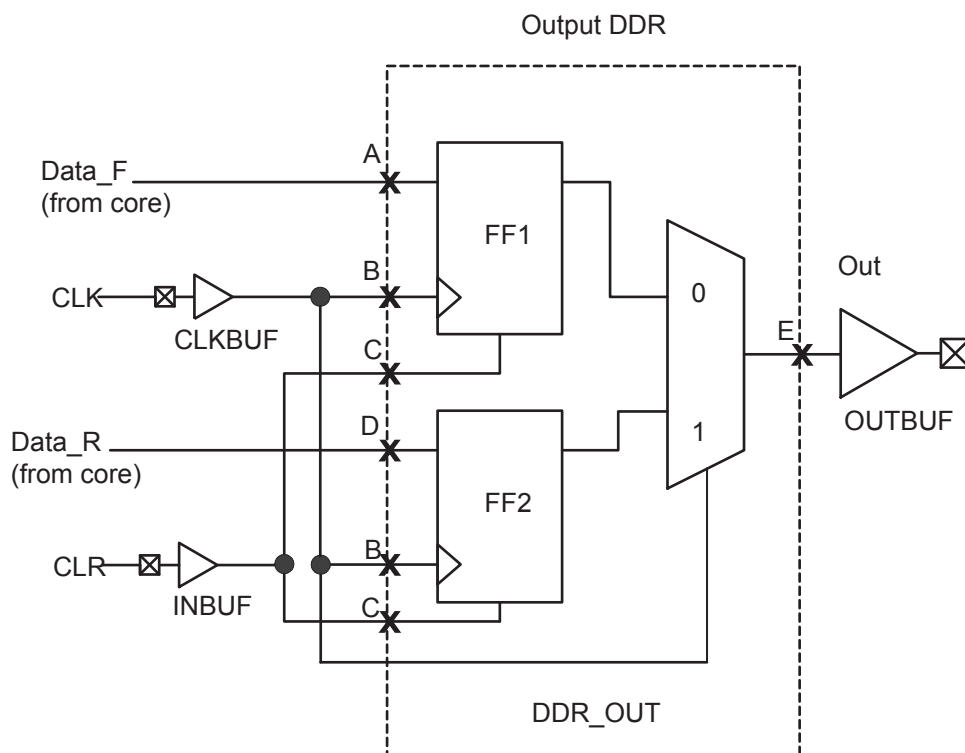


Figure 2-35 • Output DDR Timing Model

Table 2-185 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Table 2-208 • RAM512X18
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.30	0.35	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.11	0.13	ns
t_{ENH}	REN, WEN hold time	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.22	0.26	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.60	3.06	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.08	1.27	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.43	0.50	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.50	0.59	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	1.11	1.31	ns
	RESET Low to data out Low on RD (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.26	0.30	ns
t_{CYC}	Clock cycle time	3.89	4.57	ns
F_{MAX}	Maximum frequency	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-212 • FIFO Worst Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3P250 (256×16)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.92	4.61	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.61	3.06	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.14	1.34	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t_{REMRSTB}	RESET Removal	0.34	0.40	ns
t_{RECRSTB}	RESET Recovery	1.81	2.12	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-213 • FIFO Worst Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3P250 (512×8)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.52	5.31	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.61	3.06	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.14	1.34	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t_{REMRSTB}	RESET Removal	0.34	0.40	ns
t_{RECRSTB}	RESET Recovery	1.81	2.12	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-215 • FIFO Worst Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3P250 (2k×2)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	5.28	6.21	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.84	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.08	1.27	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t_{REMRSTB}	RESET Removal	0.34	0.40	ns
t_{RECRSTB}	RESET Recovery	1.81	2.12	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-18 for more details.

Timing Characteristics

Table 2-220 • JTAG 1532

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.80	0.94	ns
t_{DIHD}	Test Data Input Hold Time	1.60	1.88	ns
t_{TMSU}	Test Mode Select Setup Time	0.80	0.94	ns
t_{TMDHD}	Test Mode Select Hold Time	1.60	1.88	ns
t_{TCK2Q}	Clock to Q (data out)	6.39	7.52	ns
t_{RSTB2Q}	Reset to Q (data out)	26.63	31.33	ns
F_{TCKMAX}	TCK Maximum Frequency	18.70	15.90	MHz
t_{TRSTREM}	ResetB Removal Time	0.48	0.56	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-221 • JTAG 1532

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for All Dies

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.60	0.71	ns
t_{DIHD}	Test Data Input Hold Time	1.21	1.42	ns
t_{TMSU}	Test Mode Select Setup Time	0.60	0.71	ns
t_{TMDHD}	Test Mode Select Hold Time	1.21	1.42	ns
t_{TCK2Q}	Clock to Q (data out)	6.04	7.10	ns
t_{RSTB2Q}	Reset to Q (data out)	24.15	28.41	ns
F_{TCKMAX}	TCK Maximum Frequency	22.00	19.00	MHz
t_{TRSTREM}	ResetB Removal Time	0.00	0.00	ns
t_{TRSTREC}	ResetB Recovery Time	0.24	0.28	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

FG256	
Pin Number	A3P1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	A3P1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	A3P1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG896	
Pin Number	A3PE3000L Function
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST

FG896	
Pin Number	A3PE3000L Function
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC

FG896	
Pin Number	A3PE3000L Function
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND

FG896	
Pin Number	A3PE3000L Function
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	VCC IB0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2

FG896	
Pin Number	A3PE3000L Function
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2