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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1pqg208m

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Flash*Freeze Technology^{††}

Military ProASIC3EL devices offer proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; all core registers and SRAM cells retain their states. I/Os are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLLs. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the military ProASIC3EL device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

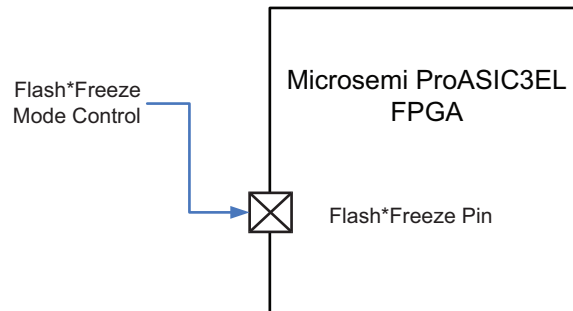


Figure 1-3 • Military ProASIC3EL Flash*Freeze Mode

VersaTiles

The military ProASIC3/EL core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The military ProASIC3/EL VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

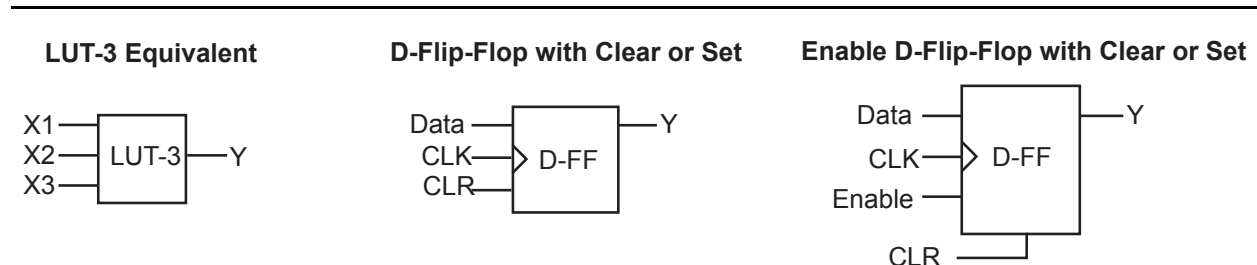


Figure 1-4 • VersaTile Configurations

^{††}Flash*Freeze technology is not supported for A3P1000.

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C) ²	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits¹

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot (125°C) ²
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.82 V
3.3 V	10%	0.69 V
	5%	0.79 V
3.6 V	10%	N/A
	5%	N/A

Notes:

1. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
2. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#).

There are five regions to consider during power-up.

Military ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#)).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.22
3.3 V LVCMOS – Wide Range	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.83
LVPECL	3.3	5.72	1.81

Notes:

1. PDC6 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VMV.

Table 2-16 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.23
3.3 V LVCMOS – Wide Range	3.3	–	16.23
2.5 V LVCMOS	2.5	–	4.66
1.8 V LVCMOS	1.8	–	1.64
1.5 V LVCMOS (JESD8-11)	1.5	–	0.99
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64

Notes:

1. PDC6 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VMV.

User I/O Characteristics

Timing Model

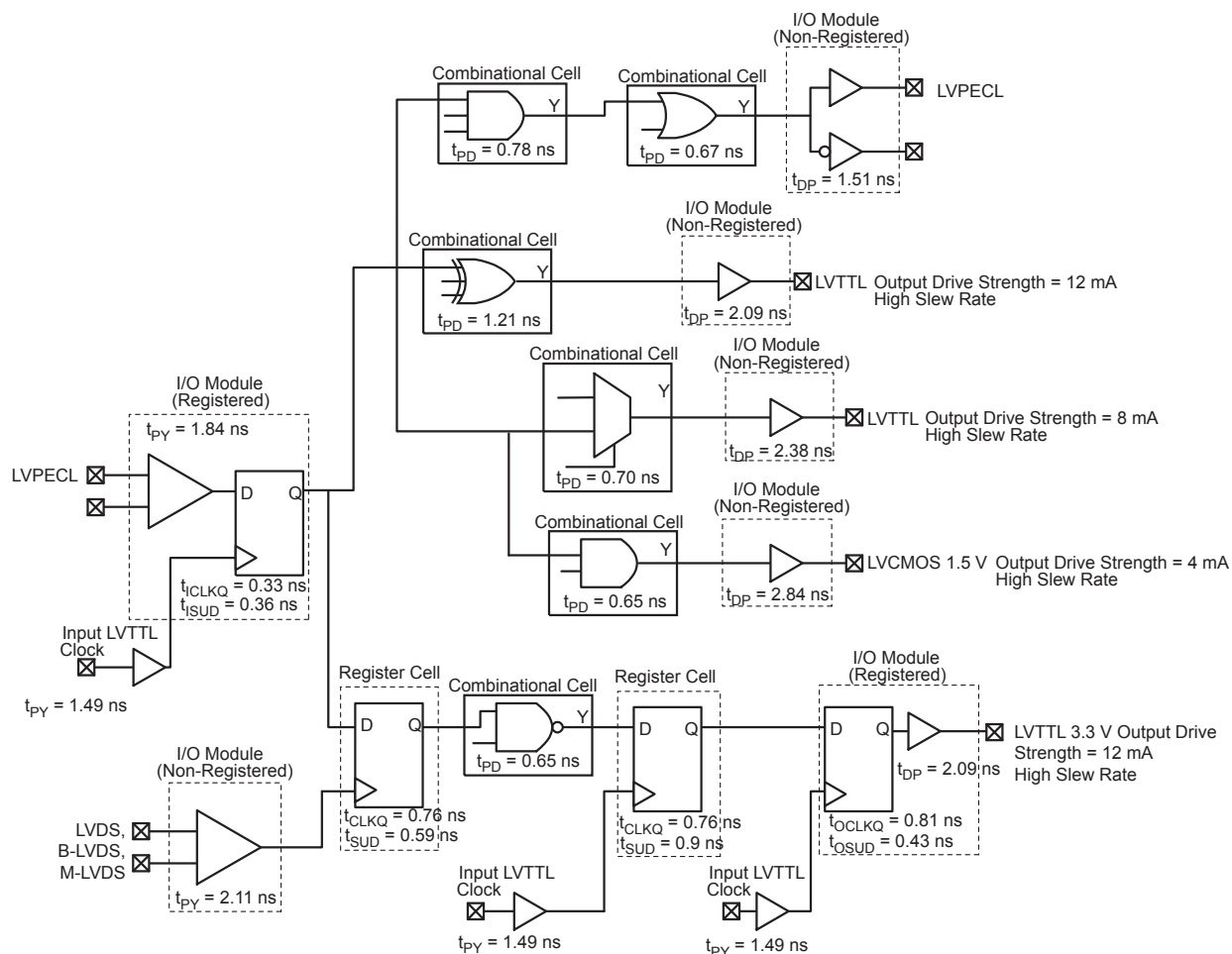


Figure 2-3 • Timing Model

Operating Conditions: –1 Speed, Military Temperature Range ($T_J = 125^\circ\text{C}$), Worst-Case VCC = 1.14 V (example for A3PE3000L and A3PE600L)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels
 Applicable to Military Conditions—Software Default Settings
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	VIL		VIH		VOL	VOH	I _{OL} ²	I _{OH} ²
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ^{1,3}	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS ^{4,5}	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{1,4,5}	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA ⁶	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA ⁶	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA ⁶	15 mA ⁶	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

- Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- Currents are measured at 125°C junction temperature.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
- Applicable to A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Output drive strength is below JEDEC specification.
- Output slew rate can be extracted using the IBIS Models.

1.2 V Core Operating Voltage

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst Case $V_{CC} = 1.14\text{ V}$, Worst Case V_{CCI}
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.09	0.05	1.49	2.03	0.44	2.12	1.56	2.76	3.06	3.99	3.43
3.3 V LVCMOS Wide Range ³	100 μA	12 mA	High	5	–	0.68	3.01	0.04	1.86	2.69	0.44	3.01	2.22	4.03	4.42	4.89	4.09
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.12	0.04	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.71	0.04	1.86	2.61	0.44	2.76	2.24	3.34	3.69	4.63	4.12
1.2 V LVCMOS	2 mA	2 mA	High	5	–	0.68	4.39	0.04	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
1.2 V LVCOMS Wide Range ⁴	100 μA	2 mA	High	5	–	0.68	4.39	0.04	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
3.3 V PCI	Per PCI spec	–	High	10	25 ⁵	0.68	2.37	0.04	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁵	0.68	2.37	0.04	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V GTL	20 mA ⁶	20 mA ⁶	High	10	25	0.68	1.75	0.05	1.99	–	0.44	1.71	1.75	–	–	3.59	3.62
2.5 V GTL	20 mA ⁶	20 mA ⁶	High	10	25	0.68	1.79	0.05	1.93	–	0.44	1.82	1.79	–	–	3.70	3.67
3.3 V GTL+	35 mA	35 mA	High	10	25	0.68	1.74	0.05	1.99	–	0.44	1.76	1.73	–	–	3.64	3.61
2.5 V GTL+	33 mA	33 mA	High	10	25	0.68	1.86	0.05	1.93	–	0.44	1.89	1.77	–	–	3.77	3.64
HSTL (I)	8 mA	8 mA	High	20	25	0.68	2.68	0.05	2.34	–	0.44	2.73	2.65	–	–	4.60	4.52
HSTL (II)	15 mA ⁶	15 mA ⁶	High	20	50	0.68	2.55	0.05	2.34	–	0.44	2.59	2.28	–	–	4.47	4.16
SSTL2 (I)	15 mA	15 mA	High	30	25	0.68	1.80	0.05	1.78	–	0.44	1.82	1.55	–	–	1.82	1.55
SSTL2 (II)	15 mA	15 mA	High	30	50	0.68	1.83	0.05	1.78	–	0.44	1.86	1.49	–	–	1.86	1.49
SSTL3 (I)	14 mA	14 mA	High	30	25	0.68	1.95	0.05	1.71	–	0.44	1.98	1.55	–	–	1.98	1.55
SSTL3 (II)	21 mA	21 mA	High	30	50	0.68	1.75	0.05	1.71	–	0.44	1.77	1.41	–	–	1.77	1.41
LVDS	24 mA	–	High	–	–	0.68	1.59	0.05	2.11	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.68	1.51	0.05	1.84	–	–	–	–	–	–	–	–

Notes:

- Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
- Output drive strength is below JEDEC specification.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-33 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.425 V,
Worst Case VCCI
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor (Ω)	t _{DOUT} (ns)	t _{DP} (ns)	t _{DIN} (ns)	t _{PY} (ns)	t _{EOUT} (ns)	t _{ZL} (ns)	t _{ZH} (ns)	t _{LZ} (ns)	t _{HZ} (ns)	t _{ZLS} (ns)	t _{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79
3.3 V LVCMOS Wide Range ³	100 μA	12 mA	High	5	–	0.54	3.47	0.04	1.44	0.39	3.47	2.57	4.65	5.18	6.64	5.75
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55
3.3 V PCI	Per PCI spec.		High	10	25 ⁴	0.54	2.51	0.04	0.81	0.39	2.55	1.83	3.00	3.35	4.65	3.92
3.3 V PCI-X	Per PCI-X spec.		High	10	25 ⁴	0.54	2.51	0.04	0.78	0.39	2.55	1.83	3.00	3.35	4.65	3.92
LVDS	24 mA		High	–	–	0.54	1.76	0.04	1.55	–	–	–	–	–	–	–
LVPECL	24 mA		High	–	–	0.54	1.68	0.04	1.31	–	–	–	–	–	–	–

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software. Software default load is higher.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-36 • I/O Output Buffer Maximum Resistances ¹
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS ⁴	2 mA	158	158
1.2 V LVCMOS Wide Range ⁴	100 μA	158	158
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA ⁵	11	–
2.5 V GTL	20 mA ⁵	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA ⁵	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$
4. Applicable to A3PE600L and A3PE3000L devices operating in the 1.2 V core range only.
5. Output drive strength is below JEDEC specification.

Table 2-41 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTTL / 3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 μ A	Same specification as regular LVCMOS 3.3 V	
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: * $T_J = 100^{\circ}\text{C}$

Table 2-92 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	–1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	–1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-93 • 1.8 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	–1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	–1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-106 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

1.2 V LVCMOS ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ²	IIH ³
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. ⁴ mA	Max. ⁴ mA	μA ⁵	μA ⁵
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	15	15

Notes:

1. Applicable to A3PE600L and A3PE3000L devices only.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 125°C junction temperature.
6. Software default selection highlighted in gray.

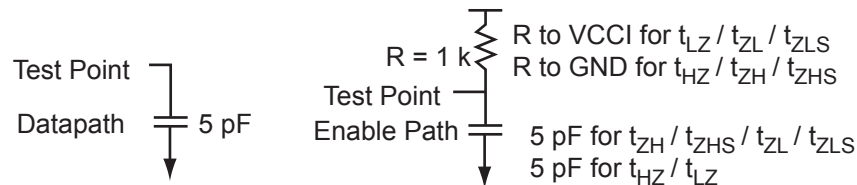


Figure 2-12 • AC Loading

Table 2-107 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C _{LOAD} (pF)
0	1.2	0.6	—	5

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-116 • 3.3 V PCI/PCI-X

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.80	2.78	0.05	2.71	3.68	0.52	2.83	1.97	3.26	3.59	5.03	4.18	ns
–1	0.68	2.37	0.05	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.5 V DC Core Voltage

Table 2-117 • 3.3 V PCI/PCI-X

Military-Case Conditions: $T_J = 125^\circ\text{C}$, VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.61	2.65	0.04	2.39	3.38	0.40	2.67	1.86	3.10	3.40	4.14	3.33	ns
–1	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-118 • 3.3 V PCI/PCI-X

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Advanced I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.63	2.95	0.05	0.95	0.45	3.00	2.15	3.53	3.94	5.46	4.61	ns
–1	0.54	2.51	0.04	0.81	0.39	2.55	1.83	3.00	3.35	4.65	3.92	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-119 • 3.3 V PCI/PCI-X

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Standard Plus I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.63	2.54	0.05	0.94	0.45	2.59	1.87	3.07	3.54	5.04	4.33	ns
–1	0.54	2.16	0.04	0.80	0.39	2.20	1.60	2.61	3.01	4.29	3.69	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-151 • SSTL2 Class II

Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$, $V_{REF} = 1.25\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.02	0.04	1.85	0.40	2.03	1.64	—	—	2.03	1.64	ns
–1	0.52	1.72	0.03	1.58	0.34	1.73	1.39	—	—	1.73	1.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class I

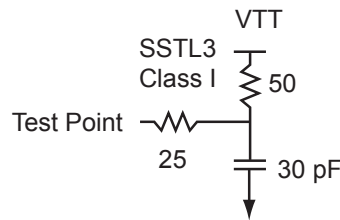
Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-152 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}^1	I_{IH}^2
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA^4	μA^4
14 mA	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCI} - 1.1$	14	14	51	54	15	15

Notes:

- I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 125°C junction temperature.


Figure 2-23 • AC Loading
Table 2-153 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.2$	$V_{REF} + 0.2$	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-154 • SSTL3 Class I

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.29	0.05	2.00	0.52	2.32	1.82	—	—	2.32	1.82	ns
–1	0.68	1.95	0.05	1.71	0.44	1.98	1.55	—	—	1.98	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-155 • SSTL3 Class I

Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.15	0.04	1.77	0.40	2.17	1.70	—	—	2.17	1.70	ns
–1	0.52	1.83	0.03	1.51	0.34	1.84	1.45	—	—	1.84	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class II

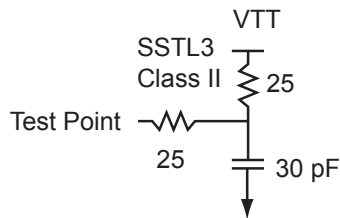
Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA^2	μA^2
21 mA	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCI} - 0.9$	21	21	103	109	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.


Figure 2-24 • AC Loading
Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.2$	$V_{REF} + 0.2$	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-158 • SSTL3 Class II

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.00	0.52	2.08	1.65	—	—	2.08	1.65	ns
–1	0.68	1.75	0.05	1.71	0.44	1.77	1.41	—	—	1.77	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-26](#). The input and output buffer delays are available in the LVDS section in [Table 2-160 on page 2-86](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

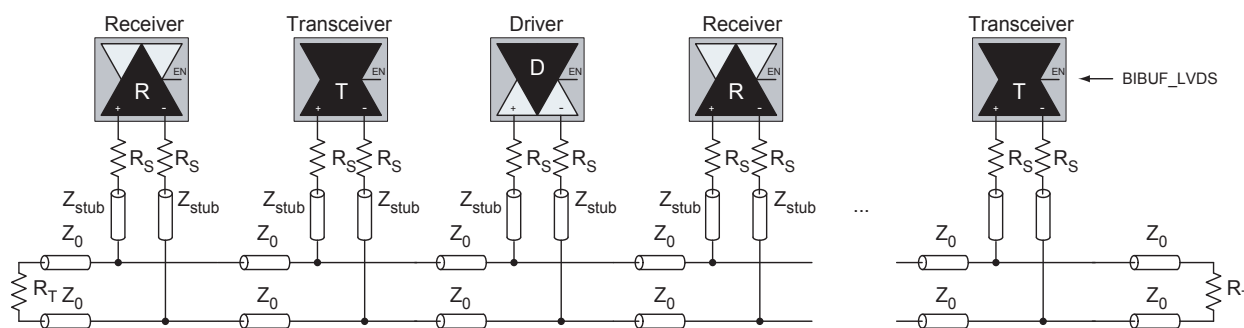


Figure 2-26 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

Table 2-191 • Combinatorial Cell Propagation Delays

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for A3P250 and A3P1000

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	$Y = !A$	t_{PD}	0.48	0.57	ns
AND2	$Y = A \cdot B$	t_{PD}	0.57	0.67	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.57	0.67	ns
OR2	$Y = A + B$	t_{PD}	0.59	0.69	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.59	0.69	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.89	1.04	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.84	0.99	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.05	1.24	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.61	0.72	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.68	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Special Function Pins

NC**No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC**Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

Military ProASIC3/EL Device Family User's Guide

http://www.microsemi.com/document-portal/doc_view/130864-military-proasic3-el-fpga-fabric-user-s-guide

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/document-portal/doc_view/131095-package-mechanical-drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG484		FG484		FG484	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
E18	GBA2/IO36PDB2V0	G9	IO09NDB0V1	H22	NC
E19	IO42NDB2V0	G10	IO09PDB0V1	J1	IO123NDB7V0
E20	GND	G11	IO13PDB0V2	J2	IO123PDB7V0
E21	NC	G12	IO21PDB1V0	J3	NC
E22	NC	G13	IO25PDB1V0	J4	IO124PDB7V0
F1	NC	G14	IO27NDB1V0	J5	IO125PDB7V0
F2	IO131NDB7V1	G15	GNDQ	J6	IO126PDB7V0
F3	IO131PDB7V1	G16	VCOMPLB	J7	IO130NDB7V1
F4	IO133NDB7V1	G17	GBB2/IO37PDB2V0	J8	VCCIB7
F5	IO134NDB7V1	G18	IO39PDB2V0	J9	GND
F6	VMV7	G19	IO39NDB2V0	J10	VCC
F7	VCCPLA	G20	IO43PDB2V0	J11	VCC
F8	GAC0/IO02NDB0V0	G21	IO43NDB2V0	J12	VCC
F9	GAC1/IO02PDB0V0	G22	NC	J13	VCC
F10	IO15NDB0V2	H1	NC	J14	GND
F11	IO15PDB0V2	H2	NC	J15	VCCIB2
F12	IO20PDB1V0	H3	VCC	J16	IO38NDB2V0
F13	IO25NDB1V0	H4	IO128NDB7V1	J17	IO40NDB2V0
F14	IO27PDB1V0	H5	IO129NDB7V1	J18	IO40PDB2V0
F15	GBC0/IO33NDB1V1	H6	IO132NDB7V1	J19	IO45PDB2V1
F16	VCCPLB	H7	IO130PDB7V1	J20	NC
F17	VMV2	H8	VMV0	J21	IO48PDB2V1
F18	IO36NDB2V0	H9	VCCIB0	J22	IO46PDB2V1
F19	IO42PDB2V0	H10	VCCIB0	K1	IO121NDB7V0
F20	NC	H11	IO13NDB0V2	K2	IO121PDB7V0
F21	NC	H12	IO21NDB1V0	K3	NC
F22	NC	H13	VCCIB1	K4	IO124NDB7V0
G1	IO127NDB7V1	H14	VCCIB1	K5	IO125NDB7V0
G2	IO127PDB7V1	H15	VMV1	K6	IO126NDB7V0
G3	NC	H16	GBC2/IO38PDB2V0	K7	GFC1/IO120PPB7V0
G4	IO128PDB7V1	H17	IO37NDB2V0	K8	VCCIB7
G5	IO129PDB7V1	H18	IO41NDB2V0	K9	VCC
G6	GAC2/IO132PDB7V1	H19	IO41PDB2V0	K10	GND
G7	VCOMPLA	H20	VCC	K11	GND
G8	GNDQ	H21	NC	K12	GND

FG896	
Pin Number	A3PE3000L Function
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0

FG896	
Pin Number	A3PE3000L Function
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3

FG896	
Pin Number	A3PE3000L Function
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0