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### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

| Product Status                 | Active   |
|--------------------------------|--|
| Number of LABs/CLBs            | -  |
| Number of Logic Elements/Cells | -  |
| Total RAM Bits                 | 147456   |
| Number of I/O                  | 177  |
| Number of Gates                | 1000000  |
| Voltage - Supply               | 1.14V ~ 1.575V   |
| Mounting Type                  | Surface Mount  |
| Operating Temperature          | -55°C ~ 125°C (TJ)   |
| Package / Case                 | 256-LBGA   |
| Supplier Device Package        | 256-FBGA (17x17)   |
| Purchase URL                   | https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-2fgg256m |
|                                |  |

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 Table 2-66 • 3.3 V LVCMOS Wide Range Low Slew

 Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

 Applicable to Advanced I/O Banks

| Drive<br>Strength | Equiv.<br>Software<br>Default<br>Drive<br>Strength<br>Option <sup>1</sup> | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>ZLS</sub> | t <sub>zнs</sub> | Units |
|-------------------|---|----------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 100 µA            | 4 mA  | Std.           | 0.63              | 9.67            | 0.05             | 1.70            | 0.45              | 9.67            | 8.03            | 4.50            | 4.18            | 13.40            | 11.77            | ns    |
|                   |   | -1             | 0.54              | 8.22            | 0.04             | 1.44            | 0.39              | 8.22            | 6.83            | 3.83            | 3.55            | 11.40            | 10.01            | ns    |
| 100 µA            | 6mA   | Std.           | 0.63              | 8.13            | 0.05             | 1.70            | 0.45              | 8.13            | 6.95            | 5.07            | 5.17            | 11.86            | 10.69            | ns    |
|                   |   | -1             | 0.54              | 6.91            | 0.04             | 1.44            | 0.39              | 6.91            | 5.92            | 4.31            | 4.40            | 10.09            | 9.09             | ns    |
| 100 µA            | 8 mA  | Std.           | 0.63              | 8.13            | 0.05             | 1.70            | 0.45              | 8.13            | 6.95            | 5.07            | 5.17            | 11.86            | 10.69            | ns    |
|                   |   | -1             | 0.54              | 6.91            | 0.04             | 1.44            | 0.39              | 6.91            | 5.92            | 4.31            | 4.40            | 10.09            | 9.09             | ns    |
| 100 µA            | 12 mA   | Std.           | 0.63              | 6.96            | 0.05             | 1.70            | 0.45              | 6.96            | 6.15            | 5.45            | 5.81            | 10.70            | 9.89             | ns    |
|                   |   | -1             | 0.54              | 5.92            | 0.04             | 1.44            | 0.39              | 5.92            | 5.24            | 4.64            | 4.94            | 9.10             | 8.41             | ns    |
| 100 µA            | 16 mA   | Std.           | 0.63              | 6.61            | 0.05             | 1.70            | 0.45              | 6.61            | 5.96            | 5.54            | 5.97            | 10.34            | 9.70             | ns    |
|                   |   | -1             | 0.54              | 5.62            | 0.04             | 1.44            | 0.39              | 5.62            | 5.07            | 4.71            | 5.08            | 8.80             | 8.25             | ns    |

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### Table 2-67 • 3.3 V LVCMOS Wide Range High Slew

Military-Case Conditions:  $T_J = 125^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V Applicable to Advanced I/O Banks

| Drive<br>Strength | Equiv.<br>Software<br>Default<br>Drive<br>Strength<br>Option <sup>1</sup> | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>ZLS</sub> | t <sub>zHS</sub> | Units |
|-------------------|---|----------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 100 µA            | 4 mA  | Std.           | 0.63              | 5.49            | 0.05             | 1.70            | 0.45              | 5.49            | 4.23            | 4.51            | 4.44            | 9.22             | 7.97             | ns    |
|                   |   | -1             | 0.54              | 4.67            | 0.04             | 1.44            | 0.39              | 4.57            | 3.60            | 3.83            | 3.78            | 7.84             | 6.78             | ns    |
| 100 µA            | 6 mA  | Std.           | 0.63              | 4.56            | 0.05             | 1.70            | 0.45              | 4.56            | 3.42            | 5.08            | 5.45            | 8.29             | 7.15             | ns    |
|                   |   | -1             | 0.54              | 3.88            | 0.04             | 1.44            | 0.39              | 3.88            | 2.91            | 4.32            | 4.64            | 7.05             | 6.08             | ns    |
| 100 µA            | 8 mA  | Std.           | 0.63              | 4.56            | 0.05             | 1.70            | 0.45              | 4.56            | 3.42            | 5.08            | 5.45            | 8.29             | 7.15             | ns    |
|                   |   | -1             | 0.54              | 3.88            | 0.04             | 1.44            | 0.39              | 3.88            | 2.91            | 4.32            | 4.64            | 7.05             | 6.08             | ns    |
| 100 µA            | 12 mA   | Std.           | 0.63              | 4.08            | 0.05             | 1.70            | 0.45              | 4.08            | 3.03            | 5.46            | 6.09            | 7.81             | 6.76             | ns    |
|                   |   | -1             | 0.54              | 3.47            | 0.04             | 1.44            | 0.39              | 3.47            | 2.57            | 4.65            | 5.18            | 6.64             | 5.75             | ns    |
| 100 µA            | 16 mA   | Std.           | 0.63              | 4.00            | 0.05             | 1.70            | 0.45              | 4.00            | 2.96            | 5.55            | 6.26            | 7.73             | 6.69             | ns    |
|                   |   | -1             | 0.54              | 3.40            | 0.04             | 1.44            | 0.39              | 3.40            | 2.51            | 4.72            | 5.32            | 6.58             | 5.69             | ns    |

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## 🌜 Microsemi.

Military ProASIC3/EL DC and Switching Characteristics

| 2.5 V<br>LVCMOS   |           | VIL       | VI        | 1         | VOL       | VOH       | I <sub>OL</sub> | I <sub>OH</sub> | I <sub>OSL</sub>        | I <sub>OSH</sub>        | ا <sub>ال</sub> 1 | I <sub>IH</sub> 2 |
|-------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------------|-----------------|-------------------------|-------------------------|-------------------|-------------------|
| Drive<br>Strength | Min.<br>V | Max.<br>V | Min.<br>V | Max.<br>V | Max.<br>V | Min.<br>V | mA              | mA              | Max.<br>mA <sup>3</sup> | Max.<br>mA <sup>3</sup> | μA <sup>4</sup>   | μA <sup>5</sup>   |
| 2 mA              | -0.3      | 0.7       | 1.7       | 2.7       | 0.7       | 1.7       | 2               | 2               | 16                      | 18                      | 15                | 15                |
| 4 mA              | -0.3      | 0.7       | 1.7       | 2.7       | 0.7       | 1.7       | 4               | 4               | 16                      | 18                      | 15                | 15                |
| 6 mA              | -0.3      | 0.7       | 1.7       | 2.7       | 0.7       | 1.7       | 6               | 6               | 32                      | 37                      | 15                | 15                |
| 8 mA              | -0.3      | 0.7       | 1.7       | 2.7       | 0.7       | 1.7       | 8               | 8               | 32                      | 37                      | 15                | 15                |
| 12 mA             | -0.3      | 0.7       | 1.7       | 2.7       | 0.7       | 1.7       | 12              | 12              | 65                      | 74                      | 15                | 15                |

## Table 2-72 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

Notes:

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 125°C junction temperature.

5. Software default selection highlighted in gray.

Test Point 
$$rac{1}{1}$$
  $rac{1}{1}$   $rac{1$ 

### Figure 2-9 • AC Loading

### Table 2-73 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (Typ) (V) | C <sub>LOAD</sub> (pF) |
|---------------|----------------|----------------------|----------------|------------------------|
| 0             | 2.5            | 1.2                  | -              | 5                      |

Note: \*Measuring point =  $V_{trip.}$  See Table 2-29 on page 2-25 for a complete table of trip points.

### 🌜 Microsemi.

Military ProASIC3/EL DC and Switching Characteristics

### 1.5 V DC Core Voltage

# Table 2-76 • 2.5 V LVCMOS Low Slew<br/>Military-Case Conditions: TJ = 125°C, VCC = 1.425 V, Worst-Case VCCI = 2.3 V<br/>Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

| Drive<br>Strength | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>PYS</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>ZH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>zLS</sub> | t <sub>zHS</sub> | Units |
|-------------------|----------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 4 mA              | Std.           | 0.61              | 6.73            | 0.04             | 1.75            | 2.26             | 0.40              | 6.83            | 5.71            | 2.54            | 1.99            | 8.30             | 7.18             | ns    |
|                   | -1             | 0.52              | 5.73            | 0.03             | 1.49            | 1.93             | 0.34              | 5.81            | 4.86            | 2.16            | 1.69            | 7.06             | 6.10             | ns    |
| 8 mA              | Std.           | 0.61              | 5.48            | 0.04             | 1.75            | 2.26             | 0.40              | 5.56            | 4.82            | 2.92            | 2.71            | 7.02             | 6.29             | ns    |
|                   | –1             | 0.52              | 4.66            | 0.03             | 1.49            | 1.93             | 0.34              | 4.73            | 4.10            | 2.48            | 2.30            | 5.98             | 5.35             | ns    |
| 12 mA             | Std.           | 0.61              | 4.59            | 0.04             | 1.75            | 2.26             | 0.40              | 4.65            | 4.18            | 3.18            | 3.18            | 6.12             | 5.65             | ns    |
|                   | -1             | 0.52              | 3.91            | 0.03             | 1.49            | 1.93             | 0.34              | 3.96            | 3.56            | 2.71            | 2.70            | 5.20             | 4.80             | ns    |
| 16 mA             | Std.           | 0.61              | 4.32            | 0.04             | 1.75            | 2.26             | 0.40              | 4.38            | 4.04            | 3.24            | 3.31            | 5.84             | 5.51             | ns    |
|                   | -1             | 0.52              | 3.68            | 0.03             | 1.49            | 1.93             | 0.34              | 3.72            | 3.44            | 2.75            | 2.81            | 4.97             | 4.69             | ns    |
| 24 mA             | Std.           | 0.61              | 4.20            | 0.04             | 1.75            | 2.26             | 0.40              | 4.26            | 4.06            | 3.31            | 3.76            | 5.72             | 5.52             | ns    |
|                   | -1             | 0.52              | 3.58            | 0.03             | 1.49            | 1.93             | 0.34              | 3.62            | 3.45            | 2.82            | 3.20            | 4.87             | 4.70             | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### Table 2-77 • 2.5 V LVCMOS High Slew

|                   | •  |
|-------------------|--|
| Military-Case Co  | nditions: T <sub>J</sub> = 125°C, VCC = 1.425 V, Worst-Case VCCI = 2.3 V |
| Applicable to Pro | I/Os for A3PE600L and A3PE3000L Only                                     |

| Drive<br>Strength | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>PYS</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>ZLS</sub> | t <sub>zHS</sub> | Units |
|-------------------|----------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 4 mA              | Std.           | 0.61              | 3.37            | 0.04             | 1.75            | 2.26             | 0.40              | 3.41            | 3.01            | 2.54            | 2.08            | 4.87             | 4.48             | ns    |
|                   | –1             | 0.52              | 2.87            | 0.03             | 1.49            | 1.93             | 0.34              | 2.90            | 2.56            | 2.16            | 1.77            | 4.14             | 3.81             | ns    |
| 8 mA              | Std.           | 0.61              | 2.74            | 0.04             | 1.75            | 2.26             | 0.40              | 2.76            | 2.29            | 2.92            | 2.82            | 4.23             | 3.75             | ns    |
|                   | -1             | 0.52              | 2.33            | 0.03             | 1.49            | 1.93             | 0.34              | 2.35            | 1.95            | 2.48            | 2.40            | 3.60             | 3.19             | ns    |
| 12 mA             | Std.           | 0.61              | 2.36            | 0.04             | 1.75            | 2.26             | 0.40              | 2.38            | 1.93            | 3.18            | 3.27            | 3.84             | 3.40             | ns    |
|                   | -1             | 0.52              | 2.01            | 0.03             | 1.49            | 1.93             | 0.34              | 2.02            | 1.65            | 2.71            | 2.78            | 3.27             | 2.89             | ns    |
| 16 mA             | Std.           | 0.61              | 2.29            | 0.04             | 1.75            | 2.26             | 0.40              | 2.31            | 1.87            | 3.24            | 3.40            | 3.77             | 3.33             | ns    |
|                   | –1             | 0.52              | 1.95            | 0.03             | 1.49            | 1.93             | 0.34              | 1.96            | 1.59            | 2.75            | 2.89            | 3.21             | 2.84             | ns    |
| 24 mA             | Std.           | 0.61              | 2.31            | 0.04             | 1.75            | 2.26             | 0.40              | 2.32            | 1.78            | 3.31            | 3.89            | 3.79             | 3.25             | ns    |
|                   | -1             | 0.52              | 1.96            | 0.03             | 1.49            | 1.93             | 0.34              | 1.98            | 1.52            | 2.82            | 3.31            | 3.22             | 2.76             | ns    |

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

| 1.5 V<br>LVCMOS   |           | VIL         | VIH         |           | VOL         | VOH         | I <sub>OL</sub> | I <sub>ОН</sub> | I <sub>OSL</sub>        | I <sub>OSH</sub>        | ا <sub>ال</sub> 1 | I <sub>IH</sub> 2 |
|-------------------|-----------|-------------|-------------|-----------|-------------|-------------|-----------------|-----------------|-------------------------|-------------------------|-------------------|-------------------|
| Drive<br>Strength | Min.<br>V | Max.<br>V   | Min.<br>V   | Max.<br>V | Max.<br>V   | Min.<br>V   | mA              | mA              | Max.<br>mA <sup>3</sup> | Max.<br>mA <sup>3</sup> | μA <sup>4</sup>   | μA <sup>4</sup>   |
| 2 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 3.6       | 0.25 * VCCI | 0.75 * VCCI | 2               | 2               | 13                      | 16                      | 15                | 15                |
| 4 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 3.6       | 0.25 * VCCI | 0.75 * VCCI | 4               | 4               | 25                      | 33                      | 15                | 15                |
| 6 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 3.6       | 0.25 * VCCI | 0.75 * VCCI | 6               | 6               | 32                      | 39                      | 15                | 15                |
| 8 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 3.6       | 0.25 * VCCI | 0.75 * VCCI | 8               | 8               | 66                      | 55                      | 15                | 15                |
| 12 mA             | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 3.6       | 0.25 * VCCI | 0.75 * VCCI | 12              | 12              | 66                      | 55                      | 15                | 15                |

### Table 2-94 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Notes:

1.  $I_{II}$  is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges</li>

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 125°C junction temperature.

5. Software default selection highlighted in gray.

## Table 2-95 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

| 1.5 V<br>LVCMOS   |           | VIL         | VIH         |           | V <sub>OL</sub> | VOH         | I <sub>OL</sub> | I <sub>ОН</sub> | I <sub>OSL</sub>        | I <sub>OSH</sub>        | ا <sub>ال</sub> 1 | I <sub>IH</sub> 2 |
|-------------------|-----------|-------------|-------------|-----------|-----------------|-------------|-----------------|-----------------|-------------------------|-------------------------|-------------------|-------------------|
| Drive<br>Strength | Min.<br>V | Max.<br>V   | Min.<br>V   | Max.<br>V | Max.<br>V       | Min.<br>V   | mA              | mA              | Max.<br>mA <sup>3</sup> | Max.<br>mA <sup>3</sup> | μA <sup>4</sup>   | μA <sup>4</sup>   |
| 2 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 1.575     | 0.25 * VCCI     | 0.75 * VCCI | 2               | 2               | 13                      | 16                      | 15                | 15                |
| 4 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 1.575     | 0.25 * VCCI     | 0.75 * VCCI | 4               | 4               | 25                      | 33                      | 15                | 15                |
| 6 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 1.575     | 0.25 * VCCI     | 0.75 * VCCI | 6               | 6               | 32                      | 39                      | 15                | 15                |
| 8 mA              | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 1.575     | 0.25 * VCCI     | 0.75 * VCCI | 8               | 8               | 66                      | 55                      | 15                | 15                |
| 12 mA             | -0.3      | 0.35 * VCCI | 0.65 * VCCI | 1.575     | 0.25 * VCCI     | 0.75 * VCCI | 12              | 12              | 66                      | 55                      | 15                | 15                |

Notes:

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges</li>

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 125°C junction temperature.

5. Software default selection highlighted in gray.

### LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-27. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



|                      | Circuit Disaram and    | Roard Laval Implana    | ntation   |
|----------------------|------------------------|------------------------|-----------|
| FIGUIE Z=Z/ • LVFEGE | CITCUIL DIAUTAILI ALIU | Dualu-Level IIIIDielle | illalioii |
|                      |                        |                        |           |

| DC Parameter       | Description                    | Min.  | Max. | Min.  | Max. | Min.  | Max. | Units |
|--------------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| VCCI               | Supply Voltage                 | 3.0   |      | 3.3   |      | 3     | 6.6  | V     |
| VOL                | Output Low Voltage             | 0.96  | 1.27 | 1.06  | 1.43 | 1.30  | 1.57 | V     |
| VOH                | Output High Voltage            | 1.8   | 2.11 | 1.92  | 2.28 | 2.13  | 2.41 | V     |
| VIL, VIH           | Input Low, Input High Voltages | 0     | 3.3  | 0     | 3.6  | 0     | 3.9  | V     |
| V <sub>ODIFF</sub> | Differential Output Voltage    | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V     |
| V <sub>OCM</sub>   | Output Common-Mode Voltage     | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V     |
| V <sub>ICM</sub>   | Input Common-Mode Voltage      | 1.01  | 2.57 | 1.01  | 2.57 | 1.01  | 2.57 | V     |
| V <sub>IDIFF</sub> | Input Differential Voltage     | 300   |      | 300   |      | 300   |      | mV    |

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) |  |  |
|---------------|----------------|----------------------|--|--|
| 1.64          | 1.94           | Cross point          |  |  |

Note: \*Measuring point =  $V_{trip.}$  See Table 2-29 on page 2-25 for a complete table of trip points.

### **I/O Register Specifications**



### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-28 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

## **Microsemi**.

Military ProASIC3/EL DC and Switching Characteristics

## Table 2-177 • Output Data Register Propagation DelaysMilitary-Case Conditions: TJ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

| Parameter            | Description  | -1   | Std. | Units |
|----------------------|--|------|------|-------|
| t <sub>OCLKQ</sub>   | Clock-to-Q of the Output Data Register                               | 0.71 | 0.83 | ns    |
| t <sub>OSUD</sub>    | Data Setup Time for the Output Data Register                         | 0.38 | 0.44 | ns    |
| t <sub>OHD</sub>     | Data Hold Time for the Output Data Register                          | 0.00 | 0.00 | ns    |
| t <sub>OSUE</sub>    | Enable Setup Time for the Output Data Register                       | 0.53 | 0.62 | ns    |
| t <sub>OHE</sub>     | Enable Hold Time for the Output Data Register                        | 0.00 | 0.00 | ns    |
| t <sub>OCLR2Q</sub>  | Asynchronous Clear-to-Q of the Output Data Register                  | 0.97 | 1.14 | ns    |
| t <sub>OPRE2Q</sub>  | Asynchronous Preset-to-Q of the Output Data Register                 | 0.97 | 1.14 | ns    |
| t <sub>OREMCLR</sub> | Asynchronous Clear Removal Time for the Output Data Register         | 0.00 | 0.00 | ns    |
| t <sub>ORECCLR</sub> | Asynchronous Clear Recovery Time for the Output Data Register        | 0.27 | 0.31 | ns    |
| t <sub>OREMPRE</sub> | Asynchronous Preset Removal Time for the Output Data Register        | 0.00 | 0.00 | ns    |
| t <sub>ORECPRE</sub> | Asynchronous Preset Recovery Time for the Output Data Register       | 0.27 | 0.31 | ns    |
| t <sub>OWCLR</sub>   | Asynchronous Clear Minimum Pulse Width for the Output Data Register  | 0.25 | 0.30 | ns    |
| t <sub>OWPRE</sub>   | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.25 | 0.30 | ns    |
| t <sub>OCKMPWH</sub> | Clock Minimum Pulse Width HIGH for the Output Data Register          | 0.41 | 0.48 | ns    |
| t <sub>OCKMPWL</sub> | Clock Minimum Pulse Width LOW for the Output Data Register           | 0.37 | 0.43 | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

## static Microsemi.

Military ProASIC3/EL DC and Switching Characteristics

### **Timing Characteristics**

### Table 2-178 • Output Enable Register Propagation Delays

### Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

| Parameter             | Description  | -1   | Std. | Units |
|-----------------------|--|------|------|-------|
| t <sub>OECLKQ</sub>   | Clock-to-Q of the Output Enable Register                               | 0.62 | 0.72 | ns    |
| t <sub>OESUD</sub>    | Data Setup Time for the Output Enable Register                         | 0.43 | 0.51 | ns    |
| t <sub>OEHD</sub>     | Data Hold Time for the Output Enable Register                          | 0.00 | 0.00 | ns    |
| t <sub>OESUE</sub>    | Enable Setup Time for the Output Enable Register                       | 0.60 | 0.71 | ns    |
| t <sub>OEHE</sub>     | Enable Hold Time for the Output Enable Register                        | 0.00 | 0.00 | ns    |
| t <sub>OECLR2Q</sub>  | Asynchronous Clear-to-Q of the Output Enable Register                  | 0.92 | 1.08 | ns    |
| t <sub>OEPRE2Q</sub>  | Asynchronous Preset-to-Q of the Output Enable Register                 | 0.92 | 1.08 | ns    |
| t <sub>OEREMCLR</sub> | Asynchronous Clear Removal Time for the Output Enable Register         | 0.00 | 0.00 | ns    |
| t <sub>OERECCLR</sub> | Asynchronous Clear Recovery Time for the Output Enable Register        | 0.31 | 0.36 | ns    |
| t <sub>OEREMPRE</sub> | Asynchronous Preset Removal Time for the Output Enable Register        | 0.00 | 0.00 | ns    |
| t <sub>OERECPRE</sub> | Asynchronous Preset Recovery Time for the Output Enable Register       | 0.31 | 0.36 | ns    |
| t <sub>OEWCLR</sub>   | Asynchronous Clear Minimum Pulse Width for the Output Enable Register  | 0.19 | 0.22 | ns    |
| t <sub>OEWPRE</sub>   | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | 0.22 | ns    |
| t <sub>OECKMPWH</sub> | Clock Minimum Pulse Width HIGH for the Output Enable Register          | 0.31 | 0.36 | ns    |
| t <sub>OECKMPWL</sub> | Clock Minimum Pulse Width LOW for the Output Enable Register           | 0.28 | 0.32 | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## Table 2-179 • Output Enable Register Propagation DelaysMilitary-Case Conditions: TJ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

| Parameter             | Description  | -1   | Std. | Units |
|-----------------------|--|------|------|-------|
| t <sub>OECLKQ</sub>   | Clock-to-Q of the Output Enable Register                               | 0.47 | 0.55 | ns    |
| t <sub>OESUD</sub>    | Data Setup Time for the Output Enable Register                         | 0.33 | 0.39 | ns    |
| t <sub>OEHD</sub>     | Data Hold Time for the Output Enable Register                          | 0.00 | 0.00 | ns    |
| t <sub>OESUE</sub>    | Enable Setup Time for the Output Enable Register                       | 0.46 | 0.54 | ns    |
| t <sub>OEHE</sub>     | Enable Hold Time for the Output Enable Register                        | 0.00 | 0.00 | ns    |
| t <sub>OECLR2Q</sub>  | Asynchronous Clear-to-Q of the Output Enable Register                  | 0.70 | 0.83 | ns    |
| t <sub>OEPRE2Q</sub>  | Asynchronous Preset-to-Q of the Output Enable Register                 | 0.70 | 0.83 | ns    |
| t <sub>OEREMCLR</sub> | Asynchronous Clear Removal Time for the Output Enable Register         | 0.00 | 0.00 | ns    |
| t <sub>OERECCLR</sub> | Asynchronous Clear Recovery Time for the Output Enable Register        | 0.24 | 0.28 | ns    |
| t <sub>OEREMPRE</sub> | Asynchronous Preset Removal Time for the Output Enable Register        | 0.00 | 0.00 | ns    |
| t <sub>OERECPRE</sub> | Asynchronous Preset Recovery Time for the Output Enable Register       | 0.24 | 0.28 | ns    |
| t <sub>OEWCLR</sub>   | Asynchronous Clear Minimum Pulse Width for the Output Enable Register  | 0.19 | 0.22 | ns    |
| t <sub>OEWPRE</sub>   | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | 0.22 | ns    |
| t <sub>OECKMPWH</sub> | Clock Minimum Pulse Width HIGH for the Output Enable Register          | 0.31 | 0.36 | ns    |
| t <sub>OECKMPWL</sub> | Clock Minimum Pulse Width LOW for the Output Enable Register           | 0.28 | 0.32 | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



### Figure 2-34 • Input DDR Timing Diagram

### Timing Characteristics

Table 2-182 • Input DDR Propagation DelaysMilitary-Case Conditions: TJ = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

| Parameter               | Description  | -1   | Std. | Units |
|-------------------------|--|------|------|-------|
| t <sub>DDRICLKQ1</sub>  | Clock-to-Out Out_QR for Input DDR                    | 0.38 | 0.45 | ns    |
| t <sub>DDRICLKQ2</sub>  | Clock-to-Out Out_QF for Input DDR                    | 0.54 | 0.63 | ns    |
| t <sub>DDRISUD1</sub>   | Data Setup for Input DDR (fall)                      | 0.39 | 0.46 | ns    |
| t <sub>DDRISUD2</sub>   | Data Setup for Input DDR (rise)                      | 0.34 | 0.40 | ns    |
| t <sub>DDRIHD1</sub>    | Data Hold for Input DDR (fall)                       | 0.00 | 0.00 | ns    |
| t <sub>DDRIHD2</sub>    | Data Hold for Input DDR (rise)                       | 0.00 | 0.00 | ns    |
| t <sub>DDRICLR2Q1</sub> | Asynchronous Clear-to-Out Out_QR for Input DDR       | 0.64 | 0.75 | ns    |
| t <sub>DDRICLR2Q2</sub> | Asynchronous Clear-to-Out Out_QF for Input DDR       | 0.79 | 0.93 | ns    |
| t <sub>DDRIREMCLR</sub> | Asynchronous Clear Removal Time for Input DDR        | 0.00 | 0.00 | ns    |
| t <sub>DDRIRECCLR</sub> | Asynchronous Clear Recovery Time for Input DDR       | 0.31 | 0.36 | ns    |
| t <sub>DDRIWCLR</sub>   | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | 0.22 | ns    |
| t <sub>DDRICKMPWH</sub> | Clock Minimum Pulse Width HIGH for Input DDR         | 0.31 | 0.36 | ns    |
| t <sub>DDRICKMPWL</sub> | Clock Minimum Pulse Width LOW for Input DDR          | 0.28 | 0.32 | ns    |
| F <sub>DDRIMAX</sub>    | Maximum Frequency for Input DDR                      | 160  | 160  | MHz   |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## **VersaTile Characteristics**

### VersaTile Specifications as a Combinatorial Module

The military ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO*, *Fusion, and ProASIC3 Macro Library Guide*.



Figure 2-37 • Sample of Combinatorial Cells

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Military ProASIC3/EL DC and Switching Characteristics

### Timing Characteristics

### Table 2-192 • Register Delays

### Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

| Parameter           | Description   | -1   | Std. | Units |
|---------------------|---|------|------|-------|
| t <sub>CLKQ</sub>   | Clock-to-Q of the Core Register                               | 0.76 | 0.90 | ns    |
| t <sub>SUD</sub>    | Data Setup Time for the Core Register                         | 0.59 | 0.70 | ns    |
| t <sub>HD</sub>     | Data Hold Time for the Core Register                          | 0.00 | 0.00 | ns    |
| t <sub>SUE</sub>    | Enable Setup Time for the Core Register                       | 0.63 | 0.74 | ns    |
| t <sub>HE</sub>     | Enable Hold Time for the Core Register                        | 0.00 | 0.00 | ns    |
| t <sub>CLR2Q</sub>  | Asynchronous Clear-to-Q of the Core Register                  | 0.55 | 0.65 | ns    |
| t <sub>PRE2Q</sub>  | Asynchronous Preset-to-Q of the Core Register                 | 0.55 | 0.65 | ns    |
| t <sub>REMCLR</sub> | Asynchronous Clear Removal Time for the Core Register         | 0.00 | 0.00 | ns    |
| t <sub>RECCLR</sub> | Asynchronous Clear Recovery Time for the Core Register        | 0.31 | 0.36 | ns    |
| t <sub>REMPRE</sub> | Asynchronous Preset Removal Time for the Core Register        | 0.00 | 0.00 | ns    |
| t <sub>RECPRE</sub> | Asynchronous Preset Recovery Time for the Core Register       | 0.31 | 0.36 | ns    |
| t <sub>WCLR</sub>   | Asynchronous Clear Minimum Pulse Width for the Core Register  | 0.30 | 0.34 | ns    |
| t <sub>WPRE</sub>   | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | 0.34 | ns    |
| t <sub>CKMPWH</sub> | Clock Minimum Pulse Width HIGH for the Core Register          | 0.56 | 0.64 | ns    |
| t <sub>CKMPWL</sub> | Clock Minimum Pulse Width LOW for the Core Register           | 0.56 | 0.64 | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Military ProASIC3/EL DC and Switching Characteristics

### **Global Tree Timing Characteristics**

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-123. Table 2-195 to Table 2-198 on page 2-121 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

### 1.2 V DC Core Voltage

### Table 2-195 • A3PE600L Global Resource Military-Case Conditions: T<sub>J</sub> = 125°C, VCC = 1.14 V

|                      |   | -                 | -1                |                   | Std.              |       |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------|
| Parameter            | Description                               | Min. <sup>1</sup> | Max. <sup>2</sup> | Min. <sup>1</sup> | Max. <sup>2</sup> | Units |
| t <sub>RCKL</sub>    | Input LOW Delay for Global Clock          | 0.95              | 1.23              | 1.12              | 1.44              | ns    |
| t <sub>RCKH</sub>    | Input HIGH Delay for Global Clock         | 0.94              | 1.26              | 1.10              | 1.48              | ns    |
| t <sub>RCKMPWH</sub> | Minimum Pulse Width HIGH for Global Clock |                   |                   |                   |                   | ns    |
| t <sub>RCKMPWL</sub> | Minimum Pulse Width LOW for Global Clock  |                   |                   |                   |                   | ns    |
| t <sub>RCKSW</sub>   | Maximum Skew for Global Clock             |                   | 0.32              |                   | 0.38              | ns    |
| F <sub>RMAX</sub>    | Maximum Frequency for Global Clock        |                   |                   |                   |                   | MHz   |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### Table 2-196 • A3PE3000L Global Resource Military-Case Conditions: T<sub>J</sub> = 125°C, VCC = 1.14 V

|                      |   | -                 | -1                |                                     | Std. |       |  |
|----------------------|---|-------------------|-------------------|-------------------------------------|------|-------|--|
| Parameter            | Description                               | Min. <sup>1</sup> | Max. <sup>2</sup> | Min. <sup>1</sup> Max. <sup>2</sup> |      | Units |  |
| t <sub>RCKL</sub>    | Input LOW Delay for Global Clock          | 1.81              | 2.09              | 2.13                                | 2.42 | ns    |  |
| t <sub>RCKH</sub>    | Input HIGH Delay for Global Clock         | 1.80              | 2.13              | 2.12                                | 2.45 | ns    |  |
| t <sub>RCKMPWH</sub> | Minimum Pulse Width HIGH for Global Clock |                   |                   |                                     |      | ns    |  |
| t <sub>RCKMPWL</sub> | Minimum Pulse Width LOW for Global Clock  |                   |                   |                                     |      | ns    |  |
| t <sub>RCKSW</sub>   | Maximum Skew for Global Clock             |                   | 0.32              |                                     | 0.38 | ns    |  |
| F <sub>RMAX</sub>    | Maximum Frequency for Global Clock        |                   |                   |                                     |      | MHz   |  |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

<sup>2.</sup> Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

<sup>3.</sup> For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### GL Globals

FF

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs " chapter of the *Military ProASIC3/EL FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter (for A3P250 and A3P1000) or "I/O Structures in IGLOOe and ProASIC3E Devices" (for A3PE600L and A3PE3000L) of the *Military ProASIC3/EL FPGA Fabric User's Guide* for an explanation of the naming of global pins.

### Flash\*Freeze Mode Activation Pin

Flash\*Freeze is available on A3PE600L and A3PE3000L devices. The FF pin is a dedicated input pin used to enter and exit Flash\*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash\*Freeze mode is not used in the design, the FF pin is available as a regular I/O. The FF pin can be configured as a Schmitt trigger input.

When Flash\*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash\*Freeze mode. While in Flash\*Freeze mode, the Flash\*Freeze pin should be constantly asserted.

The Flash\*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash\*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash\*Freeze pin location on the available packages for Military ProASIC3/EL devices. The Flash\*Freeze pin location is independent of device, allowing migration to larger or smaller devices while maintaining the same pin location on the board. Refer to the "Flash\*Freeze Technology and Low Power Modes" chapter of the *Military ProASIC3/EL FPGA Fabric User Guide* for more information on I/O states during Flash\*Freeze mode.

| Military ProASIC3/EL Packages | Flash*Freeze Pin |
|-------------------------------|------------------|
| FG484                         | W6               |
| FG896                         | AH4              |

Table 3-1 • Flash\*Freeze Pin Location in Military ProASIC3/EL Packages (device-independent)



## FG144



Note: This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/products/fpga-soc/solutions.



Note: This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/products/fpga-soc/solutions.

|               | FG484            |               | FG484            |
|---------------|------------------|---------------|------------------|
| Pin<br>Number | A3P1000 Function | Pin<br>Number | A3P1000 Function |
| Y3            | NC               | AA16          | IO122RSB2        |
| Y4            | IO182RSB2        | AA17          | IO119RSB2        |
| Y5            | GND              | AA18          | IO117RSB2        |
| Y6            | IO177RSB2        | AA19          | NC               |
| Y7            | IO174RSB2        | AA20          | NC               |
| Y8            | VCC              | AA21          | VCCIB1           |
| Y9            | VCC              | AA22          | GND              |
| Y10           | IO154RSB2        | AB1           | GND              |
| Y11           | IO148RSB2        | AB2           | GND              |
| Y12           | IO140RSB2        | AB3           | VCCIB2           |
| Y13           | NC               | AB4           | IO180RSB2        |
| Y14           | VCC              | AB5           | IO176RSB2        |
| Y15           | VCC              | AB6           | IO173RSB2        |
| Y16           | NC               | AB7           | IO167RSB2        |
| Y17           | NC               | AB8           | IO162RSB2        |
| Y18           | GND              | AB9           | IO156RSB2        |
| Y19           | NC               | AB10          | IO150RSB2        |
| Y20           | NC               | AB11          | IO145RSB2        |
| Y21           | NC               | AB12          | IO144RSB2        |
| Y22           | VCCIB1           | AB13          | IO132RSB2        |
| AA1           | GND              | AB14          | IO127RSB2        |
| AA2           | VCCIB3           | AB15          | IO126RSB2        |
| AA3           | NC               | AB16          | IO123RSB2        |
| AA4           | IO181RSB2        | AB17          | IO121RSB2        |
| AA5           | IO178RSB2        | AB18          | IO118RSB2        |
| AA6           | IO175RSB2        | AB19          | NC               |
| AA7           | IO169RSB2        | AB20          | VCCIB2           |
| AA8           | IO166RSB2        | AB21          | GND              |
| AA9           | IO160RSB2        | AB22          | GND              |
| AA10          | IO152RSB2        |               |                  |
| AA11          | IO146RSB2        |               |                  |
| AA12          | IO139RSB2        |               |                  |
| AA13          | IO133RSB2        |               |                  |
| AA14          | NC               |               |                  |

AA15

NC



Package Pin Assignments

| FG484         |                    |               | FG484              | FG484         |                    |  |
|---------------|--------------------|---------------|--------------------|---------------|--------------------|--|
| Pin<br>Number | A3PE3000L Function | Pin<br>Number | A3PE3000L Function | Pin<br>Number | A3PE3000L Function |  |
| A1            | GND                | AA14          | IO170NDB4V2        | B5            | IO08PDB0V0         |  |
| A2            | GND                | AA15          | IO170PDB4V2        | B6            | IO14NDB0V1         |  |
| A3            | VCCIB0             | AA16          | IO166NDB4V1        | B7            | IO14PDB0V1         |  |
| A4            | IO10NDB0V1         | AA17          | IO166PDB4V1        | B8            | IO18NDB0V2         |  |
| A5            | IO10PDB0V1         | AA18          | IO160NDB4V0        | B9            | IO24NDB0V2         |  |
| A6            | IO16NDB0V1         | AA19          | IO160PDB4V0        | B10           | IO34PDB0V4         |  |
| A7            | IO16PDB0V1         | AA20          | IO158NPB4V0        | B11           | IO40PDB0V4         |  |
| A8            | IO18PDB0V2         | AA21          | VCCIB3             | B12           | IO46NDB1V0         |  |
| A9            | IO24PDB0V2         | AA22          | GND                | B13           | IO54NDB1V1         |  |
| A10           | IO28NDB0V3         | AB1           | GND                | B14           | IO62NDB1V2         |  |
| A11           | IO28PDB0V3         | AB2           | GND                | B15           | IO62PDB1V2         |  |
| A12           | IO46PDB1V0         | AB3           | VCCIB5             | B16           | IO68NDB1V3         |  |
| A13           | IO54PDB1V1         | AB4           | IO216NDB5V2        | B17           | IO68PDB1V3         |  |
| A14           | IO56NDB1V1         | AB5           | IO216PDB5V2        | B18           | IO72PDB1V3         |  |
| A15           | IO56PDB1V1         | AB6           | IO210NDB5V2        | B19           | IO74PDB1V4         |  |
| A16           | IO64NDB1V2         | AB7           | IO210PDB5V2        | B20           | IO76NPB1V4         |  |
| A17           | IO64PDB1V2         | AB8           | IO208NDB5V1        | B21           | VCCIB2             |  |
| A18           | IO72NDB1V3         | AB9           | IO208PDB5V1        | B22           | GND                |  |
| A19           | IO74NDB1V4         | AB10          | IO197NDB5V0        | C1            | VCCIB7             |  |
| A20           | VCCIB1             | AB11          | IO197PDB5V0        | C2            | IO303PDB7V3        |  |
| A21           | GND                | AB12          | IO174NDB4V2        | C3            | IO305PDB7V3        |  |
| A22           | GND                | AB13          | IO174PDB4V2        | C4            | IO06NPB0V0         |  |
| AA1           | GND                | AB14          | IO172NDB4V2        | C5            | GND                |  |
| AA2           | VCCIB6             | AB15          | IO172PDB4V2        | C6            | IO12NDB0V1         |  |
| AA3           | IO228PDB5V4        | AB16          | IO168NDB4V1        | C7            | IO12PDB0V1         |  |
| AA4           | IO224PDB5V3        | AB17          | IO168PDB4V1        | C8            | VCC                |  |
| AA5           | IO218NDB5V3        | AB18          | IO162NDB4V1        | C9            | VCC                |  |
| AA6           | IO218PDB5V3        | AB19          | IO162PDB4V1        | C10           | IO34NDB0V4         |  |
| AA7           | IO212NDB5V2        | AB20          | VCCIB4             | C11           | IO40NDB0V4         |  |
| AA8           | IO212PDB5V2        | AB21          | GND                | C12           | IO48NDB1V0         |  |
| AA9           | IO198PDB5V0        | AB22          | GND                | C13           | IO48PDB1V0         |  |
| AA10          | IO198NDB5V0        | B1            | GND                | C14           | VCC                |  |
| AA11          | IO188PPB4V4        | B2            | VCCIB7             | C15           | VCC                |  |
| AA12          | IO180NDB4V3        | B3            | IO06PPB0V0         | C16           | IO70NDB1V3         |  |
| AA13          | IO180PDB4V3        | B4            | IO08NDB0V0         | C17           | IO70PDB1V3         |  |



Package Pin Assignments

| FG484         |                    | FG484         |                    | FG484         |                    |
|---------------|--------------------|---------------|--------------------|---------------|--------------------|
| Pin<br>Number | A3PE3000L Function | Pin<br>Number | A3PE3000L Function | Pin<br>Number | A3PE3000L Function |
| H13           | VCCIB1             | K4            | IO279NDB7V0        | L17           | GCA0/IO114NPB3V0   |
| H14           | VCCIB1             | K5            | IO283NDB7V1        | L18           | VCOMPLC            |
| H15           | VMV1               | K6            | IO281NDB7V0        | L19           | GCB0/IO113NPB2V3   |
| H16           | GBC2/IO84PDB2V0    | K7            | GFC1/IO275PPB7V0   | L20           | IO110PPB2V3        |
| H17           | IO83NDB2V0         | K8            | VCCIB7             | L21           | IO111NDB2V3        |
| H18           | IO100NDB2V2        | K9            | VCC                | L22           | IO111PDB2V3        |
| H19           | IO100PDB2V2        | K10           | GND                | M1            | GNDQ               |
| H20           | VCC                | K11           | GND                | M2            | IO255NPB6V2        |
| H21           | VMV2               | K12           | GND                | M3            | IO272NDB6V4        |
| H22           | IO105PDB2V2        | K13           | GND                | M4            | GFA2/IO272PDB6V4   |
| J1            | IO285NDB7V1        | K14           | VCC                | M5            | GFA1/IO273PDB6V4   |
| J2            | IO285PDB7V1        | K15           | VCCIB2             | M6            | VCCPLF             |
| J3            | VMV7               | K16           | GCC1/IO112PPB2V3   | M7            | IO271NDB6V4        |
| J4            | IO279PDB7V0        | K17           | IO108NDB2V3        | M8            | GFB2/IO271PDB6V4   |
| J5            | IO283PDB7V1        | K18           | IO108PDB2V3        | M9            | VCC                |
| J6            | IO281PDB7V0        | K19           | IO110NPB2V3        | M10           | GND                |
| J7            | IO287NDB7V1        | K20           | IO106NPB2V3        | M11           | GND                |
| J8            | VCCIB7             | K21           | IO109NDB2V3        | M12           | GND                |
| J9            | GND                | K22           | IO107NDB2V3        | M13           | GND                |
| J10           | VCC                | L1            | IO257PSB6V2        | M14           | VCC                |
| J11           | VCC                | L2            | IO276PDB7V0        | M15           | GCB2/IO116PPB3V0   |
| J12           | VCC                | L3            | IO276NDB7V0        | M16           | GCA1/IO114PPB3V0   |
| J13           | VCC                | L4            | GFB0/IO274NPB7V0   | M17           | GCC2/IO117PPB3V0   |
| J14           | GND                | L5            | GFA0/IO273NDB6V4   | M18           | VCCPLC             |
| J15           | VCCIB2             | L6            | GFB1/IO274PPB7V0   | M19           | GCA2/IO115PDB3V0   |
| J16           | IO84NDB2V0         | L7            | VCOMPLF            | M20           | IO115NDB3V0        |
| J17           | IO104NDB2V2        | L8            | GFC0/IO275NPB7V0   | M21           | IO126PDB3V1        |
| J18           | IO104PDB2V2        | L9            | VCC                | M22           | IO124PSB3V1        |
| J19           | IO106PPB2V3        | L10           | GND                | N1            | IO255PPB6V2        |
| J20           | GNDQ               | L11           | GND                | N2            | IO253NDB6V2        |
| J21           | IO109PDB2V3        | L12           | GND                | N3            | VMV6               |
| J22           | IO107PDB2V3        | L13           | GND                | N4            | GFC2/IO270PPB6V4   |
| K1            | IO277NDB7V0        | L14           | VCC                | N5            | IO261PPB6V3        |
| K2            | IO277PDB7V0        | L15           | GCC0/IO112NPB2V3   | N6            | IO263PDB6V3        |
| K3            | GNDQ               | L16           | GCB1/IO113PPB2V3   | N7            | IO263NDB6V3        |





Note: This is the bottom view.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/products/fpga-soc/solutions.



| FG896      |                    |  |  |  |  |
|------------|--------------------|--|--|--|--|
| Pin Number | A3PE3000L Function |  |  |  |  |
| H26        | IO84NDB2V0         |  |  |  |  |
| H27        | IO96PDB2V1         |  |  |  |  |
| H28        | IO96NDB2V1         |  |  |  |  |
| H29        | IO89PDB2V0         |  |  |  |  |
| H30        | IO89NDB2V0         |  |  |  |  |
| J1         | IO290NDB7V2        |  |  |  |  |
| J2         | IO290PDB7V2        |  |  |  |  |
| J3         | IO302NDB7V3        |  |  |  |  |
| J4         | IO302PDB7V3        |  |  |  |  |
| J5         | IO295NDB7V2        |  |  |  |  |
| J6         | IO299NDB7V3        |  |  |  |  |
| J7         | VCCIB7             |  |  |  |  |
| J8         | VCCPLA             |  |  |  |  |
| J9         | VCC                |  |  |  |  |
| J10        | IO04NPB0V0         |  |  |  |  |
| J11        | IO18NDB0V2         |  |  |  |  |
| J12        | IO20NDB0V2         |  |  |  |  |
| J13        | IO20PDB0V2         |  |  |  |  |
| J14        | IO32NDB0V3         |  |  |  |  |
| J15        | IO32PDB0V3         |  |  |  |  |
| J16        | IO42PDB1V0         |  |  |  |  |
| J17        | IO44NDB1V0         |  |  |  |  |
| J18        | IO44PDB1V0         |  |  |  |  |
| J19        | IO54NDB1V1         |  |  |  |  |
| J20        | IO54PDB1V1         |  |  |  |  |
| J21        | IO76NPB1V4         |  |  |  |  |
| J22        | VCC                |  |  |  |  |
| J23        | VCCPLB             |  |  |  |  |
| J24        | VCCIB2             |  |  |  |  |
| J25        | IO90PDB2V1         |  |  |  |  |
| J26        | IO90NDB2V1         |  |  |  |  |
| J27        | GBB2/IO83PDB2V0    |  |  |  |  |
| J28        | IO83NDB2V0         |  |  |  |  |
| J29        | IO91PDB2V1         |  |  |  |  |
| J30        | IO91NDB2V1         |  |  |  |  |
| K1         | IO288NDB7V1        |  |  |  |  |