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Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fg484m

Table 2-28 •   **Summary of Maximum and Minimum DC Input Levels**
             Applicable to Military Conditions

DC I/O Standard	Military[1]	
	I_{IL}[2]	I_{IH}[3]
	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	15	15
3.3 V LVCMOS Wide Range	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS[4]	15	15
1.2 V LVCMOS Wide Range[4]	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1.   *Military temperature range: –55°C to 125°C.*

2.   *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

3.   *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

4.   *Applicable to Military A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.*

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-44 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–50ºC	> 20 years
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	1 month

Table 2-45 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: **The maximum input rise/fall time is related to the noise induced in the input buffer trace. If the noise is low, the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-46 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-47 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
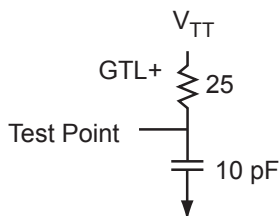5. Software default selection highlighted in gray.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-128 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	268	181	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.

2. II_H is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 125°C junction temperature.

Figure 2-17 • **AC Loading**

Table 2-129 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-130 • **3.3 V GTL+**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.04	0.05	2.34	0.52	2.07	2.03	–	–	4.28	4.24	ns
–1	0.68	1.74	0.05	1.99	0.44	1.76	1.73	–	–	3.64	3.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-131 • **3.3 V GTL+**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.95	0.04	2.11	0.40	1.92	1.95	–	–	3.38	3.41	ns
–1	0.52	1.66	0.03	1.79	0.34	1.63	1.66	–	–	2.88	2.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-139 • HSTL Class I
    Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V,
    Worst-Case VCCI = 1.4 V, VREF = 0.75 V
    Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
Std.	0.61	3.02	0.04	2.52	0.40	3.05	3.00	–	–	4.51	4.46	ns
−1	0.52	2.57	0.03	2.14	0.34	2.59	2.55	–	–	3.84	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

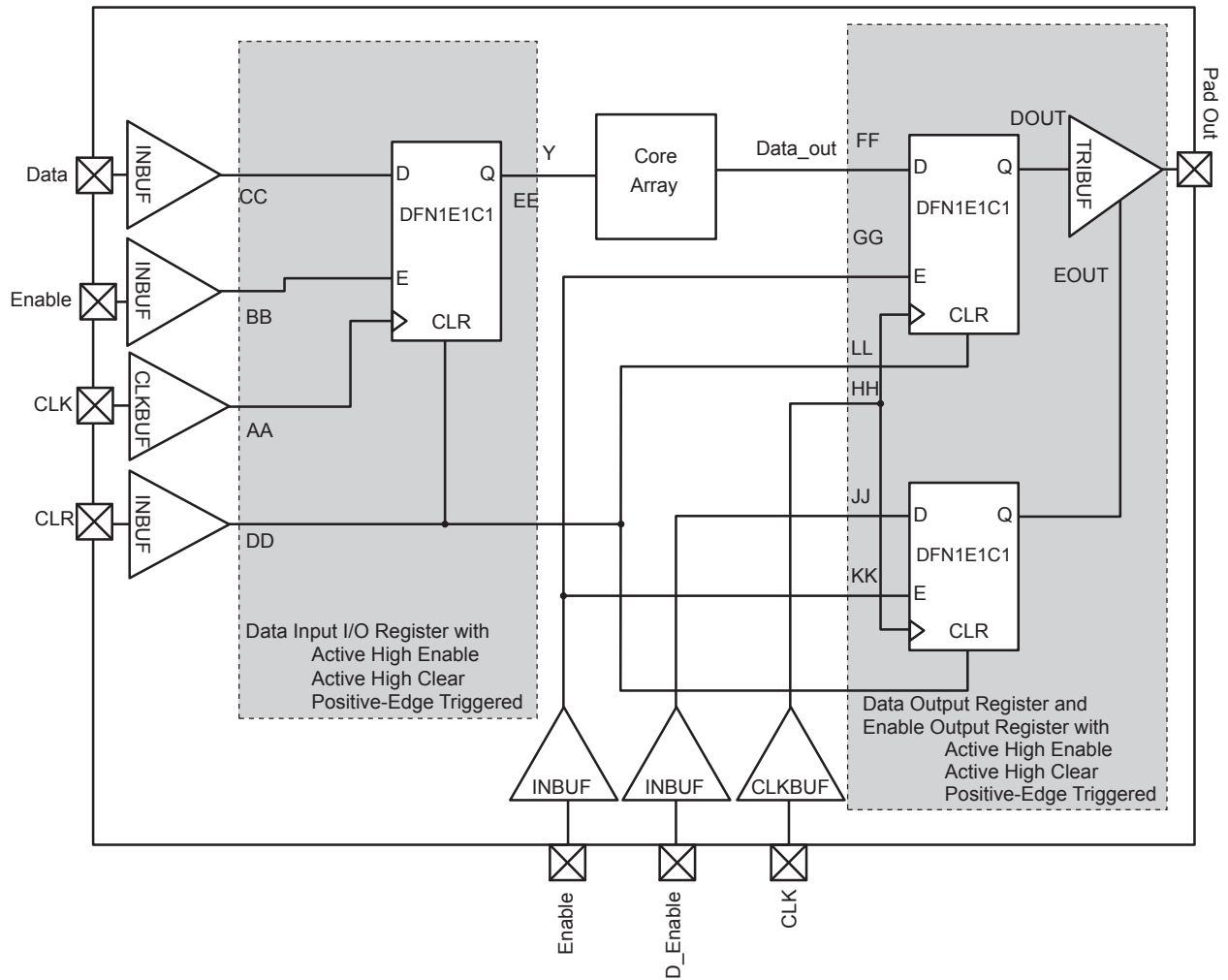### *Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear*

Figure 2-29 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-177 • **Output Data Register Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t$_{OCLKQ}$	Clock-to-Q of the Output Data Register	0.71	0.83	ns
t$_{OSUD}$	Data Setup Time for the Output Data Register	0.38	0.44	ns
t$_{OHD}$	Data Hold Time for the Output Data Register	0.00	0.00	ns
t$_{OSUE}$	Enable Setup Time for the Output Data Register	0.53	0.62	ns
t$_{OHE}$	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t$_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	0.97	1.14	ns
t$_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	0.97	1.14	ns
t$_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t$_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t$_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t$_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t$_{OWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t$_{OWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t$_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
t$_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

Table 2-178 • **Output Enable Register Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	−1	Std.	Units
t$_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.62	0.72	ns
t$_{OESUD}$	Data Setup Time for the Output Enable Register	0.43	0.51	ns
t$_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t$_{OESUE}$	Enable Setup Time for the Output Enable Register	0.60	0.71	ns
t$_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
t$_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.92	1.08	ns
t$_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.92	1.08	ns
t$_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
t$_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.31	0.36	ns
t$_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
t$_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.31	0.36	ns
t$_{OEWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t$_{OEWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t$_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
t$_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-179 • **Output Enable Register Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	−1	Std.	Units
t$_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.47	0.55	ns
t$_{OESUD}$	Data Setup Time for the Output Enable Register	0.33	0.39	ns
t$_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t$_{OESUE}$	Enable Setup Time for the Output Enable Register	0.46	0.54	ns
t$_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
t$_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.83	ns
t$_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.83	ns
t$_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
t$_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
t$_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
t$_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
t$_{OEWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t$_{OEWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t$_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
t$_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-193 • **Register Delays**
        Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t$_{CLKQ}$	Clock-to-Q of the Core Register	0.58	0.69	ns
t$_{SUD}$	Data Setup Time for the Core Register	0.45	0.53	ns
t$_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
t$_{SUE}$	Enable Setup Time for the Core Register	0.48	0.57	ns
t$_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
t$_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.42	0.50	ns
t$_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.42	0.50	ns
t$_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t$_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
t$_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t$_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
t$_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t$_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t$_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t$_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
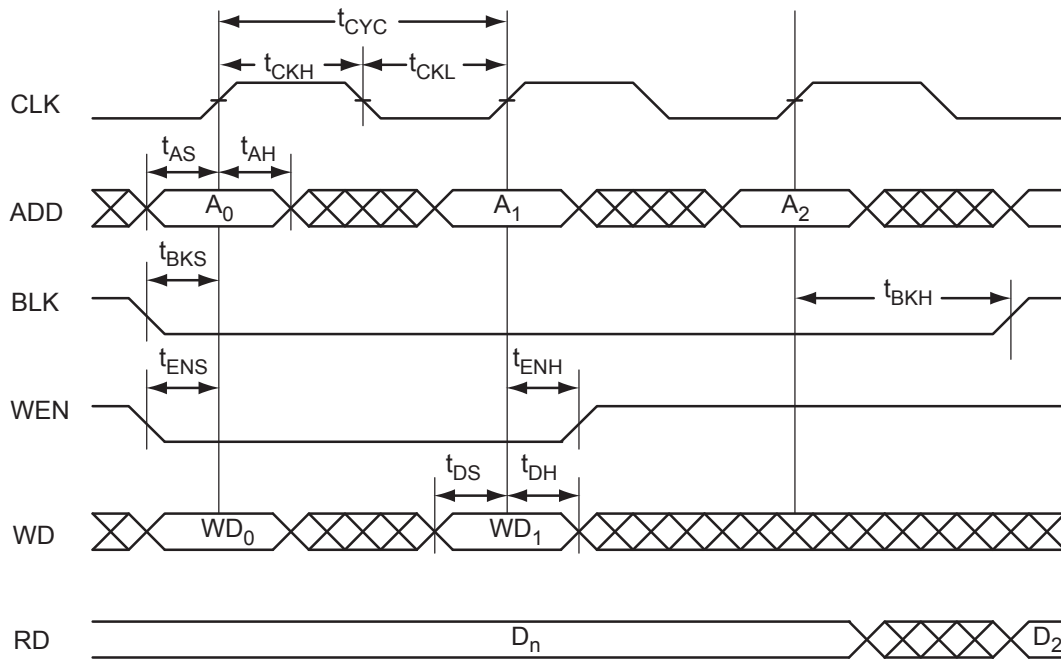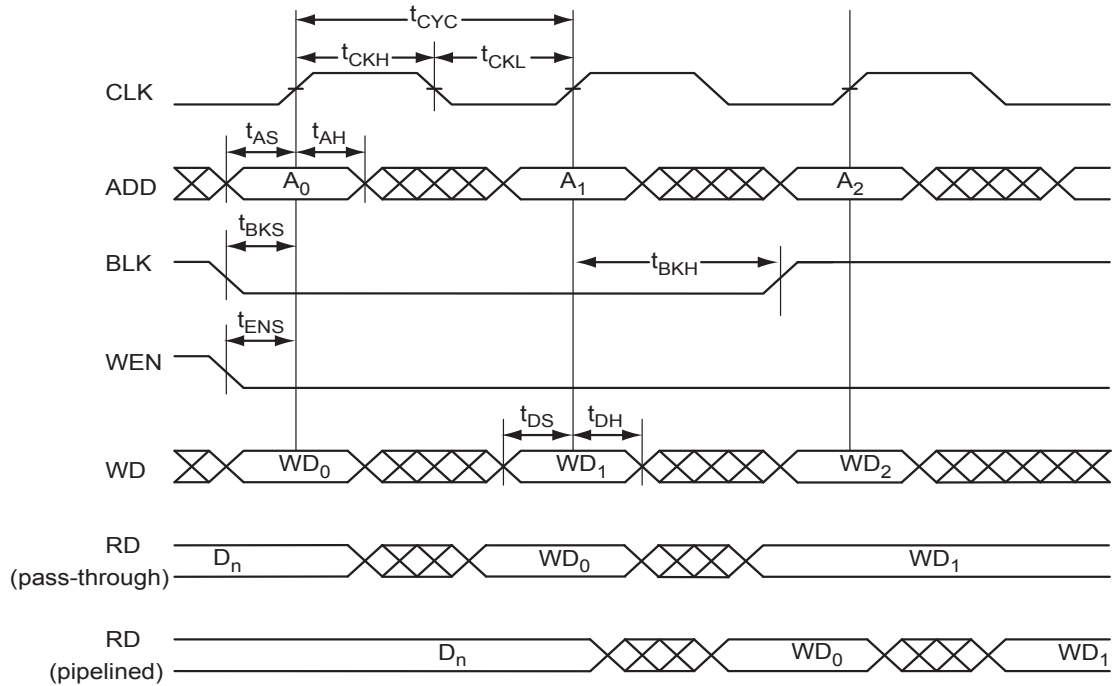
Figure 2-46 • **RAM Write, Output Retained (WMODE = 0)**

Figure 2-47 • **RAM Write, Output as Write Data (WMODE = 1)**

Table 2-204 • RAM4K9
Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t$_{AS}$	Address setup time	0.26	0.31	ns
t$_{AH}$	Address hold time	0.00	0.00	ns
t$_{ENS}$	REN, WEN setup time	0.15	0.18	ns
t$_{ENH}$	REN, WEN hold time	0.10	0.12	ns
t$_{BKS}$	BLK setup time	0.25	0.29	ns
t$_{BKH}$	BLK hold time	0.02	0.02	ns
t$_{DS}$	Input data (DIN) setup time	0.19	0.23	ns
t$_{DH}$	Input data (DIN) hold time	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	2.50	2.93	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	1.89	2.22	ns
t$_{CKQ2}$	Clock HIGH to new data valid on DOUT (pipelined)	0.95	1.11	ns
t$_{C2CWWL}$	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.24	0.29	ns
t$_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.20	0.24	ns
t$_{C2CRWH}$	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.25	0.30	ns
t$_{RSTBQ}$	RESET Low to data out Low on DOUT (flow-through)	0.98	1.15	ns
	RESET Low to data out Low on DOUT (pipelined)	0.98	1.15	ns
t$_{REMRSTB}$	RESET removal	0.30	0.36	ns
t$_{RECRSTB}$	RESET recovery	1.59	1.87	ns
t$_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t$_{CYC}$	Clock cycle time	5.39	6.20	ns
F$_{MAX}$	Maximum frequency	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-205 • **RAM4K9**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t$_{AS}$	Address setup time	0.30	0.35	ns
t$_{AH}$	Address hold time	0.00	0.00	ns
t$_{ENS}$	REN, WEN setup time	0.17	0.20	ns
t$_{ENH}$	REN, WEN hold time	0.12	0.14	ns
t$_{BKS}$	BLK setup time	0.28	0.33	ns
t$_{BKH}$	BLK hold time	0.02	0.03	ns
t$_{DS}$	Input data (DIN) setup time	0.22	0.26	ns
t$_{DH}$	Input data (DIN) hold time	0.00	0.00	ns
t$_{CKQ1}$	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.84	2.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.15	3.33	ns
t$_{CKQ2}$	Clock High to new data valid on DOUT (pipelined)	1.08	1.27	ns
t$_{C2CWWL}$	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.28	0.33	ns
t$_{C2CWWH}$	Address collision clk-to-clk delay for reliable write after write on same address – applicable to rising edge	0.26	0.30	ns
t$_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.38	0.45	ns
t$_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.42	0.49	ns
t$_{RSTBQ}$	RESET Low to data out Low on DOUT (flow-through)	1.11	1.31	ns
	RESET Low to data out Low on DOUT (pipelined)	1.11	1.31	ns
t$_{REMRSTB}$	RESET removal	0.34	0.40	ns
t$_{RECRSTB}$	RESET recovery	1.81	2.12	ns
t$_{MPWRSTB}$	RESET minimum pulse width	0.26	0.30	ns
t$_{CYC}$	Clock cycle time	3.89	4.57	ns
F$_{MAX}$	Maximum frequency	257	219	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-207 • **RAM512X18**
Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t$_{AS}$	Address setup time	0.26	0.31	ns
t$_{AH}$	Address hold time	0.00	0.00	ns
t$_{ENS}$	REN, WEN setup time	0.10	0.11	ns
t$_{ENH}$	REN, WEN hold time	0.06	0.07	ns
t$_{DS}$	Input data (WD) setup time	0.19	0.23	ns
t$_{DH}$	Input data (WD) hold time	0.00	0.00	ns
t$_{CKQ1}$	Clock High to new data valid on RD (output retained, WMODE = 0)	2.29	2.69	ns
t$_{CKQ2}$	Clock High to new data valid on RD (pipelined)	0.95	1.12	ns
t$_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t$_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t$_{RSTBQ}$	RESET Low to data out Low on RD (flow through)	0.98	1.15	ns
	RESET Low to data out Low on RD (pipelined)	0.98	1.15	ns
t$_{REMRSTB}$	RESET removal	0.30	0.36	ns
t$_{RECRSTB}$	RESET recovery	1.59	1.87	ns
t$_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t$_{CYC}$	Clock cycle time	5.39	6.20	ns
F$_{MAX}$	Maximum frequency	185	161	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
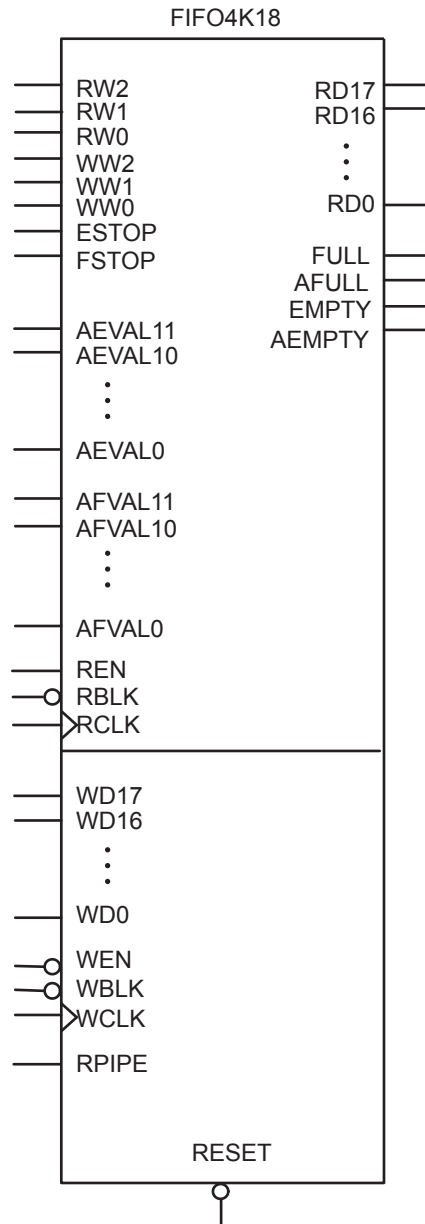
FIFO

Figure 2-49 • **FIFO Model**

Table 2-212 • **FIFO Worst Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3P250 (256×16)**

Parameter	Description	–1	Std.	Units
t$_{ENS}$	REN, WEN Setup Time	3.92	4.61	ns
t$_{ENH}$	REN, WEN Hold Time	0.00	0.00	ns
t$_{BKS}$	BLK Setup Time	1.66	1.95	ns
t$_{BKH}$	BLK Hold Time	0.00	0.00	ns
t$_{DS}$	Input Data (WD) Setup Time	0.22	0.26	ns
t$_{DH}$	Input Data (WD) Hold Time	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on RD (flow-through)	2.61	3.06	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on RD (pipelined)	1.14	1.34	ns
t$_{RCKEF}$	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t$_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t$_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t$_{RSTFG}$	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t$_{RSTAF}$	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t$_{RSTBQ}$	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t$_{REMRSTB}$	RESET Removal	0.34	0.40	ns
t$_{RECRSTB}$	RESET Recovery	1.81	2.12	ns
t$_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t$_{CYC}$	Clock Cycle Time	3.89	4.57	ns
F$_{MAX}$	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

FG144	
Pin Number	**A3P1000 Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484			FG484			FG484	
Pin Number	**A3PE3000L Function**		**Pin Number**	**A3PE3000L Function**		**Pin Number**	**A3PE3000L Function**
C18	GND		E9	IO22NDB0V2		F22	IO98NDB2V2
C19	IO76PPB1V4		E10	IO30NDB0V3		G1	IO289NDB7V1
C20	IO88NDB2V0		E11	IO38PDB0V4		G2	IO289PDB7V1
C21	IO94PPB2V1		E12	IO44NDB1V0		G3	IO291PPB7V2
C22	VCCIB2		E13	IO58NDB1V2		G4	IO295PDB7V2
D1	IO293PDB7V2		E14	IO58PDB1V2		G5	IO297PDB7V2
D2	IO303NDB7V3		E15	GBC1/IO79PDB1V4		G6	GAC2/IO307PDB7V4
D3	IO305NDB7V3		E16	GBB0/IO80NDB1V4		G7	VCOMPLA
D4	GND		E17	GNDQ		G8	GNDQ
D5	GAA0/IO00NDB0V0		E18	GBA2/IO82PDB2V0		G9	IO26NDB0V3
D6	GAA1/IO00PDB0V0		E19	IO86NDB2V0		G10	IO26PDB0V3
D7	GAB0/IO01NDB0V0		E20	GND		G11	IO36PDB0V4
D8	IO20PDB0V2		E21	IO90NDB2V1		G12	IO42PDB1V0
D9	IO22PDB0V2		E22	IO98PDB2V2		G13	IO50PDB1V1
D10	IO30PDB0V3		F1	IO299NPB7V3		G14	IO60NDB1V2
D11	IO38NDB0V4		F2	IO301NDB7V3		G15	GNDQ
D12	IO52NDB1V1		F3	IO301PDB7V3		G16	VCOMPLB
D13	IO52PDB1V1		F4	IO308NDB7V4		G17	GBB2/IO83PDB2V0
D14	IO66NDB1V3		F5	IO309NDB7V4		G18	IO92PDB2V1
D15	IO66PDB1V3		F6	VMV7		G19	IO92NDB2V1
D16	GBB1/IO80PDB1V4		F7	VCCPLA		G20	IO102PDB2V2
D17	GBA0/IO81NDB1V4		F8	GAC0/IO02NDB0V0		G21	IO102NDB2V2
D18	GBA1/IO81PDB1V4		F9	GAC1/IO02PDB0V0		G22	IO105NDB2V2
D19	GND		F10	IO32NDB0V3		H1	IO286PSB7V1
D20	IO88PDB2V0		F11	IO32PDB0V3		H2	IO291NPB7V2
D21	IO90PDB2V1		F12	IO44PDB1V0		H3	VCC
D22	IO94NPB2V1		F13	IO50NDB1V1		H4	IO295NDB7V2
E1	IO293NDB7V2		F14	IO60PDB1V2		H5	IO297NDB7V2
E2	IO299PPB7V3		F15	GBC0/IO79NDB1V4		H6	IO307NDB7V4
E3	GND		F16	VCCPLB		H7	IO287PDB7V1
E4	GAB2/IO308PDB7V4		F17	VMV2		H8	VMV0
E5	GAA2/IO309PDB7V4		F18	IO82NDB2V0		H9	VCCIB0
E6	GNDQ		F19	IO86PDB2V0		H10	VCCIB0
E7	GAB1/IO01PDB0V0		F20	IO96PDB2V1		H11	IO36NDB0V4
E8	IO20NDB0V2		F21	IO96NDB2V1		H12	IO42NDB1V0

FG484		FG484		FG484	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
N8	VCCIB6	P21	IO130PDB3V2	T12	IO194NDB5V0
N9	VCC	P22	IO128NDB3V1	T13	IO186NDB4V4
N10	GND	R1	IO247NDB6V1	T14	IO186PDB4V4
N11	GND	R2	IO245PDB6V1	T15	GNDQ
N12	GND	R3	VCC	T16	VCOMPLD
N13	GND	R4	IO249NPB6V1	T17	VJTAG
N14	VCC	R5	IO251NDB6V2	T18	GDC0/IO151NDB3V4
N15	VCCIB3	R6	IO251PDB6V2	T19	GDA1/IO153PDB3V4
N16	IO116NPB3V0	R7	GEC0/IO236NPB6V0	T20	IO144PDB3V3
N17	IO132NPB3V2	R8	VMV5	T21	IO140PDB3V3
N18	IO117NPB3V0	R9	VCCIB5	T22	IO134NDB3V2
N19	IO132PPB3V2	R10	VCCIB5	U1	IO240PPB6V0
N20	GNDQ	R11	IO196NDB5V0	U2	IO238PDB6V0
N21	IO126NDB3V1	R12	IO196PDB5V0	U3	IO238NDB6V0
N22	IO128PDB3V1	R13	VCCIB4	U4	GEB1/IO235PDB6V0
P1	IO247PDB6V1	R14	VCCIB4	U5	GEB0/IO235NDB6V0
P2	IO253PDB6V2	R15	VMV3	U6	VMV6
P3	IO270NPB6V4	R16	VCCPLD	U7	VCCPLE
P4	IO261NPB6V3	R17	GDB1/IO152PPB3V4	U8	IO233NPB5V4
P5	IO249PPB6V1	R18	GDC1/IO151PDB3V4	U9	IO222PPB5V3
P6	IO259PDB6V3	R19	IO138NDB3V3	U10	IO206PDB5V1
P7	IO259NDB6V3	R20	VCC	U11	IO202PDB5V1
P8	VCCIB6	R21	IO130NDB3V2	U12	IO194PDB5V0
P9	GND	R22	IO134PDB3V2	U13	IO176NDB4V2
P10	VCC	T1	IO243PPB6V1	U14	IO176PDB4V2
P11	VCC	T2	IO245NDB6V1	U15	VMV4
P12	VCC	T3	IO243NPB6V1	U16	TCK
P13	VCC	T4	IO241PDB6V0	U17	VPUMP
P14	GND	T5	IO241NDB6V0	U18	TRST
P15	VCCIB3	T6	GEC1/IO236PPB6V0	U19	GDA0/IO153NDB3V4
P16	GDB0/IO152NPB3V4	T7	VCOMPLE	U20	IO144NDB3V3
P17	IO136NDB3V2	T8	GNDQ	U21	IO140NDB3V3
P18	IO136PDB3V2	T9	GEA2/IO233PPB5V4	U22	IO142PDB3V3
P19	IO138PDB3V3	T10	IO206NDB5V1	V1	IO239PDB6V0
P20	VMV3	T11	IO202NDB5V1	V2	IO240NPB6V0

FG896	
Pin Number	A3PE3000L Function
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST

FG896	
Pin Number	A3PE3000L Function
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC

FG896	
Pin Number	A3PE3000L Function
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND

FG896	
Pin Number	A3PE3000L Function
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND