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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fgg256m

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-23 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-24 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}[2]	I_{OH}[2]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[1,3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS[4,5]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[1,4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA[6]	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[6]	20 mA	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[6]	15 mA[6]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength These values are for normal ranges only.*
2. *Currents are measured at 125°C junction temperature.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
6. *Output drive strength is below JEDEC specification.*
7. *Output slew rate can be extracted using the IBIS Models.*

Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Military-Case Conditions: TJ = 125°C, Worst Case VCC = 1.425 V, Worst Case VCCI Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)[2]	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	5	–	0.54	2.94	0.04	1.42	0.39	2.94	2.22	4.03	4.66	6.12	5.40
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.8 V LVCMOS	8 mA	8 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.5 V LVCMOS	4 mA	4 mA	High	5	–	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32
3.3 V PCI	Per PCI spec.	–	High	10	25 [4]	0.54	2.16	0.04	0.80	0.39	2.20	1.60	2.61	3.01	4.29	3.69
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25 [4]	0.54	2.16	0.04	0.78	0.39	2.20	1.60	2.61	3.01	4.29	3.69

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software. Software default load is higher.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-14 on page 2-71 for connectivity. This resistor is not required during normal operation.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Detailed I/O DC Characteristics

Table 2-35 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	6.25	0.05	1.12	0.45	6.37	5.29	2.91	2.70	8.83	7.75	ns
	–1	0.54	5.32	0.04	0.95	0.39	5.42	4.50	2.47	2.30	7.51	6.59	ns
6 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	–1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
8 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	–1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
12 mA	Std.	0.63	4.50	0.05	1.12	0.45	4.59	4.05	3.53	3.76	7.05	6.51	ns
	–1	0.54	3.83	0.04	0.95	0.39	3.90	3.45	3.00	3.20	5.99	5.54	ns
16 mA	Std.	0.63	4.27	0.05	1.12	0.45	4.35	3.93	3.58	3.86	6.81	6.39	ns
	–1	0.54	3.63	0.04	0.95	0.39	3.70	3.34	3.05	3.29	5.79	5.43	ns
24 mA	Std.	0.63	4.14	0.05	1.12	0.45	4.22	3.97	3.65	4.27	6.68	6.43	ns
	–1	0.54	3.53	0.04	0.95	0.39	3.59	3.38	3.10	3.63	5.68	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.55	0.05	1.12	0.45	3.62	2.79	2.91	2.87	6.07	5.25	ns
	–1	0.54	3.02	0.04	0.95	0.39	3.08	2.37	2.48	2.44	5.17	4.46	ns
6 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	–1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
8 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	–1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
12 mA	Std.	0.63	2.64	0.05	1.12	0.45	2.68	1.99	3.53	3.94	5.14	4.45	ns
	–-1	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79	ns
16 mA	Std.	0.63	2.58	0.05	1.12	0.45	2.63	1.95	3.59	4.05	5.09	4.41	ns
	–-1	0.54	2.20	0.04	0.95	0.39	2.24	1.66	3.05	3.44	4.33	3.75	ns
24 mA	Std.	0.63	2.61	0.05	1.12	0.45	2.66	1.89	3.66	4.46	5.12	4.35	ns
	–1	0.54	2.22	0.04	0.95	0.39	2.26	1.61	3.11	3.80	4.35	3.70	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-66 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.63	9.67	0.05	1.70	0.45	9.67	8.03	4.50	4.18	13.40	11.77	ns
		–1	0.54	8.22	0.04	1.44	0.39	8.22	6.83	3.83	3.55	11.40	10.01	ns
100 µA	6mA	Std.	0.63	8.13	0.05	1.70	0.45	8.13	6.95	5.07	5.17	11.86	10.69	ns
		–1	0.54	6.91	0.04	1.44	0.39	6.91	5.92	4.31	4.40	10.09	9.09	ns
100 µA	8 mA	Std.	0.63	8.13	0.05	1.70	0.45	8.13	6.95	5.07	5.17	11.86	10.69	ns
		–1	0.54	6.91	0.04	1.44	0.39	6.91	5.92	4.31	4.40	10.09	9.09	ns
100 µA	12 mA	Std.	0.63	6.96	0.05	1.70	0.45	6.96	6.15	5.45	5.81	10.70	9.89	ns
		–1	0.54	5.92	0.04	1.44	0.39	5.92	5.24	4.64	4.94	9.10	8.41	ns
100 µA	16 mA	Std.	0.63	6.61	0.05	1.70	0.45	6.61	5.96	5.54	5.97	10.34	9.70	ns
		–1	0.54	5.62	0.04	1.44	0.39	5.62	5.07	4.71	5.08	8.80	8.25	ns

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-67 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.63	5.49	0.05	1.70	0.45	5.49	4.23	4.51	4.44	9.22	7.97	ns
		–1	0.54	4.67	0.04	1.44	0.39	4.57	3.60	3.83	3.78	7.84	6.78	ns
100 µA	6 mA	Std.	0.63	4.56	0.05	1.70	0.45	4.56	3.42	5.08	5.45	8.29	7.15	ns
		–1	0.54	3.88	0.04	1.44	0.39	3.88	2.91	4.32	4.64	7.05	6.08	ns
100 µA	8 mA	Std.	0.63	4.56	0.05	1.70	0.45	4.56	3.42	5.08	5.45	8.29	7.15	ns
		–1	0.54	3.88	0.04	1.44	0.39	3.88	2.91	4.32	4.64	7.05	6.08	ns
100 µA	12 mA	Std.	0.63	4.08	0.05	1.70	0.45	4.08	3.03	5.46	6.09	7.81	6.76	ns
		–1	0.54	3.47	0.04	1.44	0.39	3.47	2.57	4.65	5.18	6.64	5.75	ns
100 µA	16 mA	Std.	0.63	4.00	0.05	1.70	0.45	4.00	2.96	5.55	6.26	7.73	6.69	ns
		–1	0.54	3.40	0.04	1.44	0.39	3.40	2.51	4.72	5.32	6.58	5.69	ns

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-78 • 2.5 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	7.07	0.05	1.44	0.45	7.20	6.32	2.95	2.43	9.66	8.78	ns
	–1	0.54	6.02	0.04	1.23	0.39	6.13	5.38	2.51	2.06	8.22	7.47	ns
6 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	–1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
8 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	–1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
12 mA	Std.	0.63	5.05	0.05	1.44	0.45	5.15	4.79	3.63	3.66	7.61	7.25	ns
	–1	0.54	4.30	0.04	1.23	0.39	4.38	4.07	3.09	3.11	6.47	6.17	ns
16 mA	Std.	0.63	4.78	0.05	1.44	0.45	4.86	4.65	3.70	3.78	7.32	7.10	ns
	–1	0.54	4.06	0.04	1.23	0.39	4.14	3.95	3.14	3.22	6.23	6.04	ns
24 mA	Std.	0.63	4.71	0.05	1.44	0.45	4.73	4.71	3.78	4.26	7.19	7.17	ns
	–1	0.54	4.01	0.04	1.23	0.39	4.03	4.01	3.21	3.62	6.12	6.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-79 • 2.5 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.63	0.05	1.44	0.45	3.70	3.34	2.94	2.53	6.16	5.80	ns
	–1	0.54	3.09	0.04	1.23	0.39	3.15	2.84	2.51	2.16	5.24	4.94	ns
6 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	–1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
8 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	–1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
12 mA	Std.	0.63	2.65	0.05	1.44	0.45	2.70	2.23	3.63	3.78	5.16	4.69	ns
	–1	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99	ns
16 mA	Std.	0.63	2.59	0.05	1.44	0.45	2.64	2.16	3.70	3.90	5.10	4.62	ns
	–1	0.54	2.21	0.04	1.23	0.39	2.25	1.83	3.15	3.32	4.34	3.93	ns
24 mA	Std.	0.63	2.61	0.05	1.44	0.45	2.66	2.08	3.78	4.40	5.12	4.54	ns
	–1	0.54	2.22	0.04	1.23	0.39	2.26	1.77	3.22	3.74	4.35	3.87	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-96 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

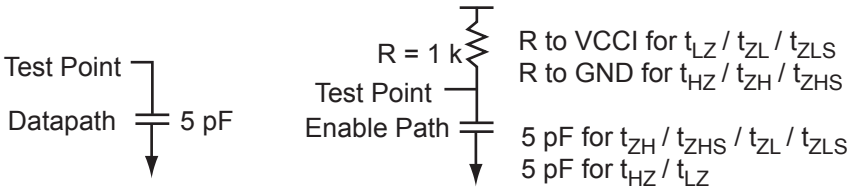

Figure 2-11 • AC Loading

Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	5

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Table 2-102 • 1.5 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	9.78	0.05	1.44	0.45	9.96	8.57	3.74	2.91	12.42	11.03	ns
	–1	0.54	8.32	0.04	1.23	0.39	8.47	7.29	3.18	2.47	10.56	9.38	ns
4 mA	Std.	0.63	8.44	0.05	1.44	0.45	8.60	7.59	4.12	3.60	11.06	10.05	ns
	–1	0.54	7.18	0.04	1.23	0.39	7.32	6.46	3.51	3.06	9.41	8.55	ns
6 mA	Std.	0.63	7.95	0.05	1.44	0.45	8.10	7.39	4.21	3.78	10.56	9.85	ns
	–1	0.54	6.77	0.04	1.23	0.39	6.89	6.29	3.58	3.21	8.98	8.38	ns
8 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	–1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns
12 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	–1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-103 • 1.5 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.98	0.05	1.58	0.45	4.06	3.80	3.73	3.04	6.52	6.26	ns
	–1	0.54	3.39	0.04	1.35	0.39	3.45	3.23	3.17	2.59	5.54	5.32	ns
4 mA	Std.	0.63	3.47	0.05	1.58	0.45	3.53	3.15	4.11	3.74	5.99	5.61	ns
	–1	0.54	2.95	0.04	1.35	0.39	3.01	2.68	3.50	3.18	5.10	4.77	ns
6 mA	Std.	0.63	3.37	0.05	1.58	0.45	3.43	3.02	4.20	3.92	5.89	5.48	ns
	–1	0.54	2.87	0.04	1.35	0.39	2.92	2.57	3.57	3.33	5.01	4.66	ns
8 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	–1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns
12 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	–1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

Table 2-112 • 1.2 V LVCMOS Wide Range Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	Std.	0.80	12.61	0.05	2.65	3.75	0.52	12.10	9.50	5.11	4.66	14.31	11.71	ns
	–1	0.68	10.72	0.05	2.25	3.19	0.44	10.30	8.08	4.35	3.97	12.17	9.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-113 • 1.2 V LVCMOS Wide Range High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	Std.	0.80	5.16	0.05	2.65	3.75	0.52	4.98	4.39	5.10	4.81	7.19	6.60	ns
	–1	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-139 • HSTL Class I
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	3.02	0.04	2.52	0.40	3.05	3.00	–	–	4.51	4.46	ns
–1	0.52	2.57	0.03	2.14	0.34	2.59	2.55	–	–	3.84	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-155 • SSTL3 Class I
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.15	0.04	1.77	0.40	2.17	1.70	–	–	2.17	1.70	ns
–1	0.52	1.83	0.03	1.51	0.34	1.84	1.45	–	–	1.84	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	103	109	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

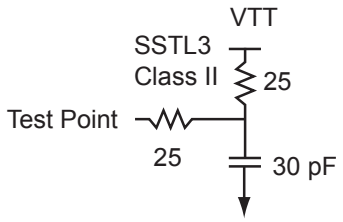

Figure 2-24 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL3 Class II
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.00	0.52	2.08	1.65	–	–	2.08	1.65	ns
–1	0.68	1.75	0.05	1.71	0.44	1.77	1.41	–	–	1.77	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-167 • LVPECL
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.80	1.78	0.05	2.16	ns
–1	0.68	1.51	0.05	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.5 V DC Core Voltage

Table 2-168 • LVPECL
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.61	1.65	0.04	1.89	ns
–1	0.52	1.40	0.03	1.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-169 • LVPECL
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.98	0.05	1.54	ns
–1	0.54	1.68	0.04	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

1.5 V DC Core Voltage

Table 2-197 • A3PE600L Global Resource
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.82	1.07	0.97	1.26	ns
t_{RCKH}	Input High Delay for Global Clock	0.81	1.10	0.95	1.30	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.30		0.35	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-198 • A3PE3000L Global Resource
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.62	1.87	1.90	2.20	ns
t_{RCKH}	Input High Delay for Global Clock	1.61	1.90	1.89	2.24	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.30		0.35	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-207 • RAM512X18
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.31	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.10	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.23	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.29	2.69	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.95	1.12	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	0.98	1.15	ns
	RESET Low to data out Low on RD (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t_{CYC}	Clock cycle time	5.39	6.20	ns
F_{MAX}	Maximum frequency	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-210 • FIFO Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.46	1.71	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.40	0.47	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.23	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.50	2.93	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	0.95	1.11	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	1.82	2.14	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.73	2.03	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.56	7.71	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	1.79	2.11	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	6.49	7.63	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	0.98	1.15	ns
	RESET LOW to Data Out LOW on RD (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET Removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET Recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.59	0.67	ns
t_{CYC}	Clock Cycle Time	5.39	6.20	ns
F_{MAX}	Maximum Frequency for FIFO	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

PQ208	
Pin Number	A3P1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC

PQ208	
Pin Number	A3P1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG484	
Pin Number	A3PE600L Function
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC

FG484	
Pin Number	A3PE600L Function
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0

FG484	
Pin Number	A3PE600L Function
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC

FG896	
Pin Number	**A3PE3000L Function**
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND

FG896	
Pin Number	**A3PE3000L Function**
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Military ProASIC3/EL Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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