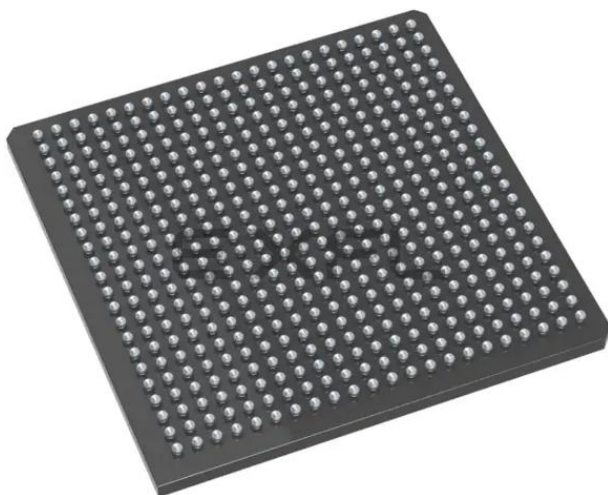




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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000l-1fg484m

2 – Military ProASIC3/EL DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage for A3PE600/3000L DC output buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VMV	DC input buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+150	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4 on page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Table 2-4 on page 2-3](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).

Table 2-18 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	141.97
3.3 V LVCMOS Wide Range	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.82
LVPECL	–	3.3	19.54	167.55

Notes:

1. Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.
2. PDC7 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CCI}.

Table 2-19 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	125.97
3.3 V LVCMOS – Wide Range	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.
2. PDC7 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CCI}.

Table 2-21 • Different Components Contributing to Dynamic Power Consumption in Military ProASIC3 and ProASIC3/EL Devices at 1.5 V VCC

Parameter	Definition	Device-Specific Dynamic Power (μ W/MHz)			
		A3PE3000L	A3PE600L	A3P1000	A3P250
PAC1	Clock contribution of a Global Rib	13.03	6.24	14.50	11.00
PAC2	Clock contribution of a Global Spine	6.69	3.47	2.48	1.58
PAC3	Clock contribution of a VersaTile row	1.46	1.46	0.81	0.81
PAC4	Clock contribution of a VersaTile used as a sequential module	0.13	0.13	0.12	0.12
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-14 on page 2-9 through Table 2-16 on page 2-10.			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12.			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Dynamic contribution for PLL	2.60			

Table 2-22 • Different Components Contributing to the Static Power Consumption in Military ProASIC3/EL Devices

Parameter	Definition	Device-Specific Dynamic Power (μW)			
		A3PE3000L	A3PE600L	A3P1000	A3P250
PDC0	Array static power in Sleep mode	0 mW	0 mW	N/A	N/A
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8 .			
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8 .			
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7 .			
PDC4	Static PLL contribution at 1.2 V operating core voltage (for A3PE600L and A3PE3000L only)	1.42 mW		N/A	
	Static PLL contribution 1.5 V operating core voltage	2.55 mW			
PDC5	Bank quiescent power (V _{CC1} -dependent)	See Table 2-9 on page 2-7 , Table 2-10 on page 2-7 , Table 2-12 on page 2-8 .			
PDC6	I/O input pin static power (standard-dependent)	See Table 2-14 on page 2-9 . through Table 2-16 on page 2-10 .			
PDC7	I/O output pin static power (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12 .			

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in the Libero SoC.

User I/O Characteristics

Timing Model

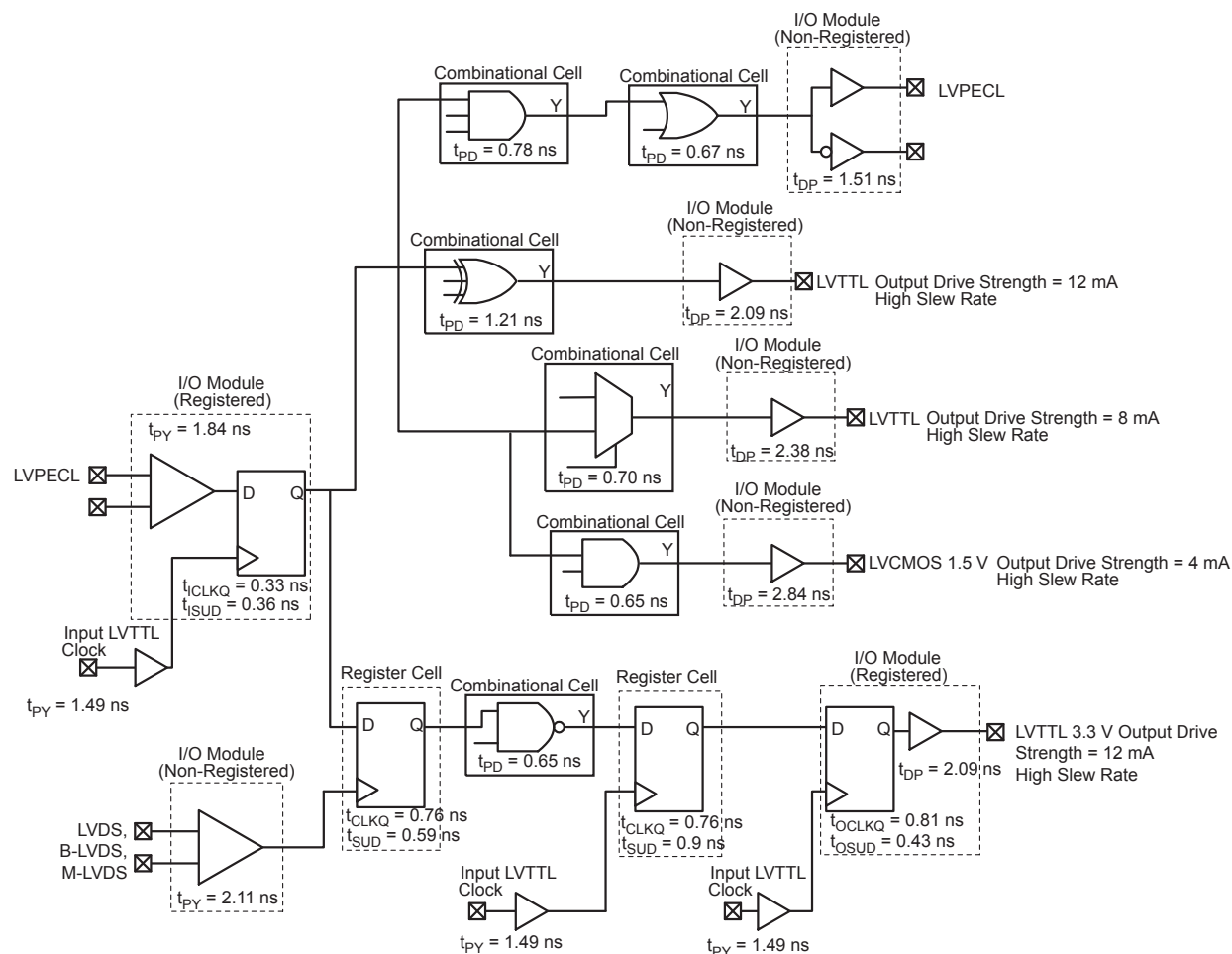


Figure 2-3 • Timing Model

Operating Conditions: –1 Speed, Military Temperature Range ($T_J = 125^\circ\text{C}$), Worst-Case $V_{CC} = 1.14$ V (example for A3PE3000L and A3PE600L)

Table 2-28 • Summary of Maximum and Minimum DC Input Levels
Applicable to Military Conditions

DC I/O Standard	Military ¹	
	I_{IL} ²	I_{IH} ³
	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	15	15
3.3 V LVCMOS Wide Range	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS ⁴	15	15
1.2 V LVCMOS Wide Range ⁴	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1. Military temperature range: $-55^{\circ}C$ to $125^{\circ}C$.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3 V < V_{IN} < V_{IL}$.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. Applicable to Military A3PE600L and A3PE3000L devices operating at $V_{CCI} \geq V_{CC}$.

Table 2-40 • I/O Short Currents IOSH/IOSL
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	Drive Strength	I_{OSL} (mA) ¹	I_{OSH} (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 μ A	Same specification as regular LVCMOS 3.3 V	
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 μ A	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X specification	Per PCI Curves	
3.3 V GTL	20 mA ²	268	181
2.5 V GTL	20 mA ²	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA ²	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

Notes:

1. $T_J = 100^\circ\text{C}$
2. Output drive strength is below JEDEC specification.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-50 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	6.04	0.05	1.75	2.38	0.52	6.14	4.84	2.68	2.43	8.35	7.05	ns
	–1	0.68	5.13	0.05	1.49	2.03	0.44	5.22	4.12	2.28	2.07	7.10	6.00	ns
8 mA	Std.	0.80	4.93	0.05	1.75	2.38	0.52	5.02	4.14	3.02	3.05	7.22	6.34	ns
	–1	0.68	4.20	0.05	1.49	2.03	0.44	4.27	3.52	2.57	2.59	6.14	5.40	ns
12 mA	Std.	0.80	4.15	0.05	1.75	2.38	0.52	4.22	3.61	3.25	3.43	6.43	5.81	ns
	–1	0.68	3.53	0.05	1.49	2.03	0.44	3.59	3.07	2.76	2.92	5.47	4.95	ns
16 mA	Std.	0.80	3.93	0.05	1.75	2.38	0.52	3.99	3.49	3.29	3.54	6.20	5.70	ns
	–1	0.68	3.34	0.05	1.49	2.03	0.44	3.40	2.97	2.80	3.01	5.27	4.85	ns
24 mA	Std.	0.80	3.81	0.05	1.75	2.38	0.52	3.87	3.51	3.36	3.94	6.08	5.71	ns
	–1	0.68	3.24	0.05	1.49	2.03	0.44	3.30	2.98	2.86	3.35	5.17	4.86	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	3.40	0.05	1.75	2.38	0.52	3.45	2.60	2.68	2.58	5.66	4.81	ns
	–1	0.68	2.89	0.05	1.49	2.03	0.44	2.94	2.21	2.28	2.19	4.81	4.09	ns
8 mA	Std.	0.80	2.79	0.05	1.75	2.38	0.52	2.84	2.08	3.02	3.19	5.04	4.29	ns
	–1	0.68	2.38	0.05	1.49	2.03	0.44	2.41	1.77	2.57	2.72	4.29	3.65	ns
12 mA	Std.	0.80	2.45	0.05	1.75	2.38	0.52	2.49	1.83	3.25	3.59	4.70	4.04	ns
	–1	0.68	2.09	0.05	1.49	2.03	0.44	2.12	1.56	2.76	3.06	3.99	3.43	ns
16 mA	Std.	0.80	2.40	0.05	1.75	2.38	0.52	2.43	1.79	3.30	3.70	4.64	3.99	ns
	–1	0.68	2.04	0.05	1.49	2.03	0.44	2.07	1.52	2.81	3.15	3.95	3.40	ns
24 mA	Std.	0.80	2.42	0.05	1.75	2.38	0.52	2.46	1.72	3.37	4.10	4.66	3.93	ns
	–1	0.68	2.06	0.05	1.49	2.03	0.44	2.09	1.47	2.86	3.49	3.97	3.34	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-80 • 2.5 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	6.45	0.05	1.43	0.45	6.56	5.71	2.48	2.19	9.02	8.17	ns
	–1	0.54	5.48	0.04	1.21	0.39	5.58	4.86	2.11	1.86	7.68	6.95	ns
6 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	–1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
8 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	–1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
12 mA	Std.	0.63	4.48	0.05	1.43	0.45	4.56	4.35	3.11	3.31	7.02	6.81	ns
	–1	0.54	3.81	0.04	1.21	0.39	3.88	3.70	2.65	2.82	5.97	5.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-81 • 2.5 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.18	0.05	1.43	0.45	3.23	2.92	2.48	2.28	5.69	5.38	ns
	–1	0.54	2.70	0.04	1.21	0.39	2.75	2.48	2.11	1.94	4.84	4.58	ns
6 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	–1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
8 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	–1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
12 mA	Std.	0.63	2.28	0.05	1.43	0.45	2.32	1.90	3.11	3.42	4.78	4.36	ns
	–1	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-82 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	15	15
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	15	15
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	6	6	35	44	15	15
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	8	8	45	51	15	15
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	12	12	91	74	15	15
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	16	16	91	74	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-83 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	15	15
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	15	15
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	15	15
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	45	51	15	15
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12	91	74	15	15
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	16	16	91	74	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	I _{IH} ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
8 mA	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	8	8	32	39	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.

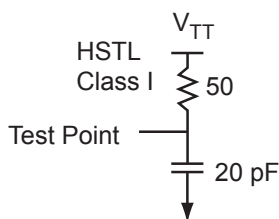


Figure 2-19 • AC Loading

Table 2-137 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-138 • HSTL Class I

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V,

Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.80	3.15	0.05	2.76	0.52	3.20	3.11	—	—	5.41	5.32	ns
−1	0.68	2.68	0.05	2.34	0.44	2.73	2.65	—	—	4.60	4.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-139 • HSTL Class I
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 1.4\text{ V}$, $V_{REF} = 0.75\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	3.02	0.04	2.52	0.40	3.05	3.00	—	—	4.51	4.46	ns
–1	0.52	2.57	0.03	2.14	0.34	2.59	2.55	—	—	3.84	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-159 • SSTL3 Class II
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$,

Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.91	0.04	1.77	0.40	1.92	1.54	–	–	1.92	1.54	ns
–1	0.52	1.63	0.03	1.51	0.34	1.64	1.31	–	–	1.64	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

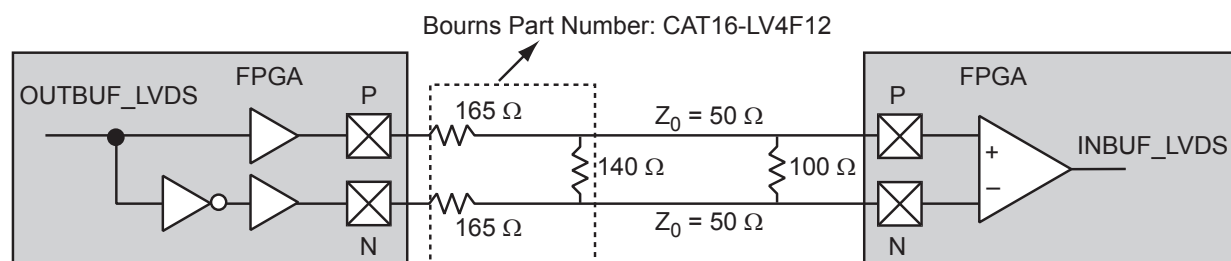
Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-25](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, military ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).


Figure 2-25 • LVDS Circuit Diagram and Board-Level Implementation

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

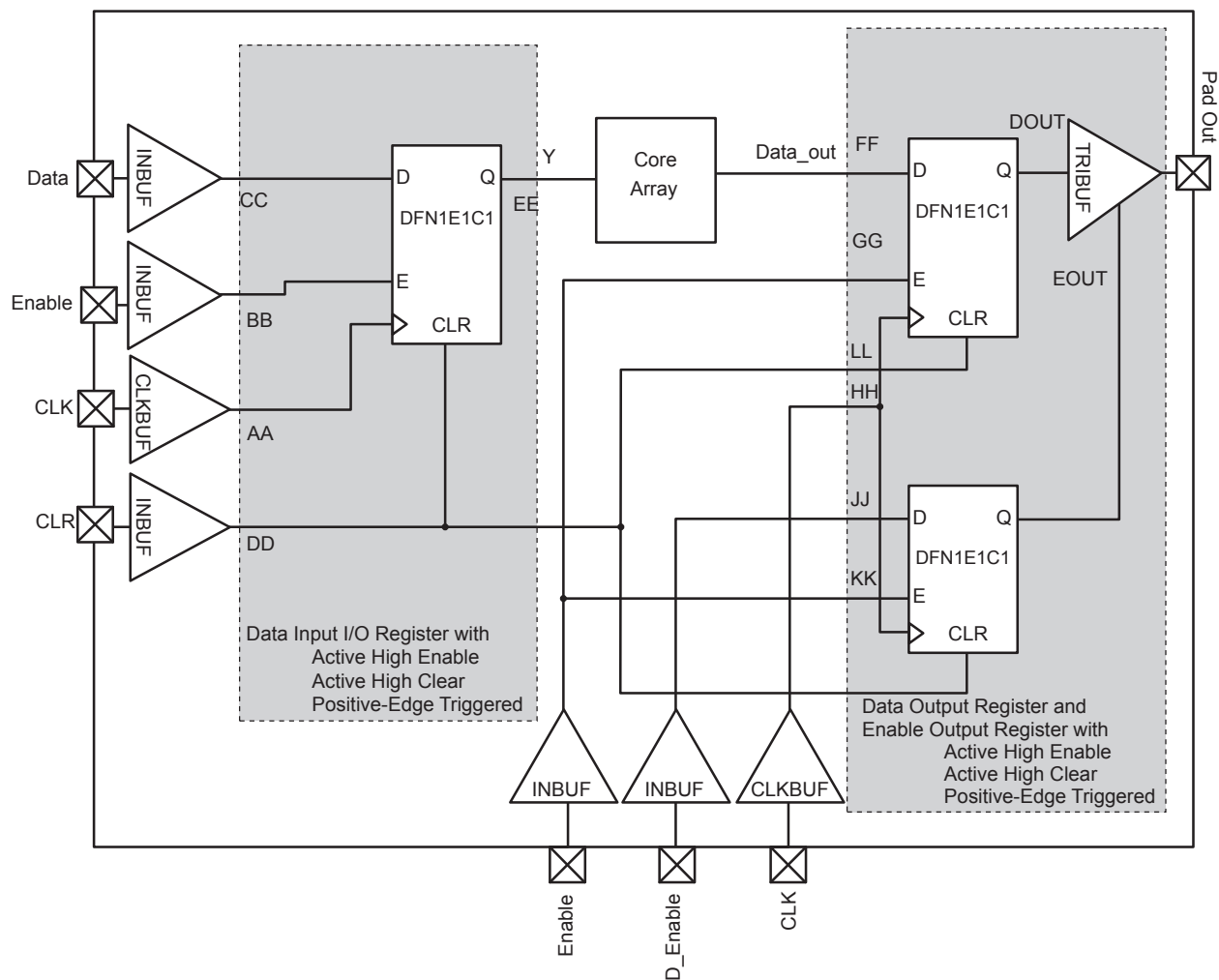


Figure 2-29 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Timing Characteristics

Table 2-172 • Input Data Register Propagation Delays
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.33	0.39	ns
t_{SUD}	Data Setup Time for the Input Data Register	0.36	0.43	ns
t_{HD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Input Data Register	0.51	0.60	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.74	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.63	0.74	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.31	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.31	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-173 • Input Data Register Propagation Delays
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.25	0.30	ns
t_{SUD}	Data Setup Time for the Input Data Register	0.28	0.33	ns
t_{HD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Input Data Register	0.39	0.46	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.56	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.56	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-183 • Input DDR Propagation Delays
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for any A3PE600L/A3PE3000L

Parameter	Description	–1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.29	0.34	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.41	0.48	ns
t_{DDRISUD1}	Data Setup for Input DDR (fall)	0.30	0.35	ns
t_{DDRISUD2}	Data Setup for Input DDR (rise)	0.26	0.31	ns
t_{DDRIHD1}	Data Hold for Input DDR (fall)	0.00	0.00	ns
t_{DDRIHD2}	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.49	0.58	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.60	0.71	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	0.28	ns
t_{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250	250	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-184 • Input DDR Propagation Delays
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.33	0.39	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.47	0.55	ns
t_{DDRISUD1}	Data Setup for Input DDR (fall)	0.30	0.35	ns
t_{DDRISUD2}	Data Setup for Input DDR (rise)	0.30	0.35	ns
t_{DDRIHD1}	Data Hold for Input DDR (fall)	0.00	0.00	ns
t_{DDRIHD2}	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.56	0.65	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.69	0.81	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
t_{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.37	0.43	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-212 • FIFO Worst Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3P250 (256×16)

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.92	4.61	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.61	3.06	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.14	1.34	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t_{REMRSTB}	RESET Removal	0.34	0.40	ns
t_{RECRSTB}	RESET Recovery	1.81	2.12	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

FG256	
Pin Number	A3P1000 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	A3P1000 Function
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	A3P1000 Function
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG256	
Pin Number	A3P1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	A3P1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	A3P1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG256	
Pin Number	A3P1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3PE3000L Function
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0

FG484	
Pin Number	A3PE3000L Function
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3