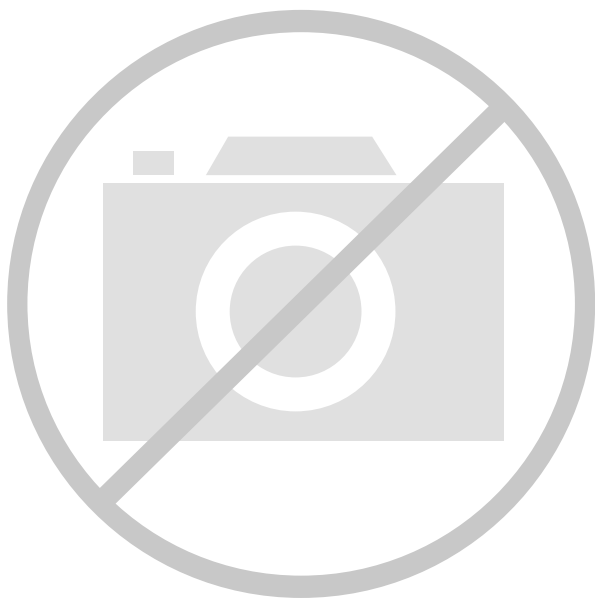




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000l-1fgg484m

A3P1000 – **1** **FG** **G** **144** **Y** **M**

Part Number

Speed Grade
Blank = Standard
1 = 15% Faster than Standard
2 = 25% Faster than Standard

Package Type
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
PQ = Plastic Quad Flat Pack (0.5 mm pitch)

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging

Package Lead Count

Security Feature
Y = Device Includes License to Implement IP Based on the
Cryptography Research, Inc. (CRI) Patent Portfolio

Application (Temperature Range)
M = Military (–55°C to 125°C Junction Temperature)

LICENSED DPA COUNTERMEASURES

Military ProASIC3/EL Devices

A3P250 = 250,000 System Gates
A3PE600L= 600,000 System Gates
A3P1000 = 1,000,000 System Gates
A3PE3000L= 3,000,000 System Gates

Military ProASIC3/EL Devices with ARM Cortex-M1

M1A3P1000 = 1,000,000 System Gates
M1A3PE3000L = 3,000,000 System Gates

Temperature Grade Offerings

Package	A3P250	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices			M1A3P1000	M1A3PE3000L
VQ100	M	–	–	–
PQ208	–	–	M	–
FG144	–	–	M	–
FG256	–	–	M	–
FG484	–	M	M	M
FG896	–	–	–	M

Note: M = Military temperature range: -55°C to 125°C junction temperature

Table 2-40 • I/O Short Currents IOSH/IOSL
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	Drive Strength	I_{OSL} (mA) ¹	I_{OSH} (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 μ A	Same specification as regular LVCMOS 3.3 V	
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 μ A	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X specification	Per PCI Curves	
3.3 V GTL	20 mA ²	268	181
2.5 V GTL	20 mA ²	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA ²	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

Notes:

1. $T_J = 100^\circ\text{C}$
2. Output drive strength is below JEDEC specification.

Table 2-54 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	6.25	0.05	1.12	0.45	6.37	5.29	2.91	2.70	8.83	7.75	ns
	–1	0.54	5.32	0.04	0.95	0.39	5.42	4.50	2.47	2.30	7.51	6.59	ns
6 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	–1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
8 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	–1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
12 mA	Std.	0.63	4.50	0.05	1.12	0.45	4.59	4.05	3.53	3.76	7.05	6.51	ns
	–1	0.54	3.83	0.04	0.95	0.39	3.90	3.45	3.00	3.20	5.99	5.54	ns
16 mA	Std.	0.63	4.27	0.05	1.12	0.45	4.35	3.93	3.58	3.86	6.81	6.39	ns
	–1	0.54	3.63	0.04	0.95	0.39	3.70	3.34	3.05	3.29	5.79	5.43	ns
24 mA	Std.	0.63	4.14	0.05	1.12	0.45	4.22	3.97	3.65	4.27	6.68	6.43	ns
	–1	0.54	3.53	0.04	0.95	0.39	3.59	3.38	3.10	3.63	5.68	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-55 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.55	0.05	1.12	0.45	3.62	2.79	2.91	2.87	6.07	5.25	ns
	–1	0.54	3.02	0.04	0.95	0.39	3.08	2.37	2.48	2.44	5.17	4.46	ns
6 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	–1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
8 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	–1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
12 mA	Std.	0.63	2.64	0.05	1.12	0.45	2.68	1.99	3.53	3.94	5.14	4.45	ns
	–1	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79	ns
16 mA	Std.	0.63	2.58	0.05	1.12	0.45	2.63	1.95	3.59	4.05	5.09	4.41	ns
	–1	0.54	2.20	0.04	0.95	0.39	2.24	1.66	3.05	3.44	4.33	3.75	ns
24 mA	Std.	0.63	2.61	0.05	1.12	0.45	2.66	1.89	3.66	4.46	5.12	4.35	ns
	–1	0.54	2.22	0.04	0.95	0.39	2.26	1.61	3.11	3.80	4.35	3.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

3.3 V LVCMOS Wide Range

Table 2-58 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	25	27	15	15
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	25	27	15	15
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	51	54	15	15
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	103	109	15	15
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	132	127	15	15
100 μA	24 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	268	181	15	15

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < V_{IN} < V_{IL}.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
4. Currents are measured at 125°C junction temperature.
5. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.
6. Software default selection highlighted in gray.

Table 2-59 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	25	27	15	15
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	25	27	15	15
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	51	54	15	15
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	51	54	15	15
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	103	109	15	15
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	132	127	15	15

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < V_{IN} < V_{IL}.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
4. Currents are measured at 125°C junction temperature.
5. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.
6. Software default selection highlighted in gray.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-62 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.80	9.08	0.05	2.18	3.16	0.52	9.08	7.17	3.85	3.40	11.28	9.38	ns
		–1	0.68	7.72	0.05	1.86	2.69	0.44	7.72	6.10	3.28	2.89	9.60	7.98	ns
100 μA	8 mA	Std.	0.80	7.37	0.05	2.18	3.16	0.52	7.37	6.10	4.38	4.35	9.58	8.31	ns
		–1	0.68	6.27	0.05	1.86	2.69	0.44	6.27	5.19	3.73	3.70	8.15	7.07	ns
100 μA	12 mA	Std.	0.80	6.17	0.05	2.18	3.16	0.52	6.17	5.30	4.73	4.94	8.37	7.51	ns
		–1	0.68	5.24	0.05	1.86	2.69	0.44	5.24	4.51	4.03	4.20	7.12	6.38	ns
100 μA	16 mA	Std.	0.80	5.82	0.05	2.18	3.16	0.52	5.82	5.12	4.80	5.11	8.03	7.33	ns
		–1	0.68	4.95	0.05	1.86	2.69	0.44	4.95	4.36	4.09	4.34	6.83	6.23	ns
100 μA	24 mA	Std.	0.80	5.64	0.05	2.18	3.16	0.52	5.64	5.14	4.90	5.72	7.85	7.35	ns
		–1	0.68	4.80	0.05	1.86	2.69	0.44	4.80	4.38	4.17	4.87	6.67	6.25	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-63 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.80	5.00	0.05	2.18	3.16	0.52	5.00	3.77	3.85	3.62	7.21	5.97	ns
		–1	0.68	4.25	0.05	1.86	2.69	0.44	4.25	3.21	3.28	3.08	6.13	5.08	ns
100 μA	8 mA	Std.	0.80	4.07	0.05	2.18	3.16	0.52	4.07	2.98	4.38	4.57	6.27	5.19	ns
		–1	0.68	3.46	0.05	1.86	2.69	0.44	3.46	2.54	3.73	3.89	5.33	4.41	ns
100 μA	12 mA	Std.	0.80	3.54	0.05	2.18	3.16	0.52	3.54	2.60	4.73	5.19	5.74	4.81	ns
		–1	0.68	3.01	0.05	1.86	2.69	0.44	3.01	2.22	4.03	4.42	4.89	4.09	ns
100 μA	16 mA	Std.	0.80	3.45	0.05	2.18	3.16	0.52	3.45	2.54	4.82	5.36	5.66	4.74	ns
		–1	0.68	2.94	0.05	1.86	2.69	0.44	2.94	2.16	4.10	4.56	4.81	4.03	ns
100 μA	24 mA	Std.	0.80	3.49	0.05	2.18	3.16	0.52	3.49	2.44	4.91	5.98	5.69	4.64	ns
		–1	0.68	2.97	0.05	1.86	2.69	0.44	2.97	2.07	4.18	5.08	4.84	3.95	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to the [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

1.5 V DC Core Voltage

Table 2-64 • 3.3 V LVCMOS Wide Range Low Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.61	8.94	0.04	1.90	2.87	0.40	8.92	7.06	3.69	3.20	10.39	8.53	ns
		–1	0.52	7.61	0.03	1.61	2.44	0.34	7.59	6.01	3.14	2.72	8.84	7.25	ns
100 μA	8 mA	Std.	0.61	7.24	0.04	1.90	2.87	0.40	7.22	5.99	4.23	4.15	8.68	7.45	ns
		–1	0.52	6.16	0.03	1.61	2.44	0.34	6.14	5.10	3.60	3.53	7.39	6.34	ns
100 μA	12 mA	Std.	0.61	6.03	0.04	1.90	2.87	0.40	6.01	5.19	4.58	4.74	7.47	6.65	ns
		–1	0.52	5.13	0.03	1.61	2.44	0.34	5.11	4.41	3.89	4.03	6.36	5.66	ns
100 μA	16 mA	Std.	0.61	5.68	0.04	1.90	2.87	0.40	5.66	5.01	4.65	4.91	7.13	6.47	ns
		–1	0.52	4.83	0.03	1.61	2.44	0.34	4.82	4.26	3.95	4.18	6.06	5.51	ns
100 μA	24 mA	Std.	0.61	5.50	0.04	1.90	2.87	0.40	5.48	5.03	4.74	5.53	6.95	6.49	ns
		–1	0.52	4.68	0.03	1.61	2.44	0.34	4.66	4.28	4.04	4.70	5.91	5.52	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-65 • 3.3 V LVCMOS Wide Range High Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.61	4.86	0.04	1.90	2.87	0.40	4.84	3.65	3.69	3.43	6.31	5.12	ns
		–1	0.52	4.14	0.03	1.61	2.44	0.34	4.12	3.11	3.14	2.91	5.37	4.35	ns
100 μA	8 mA	Std.	0.61	3.93	0.04	1.90	2.87	0.40	3.91	2.87	4.23	4.38	5.37	4.33	ns
		–1	0.52	3.34	0.03	1.61	2.44	0.34	3.33	2.44	3.60	3.72	4.57	3.68	ns
100 μA	12 mA	Std.	0.61	3.40	0.04	1.90	2.87	0.40	3.38	2.49	4.58	4.99	4.85	3.95	ns
		–1	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36	ns
100 μA	16 mA	Std.	0.61	3.31	0.04	1.90	2.87	0.40	3.29	2.42	4.66	5.16	4.76	3.89	ns
		–1	0.52	2.82	0.03	1.61	2.44	0.34	2.80	2.06	3.96	4.39	4.05	3.31	ns
100 μA	24 mA	Std.	0.61	3.35	0.04	1.90	2.87	0.40	3.33	2.32	4.76	5.78	4.80	3.79	ns
		–1	0.52	2.85	0.03	1.61	2.44	0.34	2.83	1.98	4.05	4.92	4.08	3.22	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-74 • 2.5 V LVCMOS Low Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	6.87	0.05	2.04	2.56	0.52	6.99	5.83	2.70	2.19	9.20	8.03	ns
	–1	0.68	5.84	0.05	1.73	2.17	0.44	5.95	4.96	2.29	1.86	7.82	6.83	ns
8 mA	Std.	0.80	5.62	0.05	2.04	2.56	0.52	5.72	4.94	3.08	2.90	7.92	7.14	ns
	–1	0.68	4.78	0.05	1.73	2.17	0.44	4.86	4.20	2.62	2.47	6.74	6.08	ns
12 mA	Std.	0.80	4.73	0.05	2.04	2.56	0.52	4.81	4.30	3.34	3.38	7.01	6.50	ns
	–1	0.68	4.02	0.05	1.73	2.17	0.44	4.09	3.65	2.84	2.87	5.97	5.53	ns
16 mA	Std.	0.80	4.46	0.05	2.04	2.56	0.52	4.53	4.16	3.39	3.50	6.74	6.36	ns
	–1	0.68	3.79	0.05	1.73	2.17	0.44	3.86	3.54	2.89	2.98	5.73	5.41	ns
24 mA	Std.	0.80	4.34	0.05	2.04	2.56	0.52	4.41	4.17	3.47	3.96	6.62	6.38	ns
	–1	0.68	3.69	0.05	1.73	2.17	0.44	3.75	3.55	2.95	3.96	5.63	5.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-75 • 2.5 V LVCMOS High Slew

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	3.51	0.05	2.04	2.56	0.52	3.56	3.13	2.70	2.27	5.77	5.33	ns
	–1	0.68	2.98	0.05	1.73	2.17	0.44	3.03	2.66	2.29	1.93	4.91	4.53	ns
8 mA	Std.	0.80	2.87	0.05	2.04	2.56	0.52	2.92	2.40	3.08	3.01	5.12	4.61	ns
	–1	0.68	2.44	0.05	1.73	2.17	0.44	2.48	2.05	2.62	2.56	4.36	3.92	ns
12 mA	Std.	0.80	2.50	0.05	2.04	2.56	0.52	2.53	2.05	3.34	3.47	4.74	4.25	ns
	–1	0.68	2.12	0.05	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62	ns
16 mA	Std.	0.80	2.43	0.05	2.04	2.56	0.52	2.47	1.98	3.39	3.59	4.67	4.19	ns
	–1	0.68	2.07	0.05	1.73	2.17	0.44	2.10	1.69	2.89	3.06	3.97	3.56	ns
24 mA	Std.	0.80	2.44	0.05	2.04	2.56	0.52	2.48	1.90	3.47	4.08	4.68	4.10	ns
	–1	0.68	2.08	0.05	1.73	2.17	0.44	2.11	1.61	2.95	3.47	3.98	3.49	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-78 • 2.5 V LVC MOS Low Slew

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	7.07	0.05	1.44	0.45	7.20	6.32	2.95	2.43	9.66	8.78	ns
	–1	0.54	6.02	0.04	1.23	0.39	6.13	5.38	2.51	2.06	8.22	7.47	ns
6 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	–1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
8 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	–1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
12 mA	Std.	0.63	5.05	0.05	1.44	0.45	5.15	4.79	3.63	3.66	7.61	7.25	ns
	–1	0.54	4.30	0.04	1.23	0.39	4.38	4.07	3.09	3.11	6.47	6.17	ns
16 mA	Std.	0.63	4.78	0.05	1.44	0.45	4.86	4.65	3.70	3.78	7.32	7.10	ns
	–1	0.54	4.06	0.04	1.23	0.39	4.14	3.95	3.14	3.22	6.23	6.04	ns
24 mA	Std.	0.63	4.71	0.05	1.44	0.45	4.73	4.71	3.78	4.26	7.19	7.17	ns
	–1	0.54	4.01	0.04	1.23	0.39	4.03	4.01	3.21	3.62	6.12	6.10	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-79 • 2.5 V LVC MOS High Slew

Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.63	0.05	1.44	0.45	3.70	3.34	2.94	2.53	6.16	5.80	ns
	–1	0.54	3.09	0.04	1.23	0.39	3.15	2.84	2.51	2.16	5.24	4.94	ns
6 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	–1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
8 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	–1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
12 mA	Std.	0.63	2.65	0.05	1.44	0.45	2.70	2.23	3.63	3.78	5.16	4.69	ns
	–1	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99	ns
16 mA	Std.	0.63	2.59	0.05	1.44	0.45	2.64	2.16	3.70	3.90	5.10	4.62	ns
	–1	0.54	2.21	0.04	1.23	0.39	2.25	1.83	3.15	3.32	4.34	3.93	ns
24 mA	Std.	0.63	2.61	0.05	1.44	0.45	2.66	2.08	3.78	4.40	5.12	4.54	ns
	–1	0.54	2.22	0.04	1.23	0.39	2.26	1.77	3.22	3.74	4.35	3.87	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-92 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	–1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	–1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-93 • 1.8 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	–1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	–1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-139 • HSTL Class I
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 1.4\text{ V}$, $V_{REF} = 0.75\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	3.02	0.04	2.52	0.40	3.05	3.00	—	—	4.51	4.46	ns
–1	0.52	2.57	0.03	2.14	0.34	2.59	2.55	—	—	3.84	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-27](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

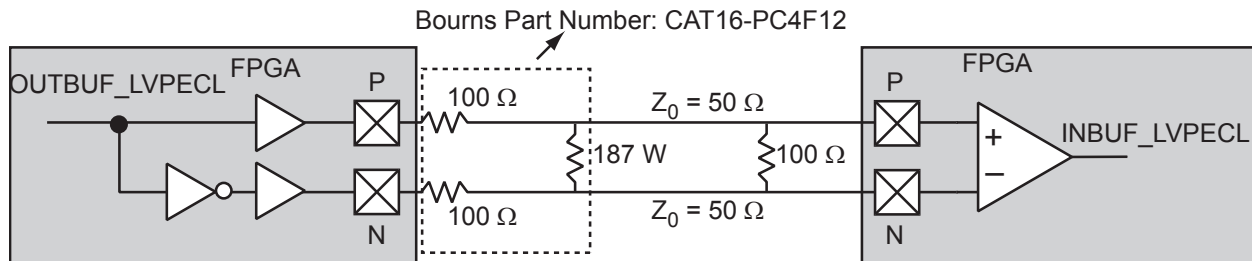


Figure 2-27 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-165 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0	3.3	3.6				V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.3	0	3.6	0	3.9	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = V_{trip} . See [Table 2-29](#) on page 2-25 for a complete table of trip points.

Input Register

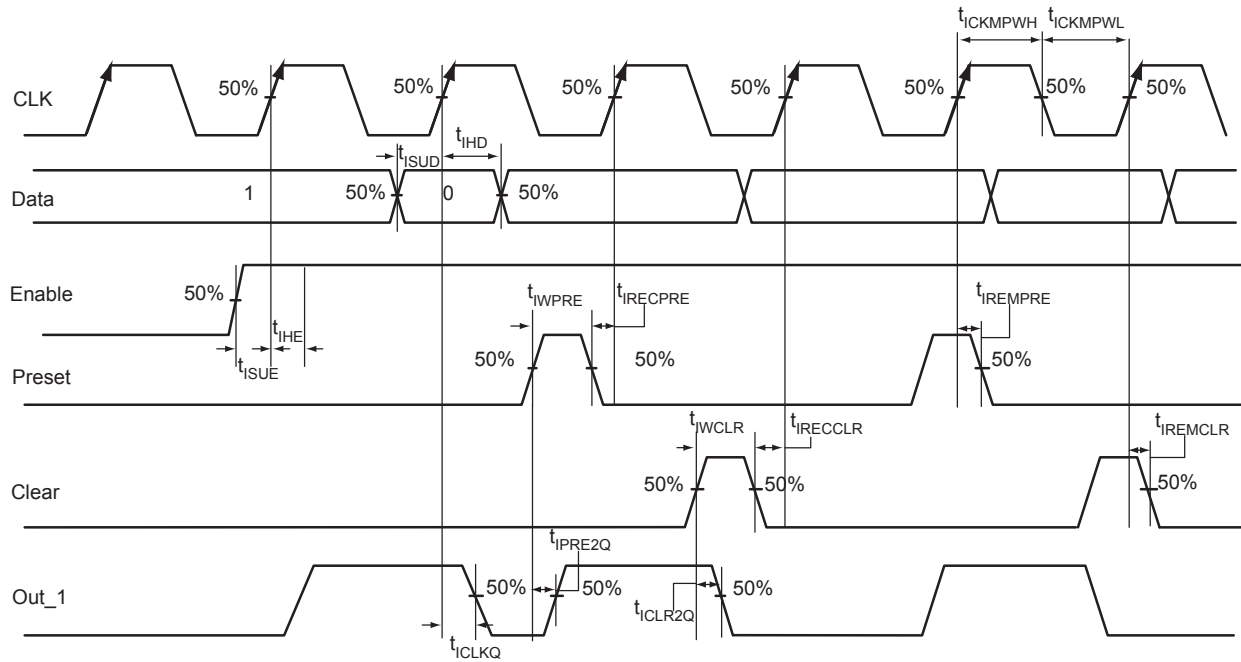


Figure 2-30 • Input Register Timing Diagram

Output Enable Register

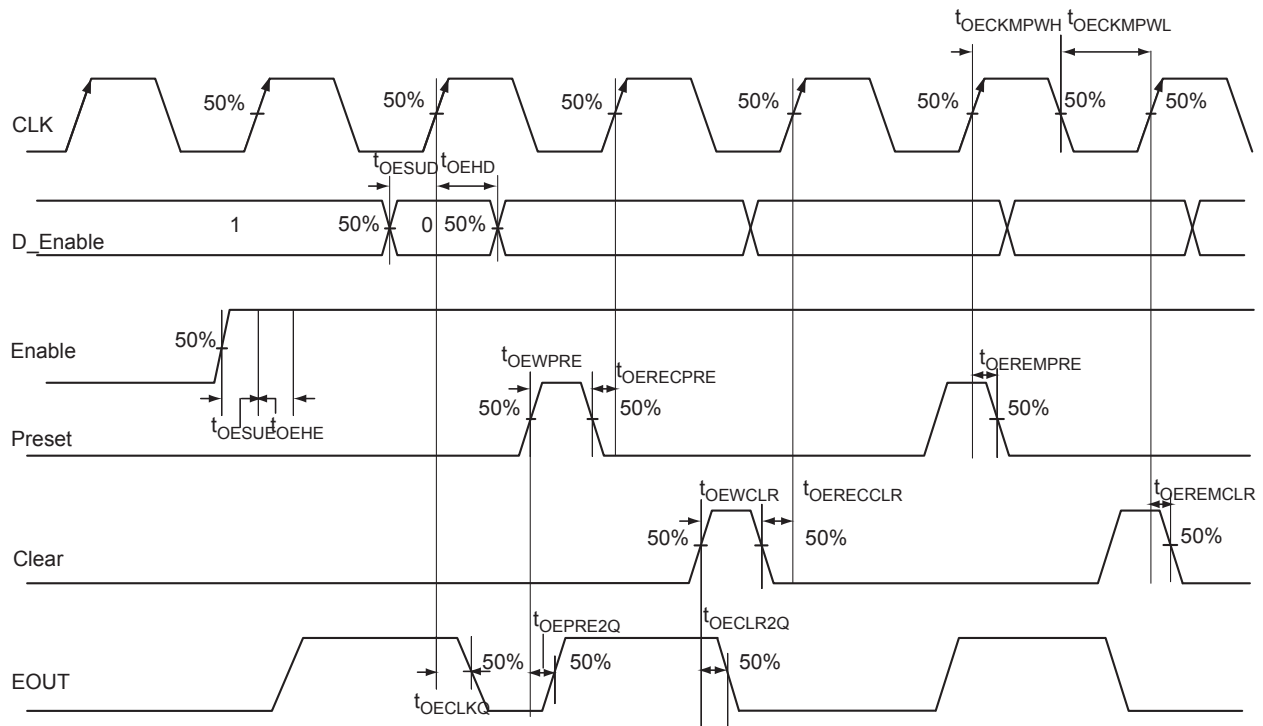


Figure 2-32 • Output Enable Register Timing Diagram

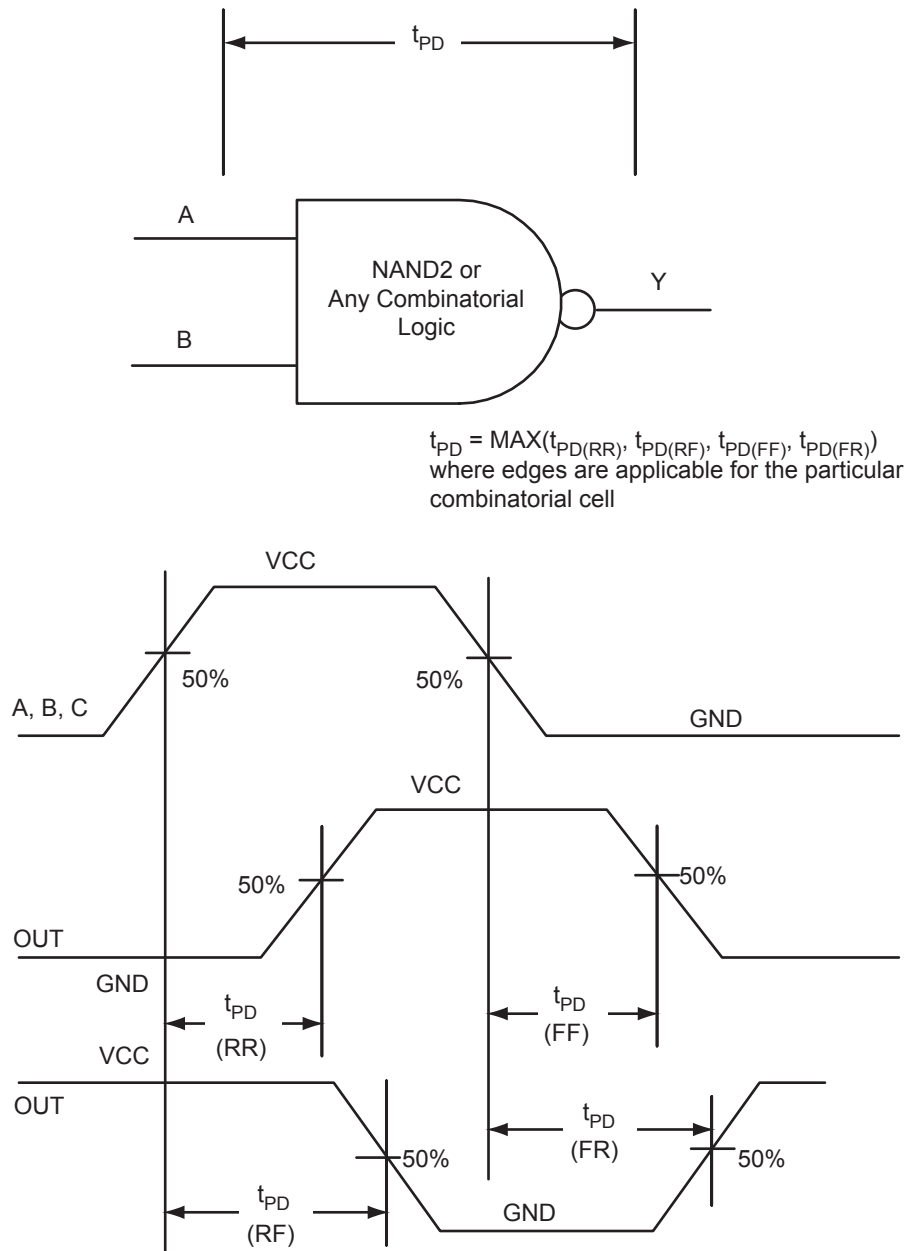


Figure 2-38 • Timing Model and Waveforms

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-201 • Military ProASIC3/EL CCC/PLL Specification
For Devices Operating at 1.2 V DC Core Voltage: Applicable to A3PE600L and A3PE3000L Only

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2, 3}		360		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ⁴			100	MHz
Input cycle-to-cycle jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁵				
LockControl = 0			25	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.025		15.65	ns
Delay Range in Block: Fixed Delay ^{1, 2}		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max. Peak-to-Peak Period Jitter ^{6, 7}			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.60%
50 MHz to 160 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.2\text{ V}$.
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the [Libero online help](#) associated with the core for more information.
4. Maximum value obtained for a –1 speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.
6. Measurements done with LVTTTL 3.3 V, 8 mA I/O drive strength and high slew rate. $V_{CC}/V_{CCPLL} = 1.14\text{V}$, VQ/PQ/TQ type of packages, 20 pF load.
7. Switching I/Os are placed outside of the PLL bank.

Table 2-206 • RAM512X18
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.35	0.41	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.13	0.15	ns
t_{ENH}	REN, WEN hold time	0.08	0.09	ns
t_{DS}	Input data (WD) setup time	0.25	0.30	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.99	3.52	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.24	1.46	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.25	0.29	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.31	0.36	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	1.28	1.50	ns
	RESET Low to data out Low on RD (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.66	0.76	ns
t_{CYC}	Clock cycle time	6.08	6.99	ns
F_{MAX}	Maximum frequency	164	143	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-208 • RAM512X18
Military-Case Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.30	0.35	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.11	0.13	ns
t_{ENH}	REN, WEN hold time	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.22	0.26	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.60	3.06	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.08	1.27	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.43	0.50	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.50	0.59	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	1.11	1.31	ns
	RESET Low to data out Low on RD (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.26	0.30	ns
t_{CYC}	Clock cycle time	3.89	4.57	ns
F_{MAX}	Maximum frequency	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

FG484		FG484		FG484	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
R8	VMV3	T21	IO108PDB1	V12	IO143RSB2
R9	VCCIB2	T22	IO105NDB1	V13	IO138RSB2
R10	VCCIB2	U1	IO195PDB3	V14	IO131RSB2
R11	IO147RSB2	U2	IO195NDB3	V15	IO125RSB2
R12	IO136RSB2	U3	IO194NPB3	V16	GDB2/IO115RSB2
R13	VCCIB2	U4	GEB1/IO189PDB3	V17	TDI
R14	VCCIB2	U5	GEB0/IO189NDB3	V18	GNDQ
R15	VMV2	U6	VMV2	V19	TDO
R16	IO110NDB1	U7	IO179RSB2	V20	GND
R17	GDB1/IO112PPB1	U8	IO171RSB2	V21	NC
R18	GDC1/IO111PDB1	U9	IO165RSB2	V22	IO109NDB1
R19	IO107NDB1	U10	IO159RSB2	W1	NC
R20	VCC	U11	IO151RSB2	W2	IO191PDB3
R21	IO104NDB1	U12	IO137RSB2	W3	NC
R22	IO105PDB1	U13	IO134RSB2	W4	GND
T1	IO198PDB3	U14	IO128RSB2	W5	IO183RSB2
T2	IO198NDB3	U15	VMV1	W6	GEB2/IO186RSB2
T3	NC	U16	TCK	W7	IO172RSB2
T4	IO194PPB3	U17	VPUMP	W8	IO170RSB2
T5	IO192PPB3	U18	TRST	W9	IO164RSB2
T6	GEC1/IO190PPB3	U19	GDA0/IO113NDB1	W10	IO158RSB2
T7	IO192NPB3	U20	NC	W11	IO153RSB2
T8	GNDQ	U21	IO108NDB1	W12	IO142RSB2
T9	GEA2/IO187RSB2	U22	IO109PDB1	W13	IO135RSB2
T10	IO161RSB2	V1	NC	W14	IO130RSB2
T11	IO155RSB2	V2	NC	W15	GDC2/IO116RSB2
T12	IO141RSB2	V3	GND	W16	IO120RSB2
T13	IO129RSB2	V4	GEA1/IO188PDB3	W17	GDA2/IO114RSB2
T14	IO124RSB2	V5	GEA0/IO188NDB3	W18	TMS
T15	GNDQ	V6	IO184RSB2	W19	GND
T16	IO110PDB1	V7	GEC2/IO185RSB2	W20	NC
T17	VJTAG	V8	IO168RSB2	W21	NC
T18	GDC0/IO111NDB1	V9	IO163RSB2	W22	NC
T19	GDA1/IO113PDB1	V10	IO157RSB2	Y1	VCCIB3
T20	NC	V11	IO149RSB2	Y2	IO191NDB3

FG896	
Pin Number	A3PE3000L Function
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4

FG896	
Pin Number	A3PE3000L Function
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0

FG896	
Pin Number	A3PE3000L Function
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1

FG896	
Pin Number	A3PE3000L Function
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND