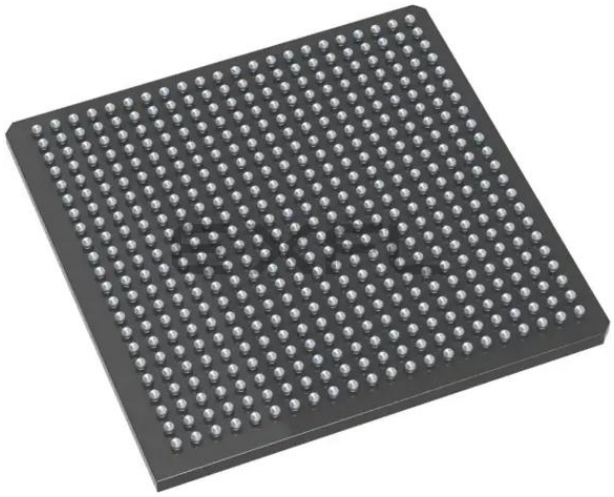

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000l-fg484m

1.5 V Core Voltage

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst Case VCCI Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)[2]	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71
3.3 V LVCOMS Wide Range[3]	100 µA	12 mA	High	5	–	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.01	0.03	1.49	1.93	0.34	2.02	1.65	2.71	2.78	3.27	2.89
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39
3.3 V PCI	Per PCI spec	–	High	10	25[4]	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[4]	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.52	1.68	0.03	1.79	–	0.34	1.58	1.68	–	–	2.83	2.92
2.5 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.52	1.72	0.03	1.73	–	0.34	1.69	1.72	–	–	2.93	2.97
3.3 V GTL+	35 mA	35 mA	High	10	25	0.52	1.66	0.03	1.79	–	0.34	1.63	1.66	–	–	2.88	2.90
2.5 V GTL+	33 mA	33 mA	High	10	25	0.52	1.75	0.03	1.73	–	0.34	1.76	1.69	–	–	3.00	2.94
HSTL (I)	8 mA	8 mA	High	20	25	0.52	2.57	0.03	2.14	–	0.34	2.59	2.55	–	–	3.84	3.79
HSTL (II)	15 mA[5]	15 mA[5]	High	20	50	0.52	2.44	0.03	2.14	–	0.34	2.46	2.19	–	–	3.71	3.43
SSTL2 (I)	15 mA	15 mA	High	30	25	0.52	1.68	0.03	1.58	–	034	1.69	1.46	–	–	1.69	1.46
SSTL2 (II)	18 mA	18 mA	High	30	50	0.52	1.72	0.03	1.58	–	0.34	1.73	1.39	–	–	1.73	1.39
SSTL3 (I)	14 mA	14 mA	High	30	25	0.52	1.83	0.03	1.51	–	0.34	1.84	1.45	–	–	1.84	1.45
SSTL3 (II)	21 mA	21 mA	High	30	50	0.52	1.63	0.03	1.51	–	0.34	1.64	1.31	–	–	1.64	1.31
LVDS	24 mA	–	High	–	–	0.52	1.48	0.03	1.86	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.52	1.40	0.03	1.61	–	–	–	–	–	–	–	–

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-14 on page 2-71 for connectivity. This resistor is not required during normal operation.*
5. *Output drive strength is below JEDEC specification.*
6. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-70 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	15	15
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	15	15
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	15	15
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	83	87	15	15
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	169	124	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-71 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

1.5 V DC Core Voltage

Table 2-88 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	–1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	–1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	–1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	–1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	–1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	–1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	–1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.61	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	–1	0.52	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	034	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-90 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	9.50	0.05	1.44	0.45	9.68	8.31	3.06	1.76	12.14	10.77	ns
	–1	0.54	8.08	0.04	1.23	0.39	8.23	7.07	2.60	1.50	10.32	9.16	ns
4 mA	Std.	0.63	7.80	0.05	1.44	0.45	7.95	7.06	3.55	3.01	10.41	9.52	ns
	–1	0.54	6.64	0.04	1.23	0.39	6.76	6.00	3.02	2.56	8.85	8.10	ns
6 mA	Std.	0.63	6.70	0.05	1.44	0.45	6.82	6.25	3.89	3.60	9.28	8.70	ns
	–1	0.54	5.70	0.04	1.23	0.39	5.80	5.31	3.31	3.06	7.90	7.40	ns
8 mA	Std.	0.63	6.31	0.05	1.44	0.45	6.43	6.07	3.97	3.75	8.89	8.53	ns
	–1	0.54	5.37	0.04	1.23	0.39	5.47	5.17	3.37	3.19	7.56	7.26	ns
12 mA	Std.	0.63	6.18	0.05	1.44	0.45	6.30	6.15	4.08	4.34	8.76	8.61	ns
	–1	0.54	5.26	0.04	1.23	0.39	5.36	5.23	3.47	3.70	7.45	7.32	ns
16 mA	Std.	0.63	6.18	0.05	1.44	0.45	6.30	6.15	4.08	4.34	8.76	8.61	ns
	–1	0.54	5.26	0.04	1.23	0.39	5.36	5.23	3.47	3.70	7.45	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-91 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	4.40	0.05	1.34	0.45	4.48	4.30	3.05	1.82	6.94	6.76	ns
	–1	0.54	3.74	0.04	1.14	0.39	3.81	3.66	2.59	1.55	5.90	5.75	ns
4 mA	Std.	0.63	3.44	0.05	1.34	0.45	3.50	3.23	3.54	3.12	5.96	5.69	ns
	–1	0.54	2.92	0.04	1.14	0.39	2.98	2.75	3.01	2.66	5.07	4.84	ns
6 mA	Std.	0.63	3.02	0.05	1.34	0.45	3.07	2.70	3.88	3.72	5.53	5.16	ns
	–1	0.54	2.57	0.04	1.14	0.39	2.61	2.30	3.30	3.16	4.71	4.39	ns
8 mA	Std.	0.63	2.94	0.05	1.34	0.45	2.99	2.60	3.96	3.87	5.45	5.06	ns
	–1	0.54	2.50	0.04	1.14	0.39	2.54	2.21	3.37	3.30	4.64	4.31	ns
12 mA	Std.	0.63	2.93	0.05	1.34	0.45	2.98	2.49	4.07	4.49	5.44	4.95	ns
	–1	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21	ns
16 mA	Std.	0.63	2.93	0.05	1.34	0.45	2.98	2.49	4.07	4.49	5.44	4.95	ns
	–1	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-94 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	32	39	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	66	55	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	66	55	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-95 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

1.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-114 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the database; Microsemi loadings for enable path characterization are described in Figure 2-14.

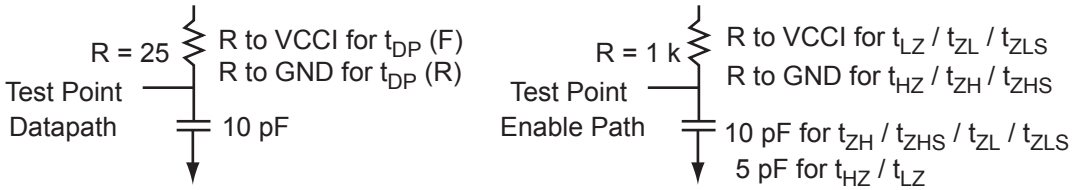

Figure 2-14 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-115.

Table 2-115 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$		10

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

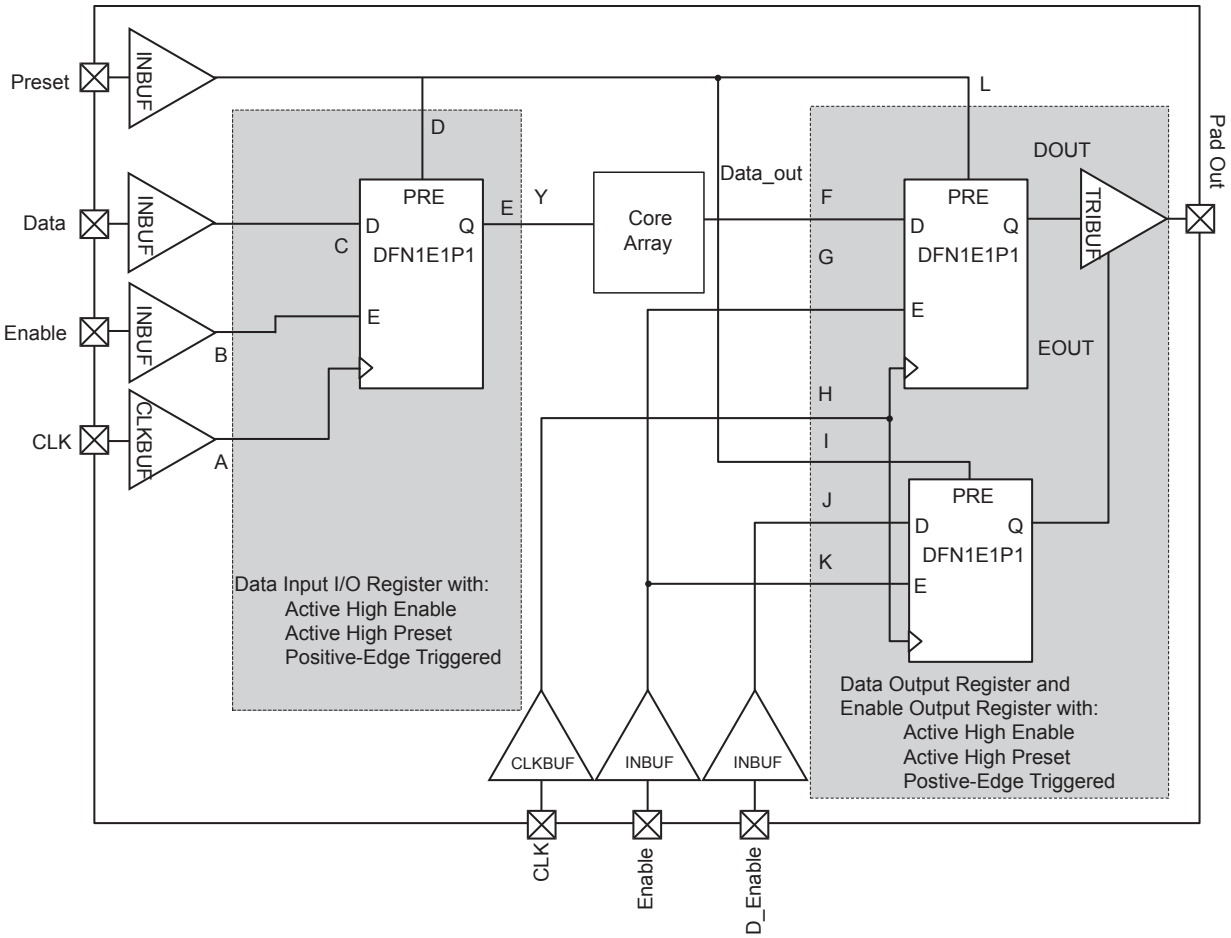

Figure 2-28 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-170 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-28 on page 2-91 for more information.*

Input Register

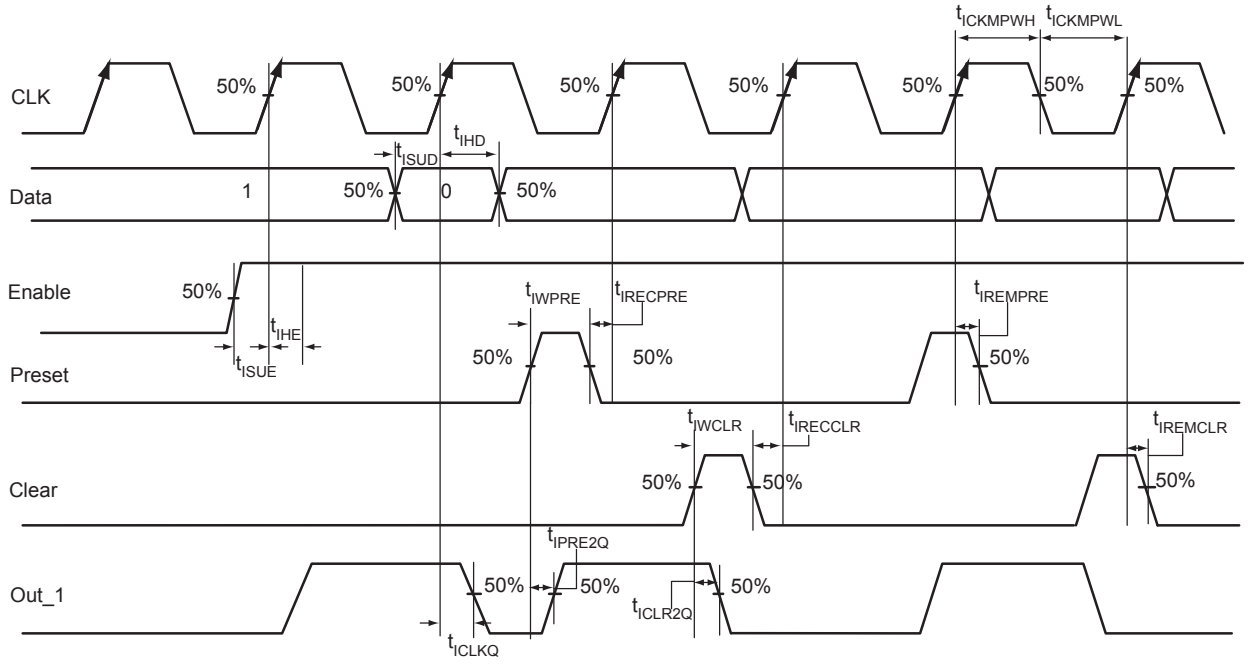

Figure 2-30 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-172 • Input Data Register Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.33	0.39	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.36	0.43	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.51	0.60	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.74	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.63	0.74	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.31	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.31	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-173 • Input Data Register Propagation Delays
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.25	0.30	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.28	0.33	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.39	0.46	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.56	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.56	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output DDR Module

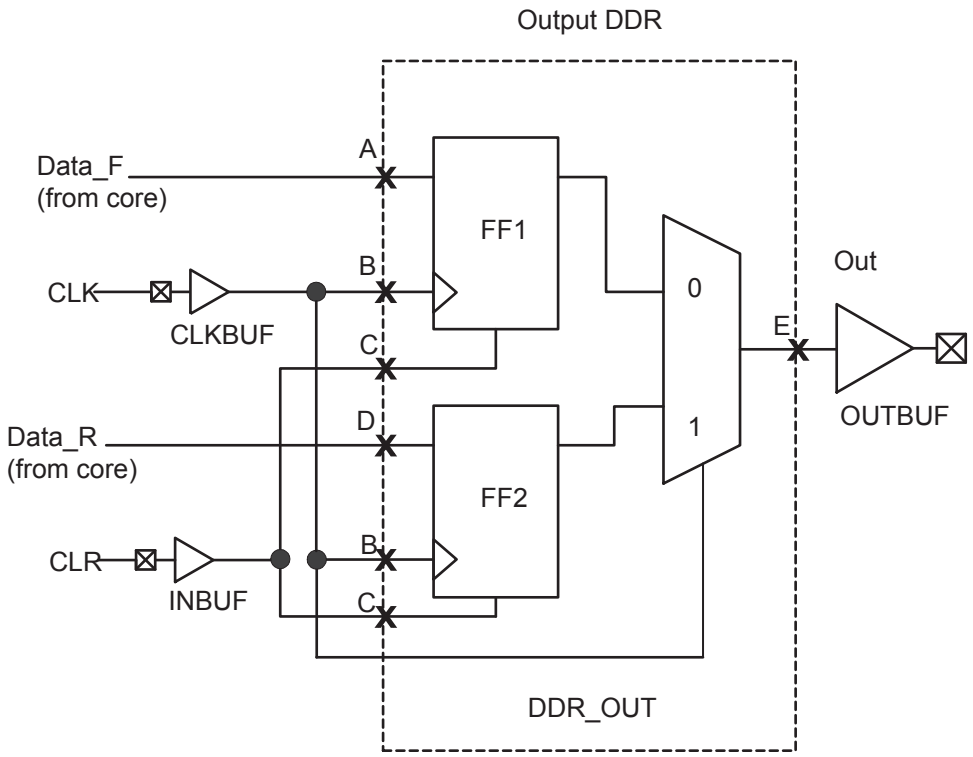

Figure 2-35 • **Output DDR Timing Model**

Table 2-185 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Table 2-191 • Combinatorial Cell Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.48	0.57	ns
AND2	Y = A · B	t_{PD}	0.57	0.67	ns
NAND2	Y = !(A · B)	t_{PD}	0.57	0.67	ns
OR2	Y = A + B	t_{PD}	0.59	0.69	ns
NOR2	Y = !(A + B)	t_{PD}	0.59	0.69	ns
XOR2	Y = A ⊕ B	t_{PD}	0.89	1.04	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.84	0.99	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.05	1.24	ns
MUX2	Y = A !S + B S	t_{PD}	0.61	0.72	ns
AND3	Y = A · B · C	t_{PD}	0.68	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-193 • Register Delays
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.58	0.69	ns
t_{SUD}	Data Setup Time for the Core Register	0.45	0.53	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.48	0.57	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.42	0.50	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.42	0.50	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-205 • RAM4K9
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.30	0.35	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.17	0.20	ns
t_{ENH}	REN, WEN hold time	0.12	0.14	ns
t_{BKS}	BLK setup time	0.28	0.33	ns
t_{BKH}	BLK hold time	0.02	0.03	ns
t_{DS}	Input data (DIN) setup time	0.22	0.26	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.84	2.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.15	3.33	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.08	1.27	ns
t_{C2CWWL}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.28	0.33	ns
t_{C2CWWH}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to rising edge	0.26	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.38	0.45	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.42	0.49	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.11	1.31	ns
	RESET Low to data out Low on DOUT (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.26	0.30	ns
t_{CYC}	Clock cycle time	3.89	4.57	ns
F_{MAX}	Maximum frequency	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VQ100	
Pin Number	**A3P250 Function**
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	**A3P250 Function**
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	**A3P250 Function**
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

FG896	
Pin Number	A3PE3000L Function
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0

FG896	
Pin Number	A3PE3000L Function
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3

FG896	
Pin Number	A3PE3000L Function
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0

FG896	
Pin Number	**A3PE3000L Function**
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND

FG896	
Pin Number	**A3PE3000L Function**
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7
R11	VCC
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4

FG896	
Pin Number	**A3PE3000L Function**
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND

FG896	
Pin Number	**A3PE3000L Function**
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	VCC
V21	VCCIB3
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2
V26	IO126NDB3V1
V27	IO129NDB3V1
V28	IO127NDB3V1
V29	IO125NDB3V1
V30	IO123PDB3V1
W1	IO266NDB6V4
W2	IO262NDB6V3
W3	IO260NDB6V3
W4	IO252NDB6V2
W5	IO251NDB6V2
W6	IO251PDB6V2
W7	IO255NDB6V2
W8	IO249PPB6V1
W9	IO253PDB6V2
W10	VCCIB6
W11	VCC
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND