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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p1000-1pqg208m

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2 – Military ProASIC3/EL DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage for A3PE600/3000L DC output buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VMV	DC input buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+150	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4 on page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Table 2-4 on page 2-3](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).

Table 2-2 • Recommended Operating Conditions ¹

Symbol	Parameter		Military	Units
T _J	Junction temperature		–55 to 125 ²	°C
VCC	1.5 V DC core supply voltage ³		1.425 to 1.575	V
	1.2 V – 1.5 V wide range DC core supply voltage ⁴		1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	V
VPUMP ⁵	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation ⁶	0 to 3.6	V
VCCPLL ⁵	Analog power supply (PLL)	1.5 V DC core supply voltage ³	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage ⁴	1.14 to 1.575	V
VCCI and VMV ⁵	1.2 V DC supply voltage ⁴		1.14 to 1.26	V
	1.2 V wide range DC supply voltage ⁴		1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.0 V DC supply voltage ⁷		2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. Default Junction Temperature Range in the Libero SoC software is set from 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the [Libero SoC Online Help](#).
3. For A3P250 and A3P1000
4. For A3PE600L and A3PE3000L devices only, operating at VCCI ≥ VCC.
5. See the ["Pin Descriptions and Packaging" section on page 3-1](#) for instructions and recommendations on tie-off and supply grouping.
6. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-25 on page 2-22](#). VCCI should be at the same voltage within a given I/O bank.
7. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.
8. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C) ²	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits¹

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot (125°C) ²
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.82 V
3.3 V	10%	0.69 V
	5%	0.79 V
3.6 V	10%	N/A
	5%	N/A

Notes:

1. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
2. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#).

There are five regions to consider during power-up.

Military ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#)).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

Table 2-18 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	141.97
3.3 V LVCMOS Wide Range	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.82
LVPECL	–	3.3	19.54	167.55

Notes:

1. Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.
2. PDC7 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CCI}.

Table 2-19 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	125.97
3.3 V LVCMOS – Wide Range	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.
2. PDC7 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CCI}.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-23 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-24 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

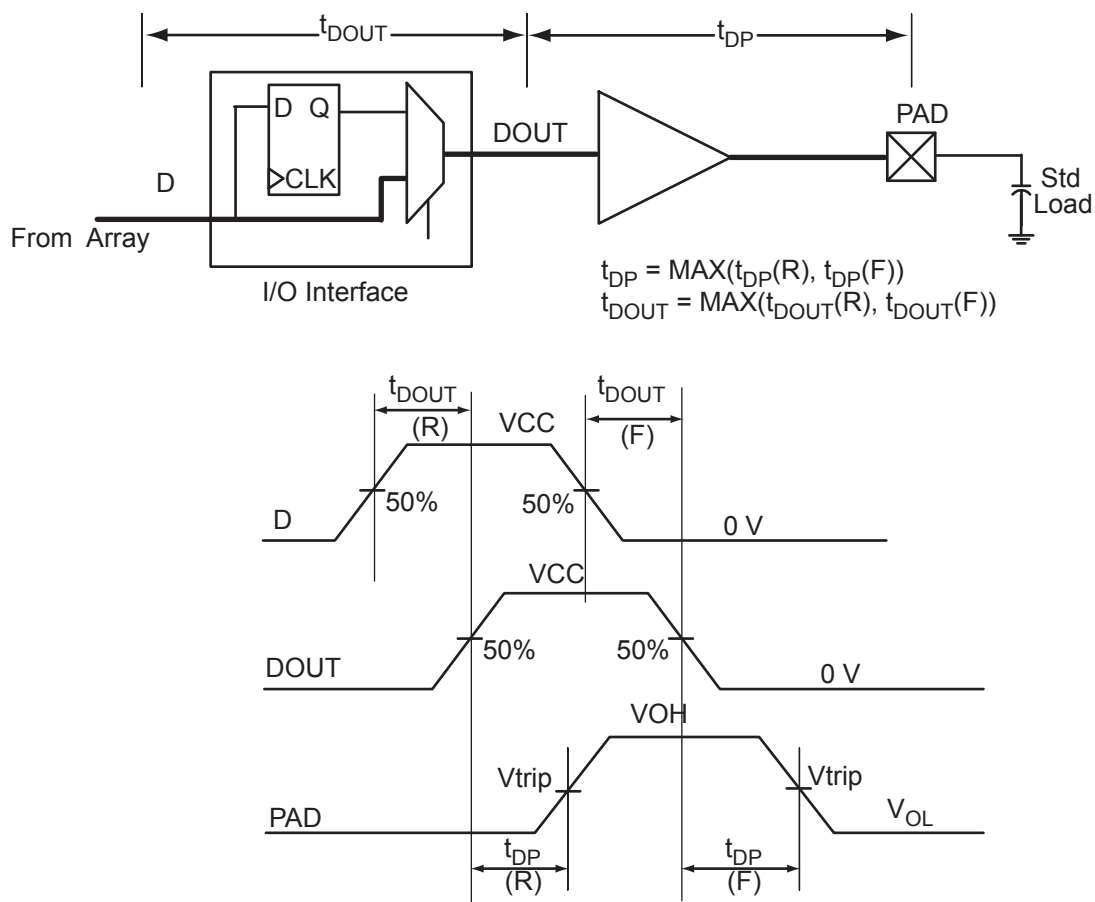


Figure 2-5 • Output Buffer Model and Delays (example)

1.2 V Core Operating Voltage

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst Case $V_{CC} = 1.14\text{ V}$, Worst Case V_{CCI}
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.09	0.05	1.49	2.03	0.44	2.12	1.56	2.76	3.06	3.99	3.43
3.3 V LVCMOS Wide Range ³	100 μA	12 mA	High	5	–	0.68	3.01	0.04	1.86	2.69	0.44	3.01	2.22	4.03	4.42	4.89	4.09
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.12	0.04	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.71	0.04	1.86	2.61	0.44	2.76	2.24	3.34	3.69	4.63	4.12
1.2 V LVCMOS	2 mA	2 mA	High	5	–	0.68	4.39	0.04	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
1.2 V LVCOMS Wide Range ⁴	100 μA	2 mA	High	5	–	0.68	4.39	0.04	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
3.3 V PCI	Per PCI spec	–	High	10	25 ⁵	0.68	2.37	0.04	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁵	0.68	2.37	0.04	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V GTL	20 mA ⁶	20 mA ⁶	High	10	25	0.68	1.75	0.05	1.99	–	0.44	1.71	1.75	–	–	3.59	3.62
2.5 V GTL	20 mA ⁶	20 mA ⁶	High	10	25	0.68	1.79	0.05	1.93	–	0.44	1.82	1.79	–	–	3.70	3.67
3.3 V GTL+	35 mA	35 mA	High	10	25	0.68	1.74	0.05	1.99	–	0.44	1.76	1.73	–	–	3.64	3.61
2.5 V GTL+	33 mA	33 mA	High	10	25	0.68	1.86	0.05	1.93	–	0.44	1.89	1.77	–	–	3.77	3.64
HSTL (I)	8 mA	8 mA	High	20	25	0.68	2.68	0.05	2.34	–	0.44	2.73	2.65	–	–	4.60	4.52
HSTL (II)	15 mA ⁶	15 mA ⁶	High	20	50	0.68	2.55	0.05	2.34	–	0.44	2.59	2.28	–	–	4.47	4.16
SSTL2 (I)	15 mA	15 mA	High	30	25	0.68	1.80	0.05	1.78	–	0.44	1.82	1.55	–	–	1.82	1.55
SSTL2 (II)	15 mA	15 mA	High	30	50	0.68	1.83	0.05	1.78	–	0.44	1.86	1.49	–	–	1.86	1.49
SSTL3 (I)	14 mA	14 mA	High	30	25	0.68	1.95	0.05	1.71	–	0.44	1.98	1.55	–	–	1.98	1.55
SSTL3 (II)	21 mA	21 mA	High	30	50	0.68	1.75	0.05	1.71	–	0.44	1.77	1.41	–	–	1.77	1.41
LVDS	24 mA	–	High	–	–	0.68	1.59	0.05	2.11	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.68	1.51	0.05	1.84	–	–	–	–	–	–	–	–

Notes:

- Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
- Output drive strength is below JEDEC specification.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.5 V Core Voltage

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$, Worst Case VCCI
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71
3.3 V LVCOMS Wide Range ³	100 μA	12 mA	High	5	–	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.01	0.03	1.49	1.93	0.34	2.02	1.65	2.71	2.78	3.27	2.89
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39
3.3 V PCI	Per PCI spec	–	High	10	25 ⁴	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁴	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V GTL	20 mA ⁵	20 mA ⁵	High	10	25	0.52	1.68	0.03	1.79	–	0.34	1.58	1.68	–	–	2.83	2.92
2.5 V GTL	20 mA ⁵	20 mA ⁵	High	10	25	0.52	1.72	0.03	1.73	–	0.34	1.69	1.72	–	–	2.93	2.97
3.3 V GTL+	35 mA	35 mA	High	10	25	0.52	1.66	0.03	1.79	–	0.34	1.63	1.66	–	–	2.88	2.90
2.5 V GTL+	33 mA	33 mA	High	10	25	0.52	1.75	0.03	1.73	–	0.34	1.76	1.69	–	–	3.00	2.94
HSTL (I)	8 mA	8 mA	High	20	25	0.52	2.57	0.03	2.14	–	0.34	2.59	2.55	–	–	3.84	3.79
HSTL (II)	15 mA ⁵	15 mA ⁵	High	20	50	0.52	2.44	0.03	2.14	–	0.34	2.46	2.19	–	–	3.71	3.43
SSTL2 (I)	15 mA	15 mA	High	30	25	0.52	1.68	0.03	1.58	–	0.34	1.69	1.46	–	–	1.69	1.46
SSTL2 (II)	18 mA	18 mA	High	30	50	0.52	1.72	0.03	1.58	–	0.34	1.73	1.39	–	–	1.73	1.39
SSTL3 (I)	14 mA	14 mA	High	30	25	0.52	1.83	0.03	1.51	–	0.34	1.84	1.45	–	–	1.84	1.45
SSTL3 (II)	21 mA	21 mA	High	30	50	0.52	1.63	0.03	1.51	–	0.34	1.64	1.31	–	–	1.64	1.31
LVDS	24 mA	–	High	–	–	0.52	1.48	0.03	1.86	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.52	1.40	0.03	1.61	–	–	–	–	–	–	–	–

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
- Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
- Output drive strength is below JEDEC specification.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Military-Case Conditions: TJ = 125°C, Worst Case VCC = 1.425 V,
Worst Case VCCI
Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF) ²	External Resistor	t _{DOU} (ns)	t _{DP} (ns)	t _{DIN} (ns)	t _{PY} (ns)	t _{EOUT} (ns)	t _{ZL} (ns)	t _{ZH} (ns)	t _{LZ} (ns)	t _{HZ} (ns)	t _{ZLS} (ns)	t _{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56
3.3 V LVCMOS Wide Range ³	100 µA	12 mA	High	5	–	0.54	2.94	0.04	1.42	0.39	2.94	2.22	4.03	4.66	6.12	5.40
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.8 V LVCMOS	8 mA	8 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.5 V LVCMOS	4 mA	4 mA	High	5	–	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32
3.3 V PCI	Per PCI spec.	–	High	10	25 ⁴	0.54	2.16	0.04	0.80	0.39	2.20	1.60	2.61	3.01	4.29	3.69
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25 ⁴	0.54	2.16	0.04	0.78	0.39	2.20	1.60	2.61	3.01	4.29	3.69

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software. Software default load is higher.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-14 on page 2-71](#) for connectivity. This resistor is not required during normal operation.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Detailed I/O DC Characteristics

Table 2-35 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

1.5 V DC Core Voltage

Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	5.90	0.04	1.45	2.09	0.40	5.98	4.73	2.52	2.24	7.45	6.19	ns
	–1	0.52	5.02	0.03	1.23	1.78	0.34	5.09	4.02	2.15	1.90	6.34	5.27	ns
8 mA	Std.	0.61	4.80	0.04	1.45	2.09	0.40	4.86	4.02	2.87	2.85	6.32	5.49	ns
	–1	0.52	4.08	0.03	1.23	1.78	0.34	4.13	3.42	2.44	2.43	5.38	4.67	ns
12 mA	Std.	0.61	4.02	0.04	1.45	2.09	0.40	4.06	3.49	3.09	3.23	5.53	4.96	ns
	–1	0.52	3.42	0.03	1.23	1.78	0.34	3.46	2.97	2.63	2.75	4.70	4.22	ns
16 mA	Std.	0.61	3.79	0.04	1.45	2.09	0.40	3.84	3.38	3.14	3.34	5.30	4.84	ns
	–1	0.52	3.23	0.03	1.23	1.78	0.34	3.26	2.87	2.67	2.84	4.51	4.12	ns
24 mA	Std.	0.61	3.67	0.04	1.45	2.09	0.40	3.72	3.39	3.20	3.74	5.18	4.86	ns
	–1	0.52	3.13	0.03	1.23	1.78	0.34	3.16	2.88	2.72	3.18	4.41	4.13	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-53 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	3.26	0.04	1.45	2.09	0.40	3.30	2.48	2.52	2.38	4.76	3.95	ns
	–1	0.52	2.77	0.03	1.23	1.78	0.34	2.80	2.11	2.15	2.03	4.05	3.36	ns
8 mA	Std.	0.61	2.66	0.04	1.45	2.09	0.40	2.68	1.97	2.87	3.00	4.15	3.43	ns
	–1	0.52	2.26	0.03	1.23	1.78	0.34	2.28	1.67	2.44	2.55	3.53	2.92	ns
12 mA	Std.	0.61	2.32	0.04	1.45	2.09	0.40	2.33	1.72	3.09	3.40	3.80	3.18	ns
	–1	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71	ns
16 mA	Std.	0.61	2.26	0.04	1.45	2.09	0.40	2.28	1.67	3.15	3.51	3.74	3.14	ns
	–1	0.52	1.92	0.03	1.23	1.78	0.34	1.94	1.42	2.68	2.98	3.18	2.67	ns
24 mA	Std.	0.61	2.28	0.04	1.45	2.09	0.40	2.30	1.61	3.21	3.90	3.77	3.07	ns
	–1	0.52	1.94	0.03	1.23	1.78	0.34	1.96	1.37	2.73	3.32	3.20	2.61	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-66 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.63	9.67	0.05	1.70	0.45	9.67	8.03	4.50	4.18	13.40	11.77	ns
		–1	0.54	8.22	0.04	1.44	0.39	8.22	6.83	3.83	3.55	11.40	10.01	ns
100 μA	6 mA	Std.	0.63	8.13	0.05	1.70	0.45	8.13	6.95	5.07	5.17	11.86	10.69	ns
		–1	0.54	6.91	0.04	1.44	0.39	6.91	5.92	4.31	4.40	10.09	9.09	ns
100 μA	8 mA	Std.	0.63	8.13	0.05	1.70	0.45	8.13	6.95	5.07	5.17	11.86	10.69	ns
		–1	0.54	6.91	0.04	1.44	0.39	6.91	5.92	4.31	4.40	10.09	9.09	ns
100 μA	12 mA	Std.	0.63	6.96	0.05	1.70	0.45	6.96	6.15	5.45	5.81	10.70	9.89	ns
		–1	0.54	5.92	0.04	1.44	0.39	5.92	5.24	4.64	4.94	9.10	8.41	ns
100 μA	16 mA	Std.	0.63	6.61	0.05	1.70	0.45	6.61	5.96	5.54	5.97	10.34	9.70	ns
		–1	0.54	5.62	0.04	1.44	0.39	5.62	5.07	4.71	5.08	8.80	8.25	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-67 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.63	5.49	0.05	1.70	0.45	5.49	4.23	4.51	4.44	9.22	7.97	ns
		–1	0.54	4.67	0.04	1.44	0.39	4.57	3.60	3.83	3.78	7.84	6.78	ns
100 μA	6 mA	Std.	0.63	4.56	0.05	1.70	0.45	4.56	3.42	5.08	5.45	8.29	7.15	ns
		–1	0.54	3.88	0.04	1.44	0.39	3.88	2.91	4.32	4.64	7.05	6.08	ns
100 μA	8 mA	Std.	0.63	4.56	0.05	1.70	0.45	4.56	3.42	5.08	5.45	8.29	7.15	ns
		–1	0.54	3.88	0.04	1.44	0.39	3.88	2.91	4.32	4.64	7.05	6.08	ns
100 μA	12 mA	Std.	0.63	4.08	0.05	1.70	0.45	4.08	3.03	5.46	6.09	7.81	6.76	ns
		–1	0.54	3.47	0.04	1.44	0.39	3.47	2.57	4.65	5.18	6.64	5.75	ns
100 μA	16 mA	Std.	0.63	4.00	0.05	1.70	0.45	4.00	2.96	5.55	6.26	7.73	6.69	ns
		–1	0.54	3.40	0.04	1.44	0.39	3.40	2.51	4.72	5.32	6.58	5.69	ns

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-92 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	–1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	–1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-93 • 1.8 V LVCMOS High Slew
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	–1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	–1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-106 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

1.2 V LVCMOS ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ²	IIH ³
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. ⁴ mA	Max. ⁴ mA	μA ⁵	μA ⁵
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD	15	15

Notes:

1. Applicable to A3PE600L and A3PE3000L devices only.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 125°C junction temperature.
6. Software default selection highlighted in gray.

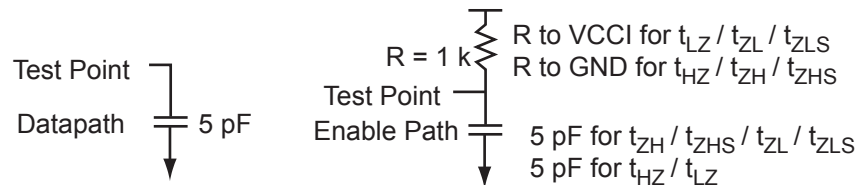


Figure 2-12 • AC Loading

Table 2-107 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C _{LOAD} (pF)
0	1.2	0.6	—	5

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Table 2-155 • SSTL3 Class I

Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.15	0.04	1.77	0.40	2.17	1.70	—	—	2.17	1.70	ns
–1	0.52	1.83	0.03	1.51	0.34	1.84	1.45	—	—	1.84	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

SSTL3 Class II

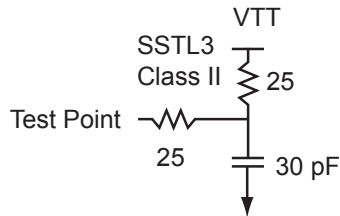
Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
21 mA	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCI} - 0.9$	21	21	103	109	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.


Figure 2-24 • AC Loading
Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.2$	$V_{REF} + 0.2$	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip} . See [Table 2-29 on page 2-25](#) for a complete table of trip points.

Timing Characteristics

Table 2-158 • SSTL3 Class II

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$, $V_{REF} = 1.5\text{ V}$
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.00	0.52	2.08	1.65	—	—	2.08	1.65	ns
–1	0.68	1.75	0.05	1.71	0.44	1.77	1.41	—	—	1.77	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

PQ208	
Pin Number	A3P1000 Function
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1

PQ208	
Pin Number	A3P1000 Function
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

PQ208	
Pin Number	A3P1000 Function
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG484		FG484	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
Y3	NC	AA16	IO122RSB2
Y4	IO182RSB2	AA17	IO119RSB2
Y5	GND	AA18	IO117RSB2
Y6	IO177RSB2	AA19	NC
Y7	IO174RSB2	AA20	NC
Y8	VCC	AA21	VCCIB1
Y9	VCC	AA22	GND
Y10	IO154RSB2	AB1	GND
Y11	IO148RSB2	AB2	GND
Y12	IO140RSB2	AB3	VCCIB2
Y13	NC	AB4	IO180RSB2
Y14	VCC	AB5	IO176RSB2
Y15	VCC	AB6	IO173RSB2
Y16	NC	AB7	IO167RSB2
Y17	NC	AB8	IO162RSB2
Y18	GND	AB9	IO156RSB2
Y19	NC	AB10	IO150RSB2
Y20	NC	AB11	IO145RSB2
Y21	NC	AB12	IO144RSB2
Y22	VCCIB1	AB13	IO132RSB2
AA1	GND	AB14	IO127RSB2
AA2	VCCIB3	AB15	IO126RSB2
AA3	NC	AB16	IO123RSB2
AA4	IO181RSB2	AB17	IO121RSB2
AA5	IO178RSB2	AB18	IO118RSB2
AA6	IO175RSB2	AB19	NC
AA7	IO169RSB2	AB20	VCCIB2
AA8	IO166RSB2	AB21	GND
AA9	IO160RSB2	AB22	GND
AA10	IO152RSB2		
AA11	IO146RSB2		
AA12	IO139RSB2		
AA13	IO133RSB2		
AA14	NC		
AA15	NC		

FG896	
Pin Number	A3PE3000L Function
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0

FG896	
Pin Number	A3PE3000L Function
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3

FG896	
Pin Number	A3PE3000L Function
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0

FG896	
Pin Number	A3PE3000L Function
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	VCC IB0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2

FG896	
Pin Number	A3PE3000L Function
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2