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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

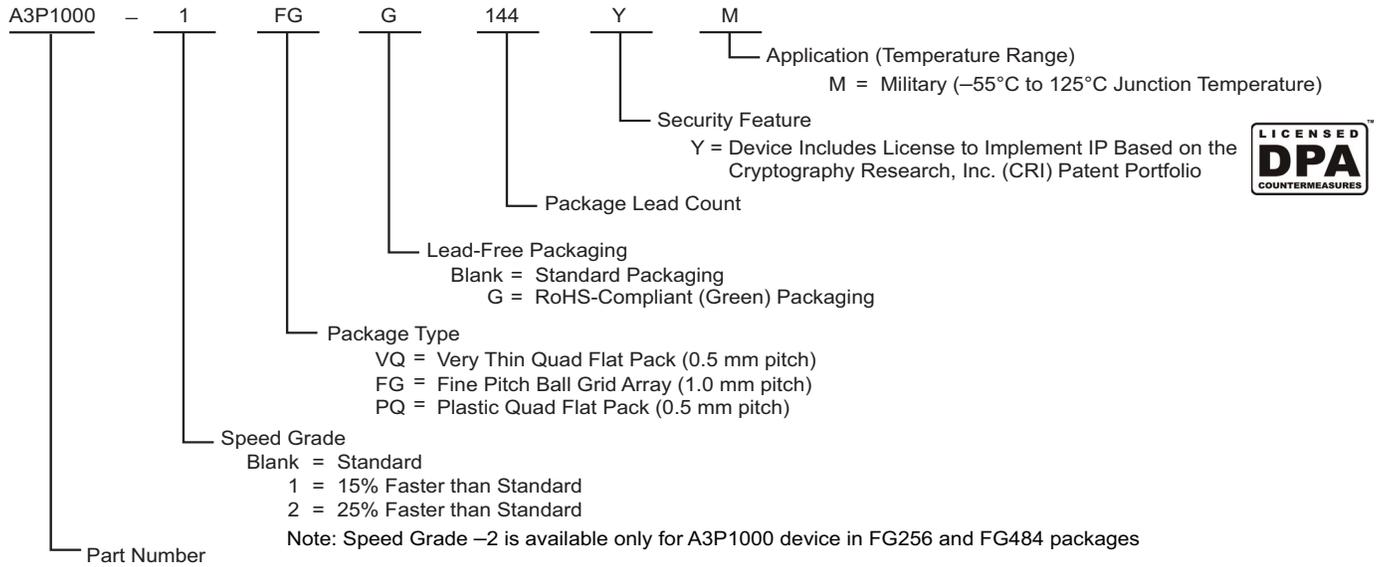
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p1000-fg144m

Military ProASIC3/EL Ordering Information



Military ProASIC3/EL Devices

A3P250 = 250,000 System Gates
 A3PE600L = 600,000 System Gates
 A3P1000 = 1,000,000 System Gates
 A3PE3000L = 3,000,000 System Gates

Military ProASIC3/EL Devices with ARM Cortex-M1

M1A3P1000 = 1,000,000 System Gates
 M1A3PE3000L = 3,000,000 System Gates

Temperature Grade Offerings

Package	A3P250	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices			M1A3P1000	M1A3PE3000L
VQ100	M	-	-	-
PQ208	-	-	M	-
FG144	-	-	M	-
FG256	-	-	M	-
FG484	-	M	M	M
FG896	-	-	-	M

Note: M = Military temperature range: -55°C to 125°C junction temperature

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-23 on page 2-17](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-23 on page 2-17](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-23 on page 2-17](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-23 on page 2-17](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-24 on page 2-17](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-24 on page 2-17](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC13 * F_{CLKOUT}$ product) to the total PLL contribution.

Table 2-54 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	6.25	0.05	1.12	0.45	6.37	5.29	2.91	2.70	8.83	7.75	ns
	-1	0.54	5.32	0.04	0.95	0.39	5.42	4.50	2.47	2.30	7.51	6.59	ns
6 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	-1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
8 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	-1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
12 mA	Std.	0.63	4.50	0.05	1.12	0.45	4.59	4.05	3.53	3.76	7.05	6.51	ns
	-1	0.54	3.83	0.04	0.95	0.39	3.90	3.45	3.00	3.20	5.99	5.54	ns
16 mA	Std.	0.63	4.27	0.05	1.12	0.45	4.35	3.93	3.58	3.86	6.81	6.39	ns
	-1	0.54	3.63	0.04	0.95	0.39	3.70	3.34	3.05	3.29	5.79	5.43	ns
24 mA	Std.	0.63	4.14	0.05	1.12	0.45	4.22	3.97	3.65	4.27	6.68	6.43	ns
	-1	0.54	3.53	0.04	0.95	0.39	3.59	3.38	3.10	3.63	5.68	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-55 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.55	0.05	1.12	0.45	3.62	2.79	2.91	2.87	6.07	5.25	ns
	-1	0.54	3.02	0.04	0.95	0.39	3.08	2.37	2.48	2.44	5.17	4.46	ns
6 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	-1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
8 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	-1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
12 mA	Std.	0.63	2.64	0.05	1.12	0.45	2.68	1.99	3.53	3.94	5.14	4.45	ns
	-1	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79	ns
16 mA	Std.	0.63	2.58	0.05	1.12	0.45	2.63	1.95	3.59	4.05	5.09	4.41	ns
	-1	0.54	2.20	0.04	0.95	0.39	2.24	1.66	3.05	3.44	4.33	3.75	ns
24 mA	Std.	0.63	2.61	0.05	1.12	0.45	2.66	1.89	3.66	4.46	5.12	4.35	ns
	-1	0.54	2.22	0.04	0.95	0.39	2.26	1.61	3.11	3.80	4.35	3.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

3.3 V LVCMOS Wide Range

Table 2-58 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	25	27	15	15
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	25	27	15	15
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	51	54	15	15
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	103	109	15	15
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	132	127	15	15
100 μA	24 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	268	181	15	15

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
- I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
- Currents are measured at 125°C junction temperature.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.
- Software default selection highlighted in gray.

Table 2-59 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	25	27	15	15
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	25	27	15	15
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	51	54	15	15
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	51	54	15	15
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	103	109	15	15
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100	100	132	127	15	15

Notes:

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
- I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
- I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
- Currents are measured at 125°C junction temperature.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.
- Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-70 • Minimum and Maximum DC Input and Output Levels
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	15	15
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	15	15
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	15	15
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	83	87	15	15
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	169	124	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-71 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	15	15
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	15	15
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	15	15
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	15	15
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	15	15
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	15	15
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.

1.5 V DC Core Voltage
Table 2-88 • 1.8 V LVCMOS Low Slew
**Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	-1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	-1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	-1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	-1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	-1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	-1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • 1.8 V LVCMOS High Slew
**Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	-1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	-1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	-1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.61	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	-1	0.52	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	-1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	-1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

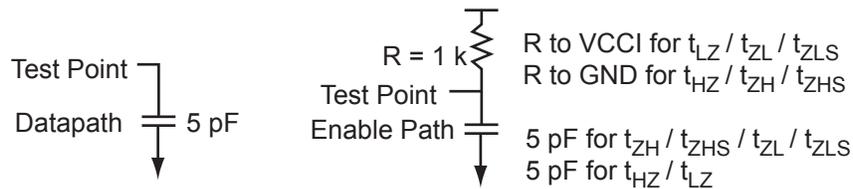
1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-96 • Minimum and Maximum DC Input and Output Levels
 Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.
5. Software default selection highlighted in gray.


Figure 2-11 • AC Loading
Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C _{LOAD} (pF)
0	1.5	0.75	–	5

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
8 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	32	39	15	15

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 125°C junction temperature.

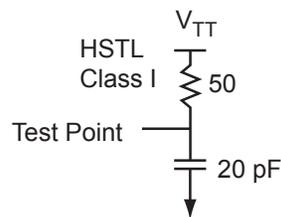


Figure 2-19 • AC Loading

Table 2-137 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = V_{trip} . See Table 2-29 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-138 • HSTL Class I

Military-Case Conditions: $T_j = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V,

Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.80	3.15	0.05	2.76	0.52	3.20	3.11	-	-	5.41	5.32	ns
-1	0.68	2.68	0.05	2.34	0.44	2.73	2.65	-	-	4.60	4.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-162 • LVDS

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.80	1.87	0.05	2.48	ns
-1	0.68	1.59	0.05	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.5 V DC Core Voltage

Table 2-163 • LVDS

Military-Case Conditions: $T_J = 125^\circ\text{C}$, VCC = 1.425 V, Worst-Case VCCI = 2.3 V
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.61	1.75	0.04	2.18	ns
-1	0.52	1.48	0.03	1.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-164 • LVDS

Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	2.07	0.05	1.82	ns
-1	0.54	1.76	0.04	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Timing Characteristics

Table 2-178 • Output Enable Register Propagation Delays
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

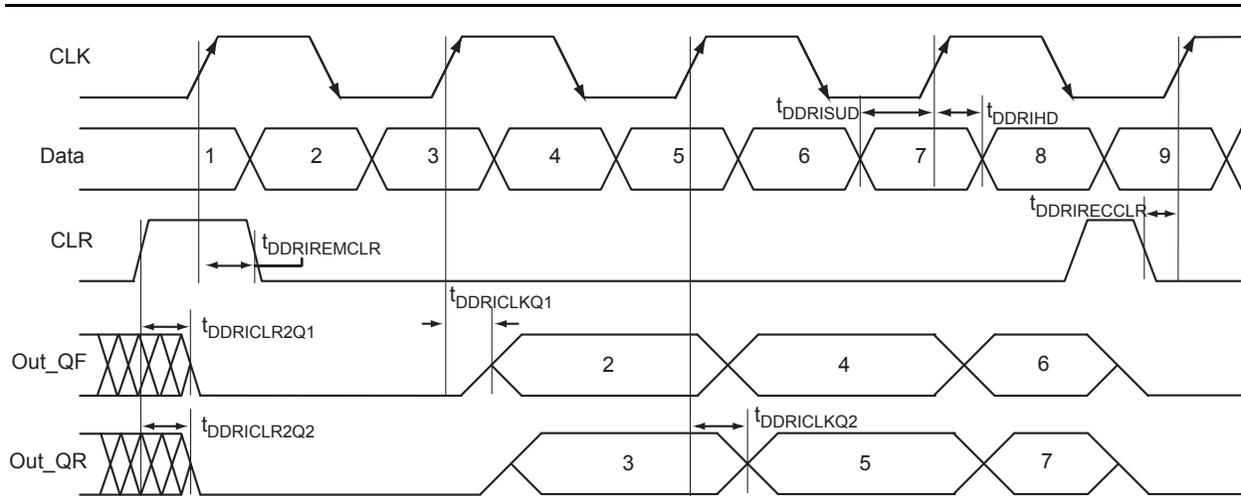
Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.62	0.72	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.43	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.60	0.71	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.31	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.31	0.36	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-179 • Output Enable Register Propagation Delays
 Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.47	0.55	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.33	0.39	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.46	0.54	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.


Figure 2-34 • Input DDR Timing Diagram

Timing Characteristics

Table 2-182 • Input DDR Propagation Delays

 Military-Case Conditions: $T_j = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.38	0.45	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.54	0.63	ns
t_{DDRISUD1}	Data Setup for Input DDR (fall)	0.39	0.46	ns
t_{DDRISUD2}	Data Setup for Input DDR (rise)	0.34	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (fall)	0.00	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.64	0.75	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.79	0.93	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.31	0.36	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	160	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-187 • Output DDR Propagation Delays
Military-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$ for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.74	0.87	ns
t_{DDRISUD1}	Data_F Data Setup for Output DDR	0.40	0.47	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.40	0.47	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.00	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
F_{DDROMAX}	Maximum Frequency for the Output DDR	250	250	MHz

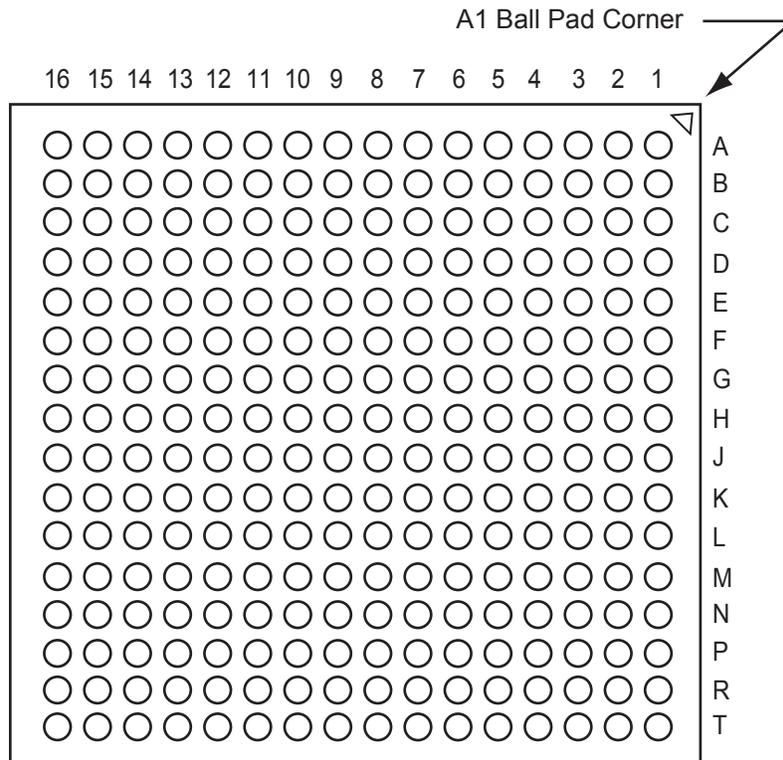
Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-188 • Output DDR Propagation Delays
Military-Case Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$ for A3P250 and A3P1000

Parameter	Description	-1	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.84	0.99	ns
t_{DDRISUD1}	Data_F Data Setup for Output DDR	0.46	0.54	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.46	0.54	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.13	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
F_{DDROMAX}	Maximum Frequency for the Output DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG256	
Pin Number	A3P1000 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	A3P1000 Function
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

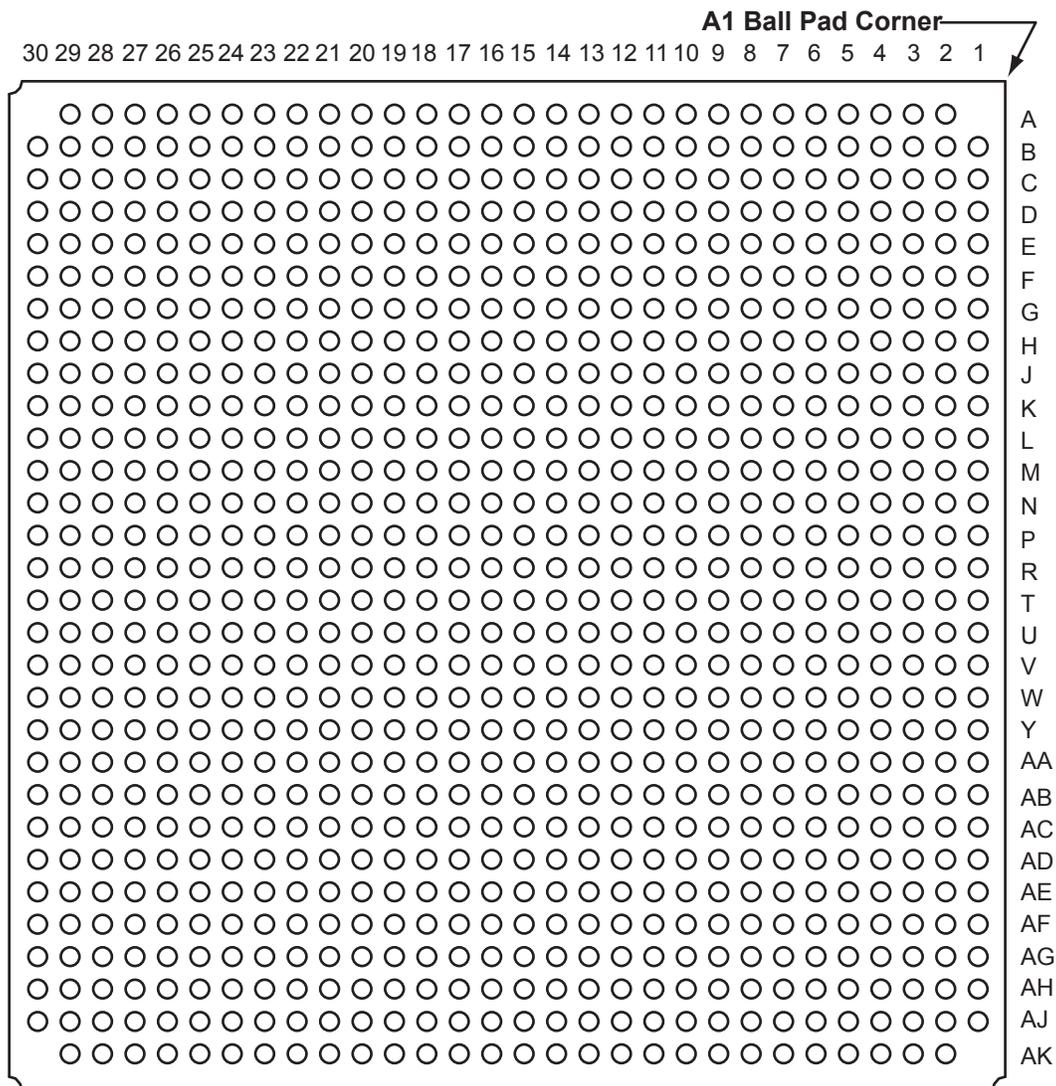
FG256	
Pin Number	A3P1000 Function
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG256	
Pin Number	A3P1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484		FG484		FG484	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
A1	GND	B14	NC	D5	GAA0/IO00NDB0V0
A2	GND	B15	NC	D6	GAA1/IO00PDB0V0
A3	VCCIB0	B16	IO30NDB1V1	D7	GAB0/IO01NDB0V0
A4	IO06NDB0V1	B17	IO30PDB1V1	D8	IO05PDB0V0
A5	IO06PDB0V1	B18	IO32PDB1V1	D9	IO10PDB0V1
A6	IO08NDB0V1	B19	NC	D10	IO12PDB0V2
A7	IO08PDB0V1	B20	NC	D11	IO16NDB0V2
A8	IO11PDB0V1	B21	VCCIB2	D12	IO23NDB1V0
A9	IO17PDB0V2	B22	GND	D13	IO23PDB1V0
A10	IO18NDB0V2	C1	VCCIB7	D14	IO28NDB1V1
A11	IO18PDB0V2	C2	NC	D15	IO28PDB1V1
A12	IO22PDB1V0	C3	NC	D16	GBB1/IO34PDB1V1
A13	IO26PDB1V0	C4	NC	D17	GBA0/IO35NDB1V1
A14	IO29NDB1V1	C5	GND	D18	GBA1/IO35PDB1V1
A15	IO29PDB1V1	C6	IO04NDB0V0	D19	GND
A16	IO31NDB1V1	C7	IO04PDB0V0	D20	NC
A17	IO31PDB1V1	C8	VCC	D21	NC
A18	IO32NDB1V1	C9	VCC	D22	NC
A19	NC	C10	IO14NDB0V2	E1	NC
A20	VCCIB1	C11	IO19NDB0V2	E2	NC
A21	GND	C12	NC	E3	GND
A22	GND	C13	NC	E4	GAB2/IO133PDB7V1
B1	GND	C14	VCC	E5	GAA2/IO134PDB7V1
B2	VCCIB7	C15	VCC	E6	GNDQ
B3	NC	C16	NC	E7	GAB1/IO01PDB0V0
B4	IO03NDB0V0	C17	NC	E8	IO05NDB0V0
B5	IO03PDB0V0	C18	GND	E9	IO10NDB0V1
B6	IO07NDB0V1	C19	NC	E10	IO12NDB0V2
B7	IO07PDB0V1	C20	NC	E11	IO16PDB0V2
B8	IO11NDB0V1	C21	NC	E12	IO20NDB1V0
B9	IO17NDB0V2	C22	VCCIB2	E13	IO24NDB1V0
B10	IO14PDB0V2	D1	NC	E14	IO24PDB1V0
B11	IO19PDB0V2	D2	NC	E15	GBC1/IO33PDB1V1
B12	IO22NDB1V0	D3	NC	E16	GBB0/IO34NDB1V1
B13	IO26NDB1V0	D4	GND	E17	GNDQ

FG484		FG484		FG484	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GND	B14	IO58RSB0	D5	GAA0/IO00RSB0
A2	GND	B15	IO63RSB0	D6	GAA1/IO01RSB0
A3	VCCIB0	B16	IO66RSB0	D7	GAB0/IO02RSB0
A4	IO07RSB0	B17	IO68RSB0	D8	IO16RSB0
A5	IO09RSB0	B18	IO70RSB0	D9	IO22RSB0
A6	IO13RSB0	B19	NC	D10	IO28RSB0
A7	IO18RSB0	B20	NC	D11	IO35RSB0
A8	IO20RSB0	B21	VCCIB1	D12	IO45RSB0
A9	IO26RSB0	B22	GND	D13	IO50RSB0
A10	IO32RSB0	C1	VCCIB3	D14	IO55RSB0
A11	IO40RSB0	C2	IO220PDB3	D15	IO61RSB0
A12	IO41RSB0	C3	NC	D16	GBB1/IO75RSB0
A13	IO53RSB0	C4	NC	D17	GBA0/IO76RSB0
A14	IO59RSB0	C5	GND	D18	GBA1/IO77RSB0
A15	IO64RSB0	C6	IO10RSB0	D19	GND
A16	IO65RSB0	C7	IO14RSB0	D20	NC
A17	IO67RSB0	C8	VCC	D21	NC
A18	IO69RSB0	C9	VCC	D22	NC
A19	NC	C10	IO30RSB0	E1	IO219NDB3
A20	VCCIB0	C11	IO37RSB0	E2	NC
A21	GND	C12	IO43RSB0	E3	GND
A22	GND	C13	NC	E4	GAB2/IO224PDB3
B1	GND	C14	VCC	E5	GAA2/IO225PDB3
B2	VCCIB3	C15	VCC	E6	GNDQ
B3	NC	C16	NC	E7	GAB1/IO03RSB0
B4	IO06RSB0	C17	NC	E8	IO17RSB0
B5	IO08RSB0	C18	GND	E9	IO21RSB0
B6	IO12RSB0	C19	NC	E10	IO27RSB0
B7	IO15RSB0	C20	NC	E11	IO34RSB0
B8	IO19RSB0	C21	NC	E12	IO44RSB0
B9	IO24RSB0	C22	VCCIB1	E13	IO51RSB0
B10	IO31RSB0	D1	IO219PDB3	E14	IO57RSB0
B11	IO39RSB0	D2	IO220NDB3	E15	GBC1/IO73RSB0
B12	IO48RSB0	D3	NC	E16	GBB0/IO74RSB0
B13	IO54RSB0	D4	GND	E17	IO71RSB0

FG896



Note: This is the bottom view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG896	
Pin Number	A3PE3000L Function
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4

FG896	
Pin Number	A3PE3000L Function
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0

FG896	
Pin Number	A3PE3000L Function
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1

FG896	
Pin Number	A3PE3000L Function
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND