Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p1000-fgg144m

1 – Military ProASIC3/EL Device Family Overview

General Description

The military ProASIC3/EL family of flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single chip, 1.2 V to 1.5 V core and I/O operation, reprogrammability, and advanced features.

Microsemi's proven Flash*Freeze technology enables military ProASIC3EL device users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies, and retaining internal states of the device. This greatly simplifies power management. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives military ProASIC3/EL devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). Military ProASIC3/EL devices offer dramatic dynamic power savings, giving FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Military ProASIC3/EL devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). Military ProASIC3/EL devices support devices from 250K system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 military ProASIC3/EL devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 military ProASIC3/EL device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available at no cost from Microsemi for use in M1 military ProASIC3/EL FPGAs.

The ARM-enabled devices have ordering numbers that begin with M1 and do not support AES decryption.

Flash*Freeze Technology[†]

Military ProASIC3EL devices offer Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. When Flash*Freeze mode is activated, military ProASIC3EL devices enter a static state while retaining the contents of registers and SRAM. Power is conserved without the need for additional external components to turn off I/Os or clocks. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of military ProASIC3EL devices to support a 1.2 V core voltage allows for an even greater reduction in power consumption, which enables low total system power.

When the military ProASIC3EL device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make military ProASIC3EL devices suitable for low-power data transfer and manipulation in military-temperature applications where available power may be limited (e.g., in battery-powered equipment); or where heat dissipation may be limited (e.g., in enclosures with no forced cooling).

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† Flash*Freeze technology is not supported on A3P1000.

Flash Advantages

Low Power[f]

The military ProASIC3EL family of flash-based FPGAs provides a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

Military ProASIC3EL devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the power-driven layout (PDL) feature in Libero$^®$SoC offers up to 30% additional power reduction. With Flash*Freeze technology, military ProASIC3EL device is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich, and high-performance solution.

Security

Nonvolatile, flash-based military ProASIC3/EL devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. Military ProASIC3/EL devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Military ProASIC3/EL devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in military ProASIC3/EL devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. Military ProASIC3/EL devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Military ProASIC3/EL devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the military ProASIC3/EL family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The military ProASIC3/EL family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A military ProASIC3/EL device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based military ProASIC3/EL FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

Flash-based military ProASIC3/EL devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based military ProASIC3/EL devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the military ProASIC3/EL device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based military ProASIC3/EL devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

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f A3P1000 only supports 1.5 V core operation.

User Nonvolatile FlashROM

Military ProASIC3/EL devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

FlashROM is written using the standard military ProASIC3/EL IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Microsemi military ProASIC3/EL development software solutions, Libero SoC has extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Military ProASIC3/EL devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Military ProASIC3 devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the military ProASIC3 family contains six CCCs, located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

Military ProASIC3EL devices also contain six CCCs; however, all six are equipped with a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

Table 2-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits[1]**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot (125°C)[2]
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.82 V
3.3 V	10%	0.69 V
	5%	0.79 V
3.6 V	10%	N/A
	5%	N/A

Notes:

1. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

Military ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
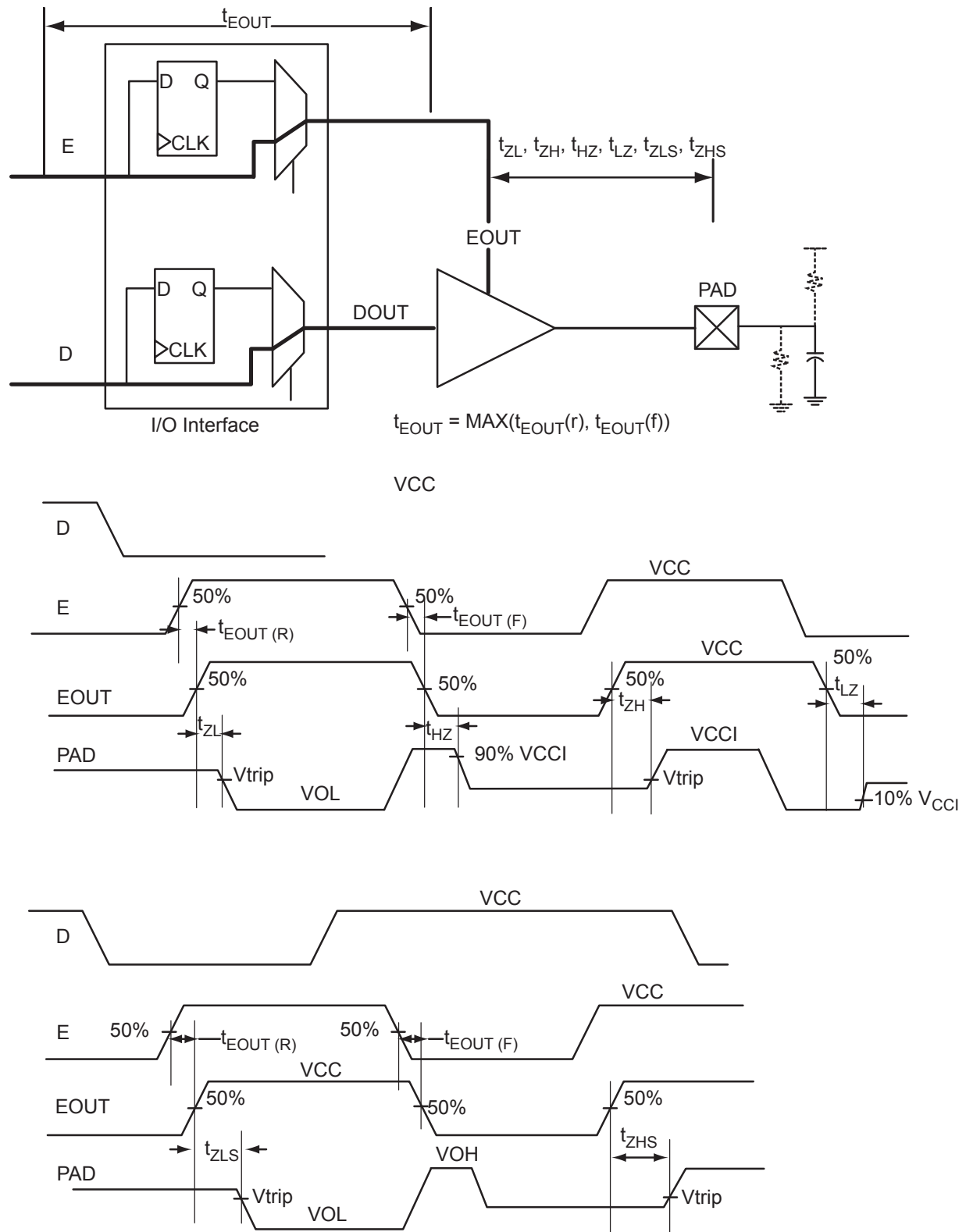
$$t_{EOUT} = MAX(t_{EOUT}(r), t_{EOUT}(f))$$

Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-60 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard Plus I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA 5	µA 5
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	103	109	15	15
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	132	127	15	15

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.

2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4. Currents are measured at 125°C junction temperature.

5. All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.

6. Software default selection highlighted in gray.

Figure 2-8 • **AC Loading**

Table 2-61 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_LOAD (pF)
0	3.3	1.4	–	5

Note: *Measuring point = $V_{trip.}$ See Table 2-29 on page 2-25 for a complete table of trip points.

Table 2-84 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	15	15
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	15	15
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	15	15
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	35	44	15	15

Notes:

1. I_{IL} *is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < VIN < VIL.*

2. I_{IH} *is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

3. *Currents are measured at 100°C junction temperature and maximum voltage.*

4. *Currents are measured at 125°C junction temperature.*

5. *Software default selection highlighted in gray.*

Test Point

Datapath ═ 5 pF

R = 1 k
Test Point
Enable Path ═

R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}
R to GND for t_{HZ} / t_{ZH} / t_{ZHS}

5 pF for t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}
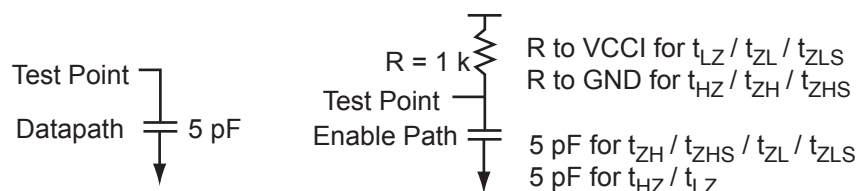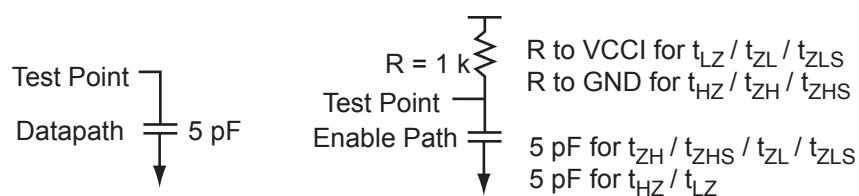5 pF for t_{HZ} / t_{LZ}

Figure 2-10 • **AC Loading**

Table 2-85 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	5

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-86 • **1.8 V LVCMOS Low Slew**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	Std.	0.80	9.16	0.05	2.00	2.82	0.52	9.32	7.69	2.77	1.20	11.53	9.89	ns
	−1	0.68	7.79	0.05	1.70	2.40	0.44	7.93	6.54	2.36	1.02	9.81	8.42	ns
4 mA	Std.	0.80	7.55	0.05	2.00	2.82	0.52	7.68	6.48	3.23	2.76	9.88	8.68	ns
	−1	0.68	6.42	0.05	1.70	2.40	0.44	6.53	5.51	2.75	2.35	8.41	7.38	ns
6 mA	Std.	0.80	6.40	0.05	2.00	2.82	0.52	6.51	5.65	3.54	3.34	8.71	7.85	ns
	−1	0.68	5.44	0.05	1.70	2.40	0.44	5.54	4.80	3.01	2.84	7.41	6.68	ns
8 mA	Std.	0.80	6.01	0.05	2.00	2.82	0.52	6.12	5.48	3.61	3.50	8.32	7.69	ns
	−1	0.68	5.11	0.05	1.70	2.40	0.44	5.20	4.66	3.07	2.98	7.08	6.54	ns
12 mA	Std.	0.80	5.90	0.05	2.00	2.82	0.52	6.00	5.49	3.71	4.08	8.21	7.70	ns
	−1	0.68	5.02	0.05	1.70	2.40	0.44	5.11	4.67	3.16	3.47	6.98	6.55	ns
16 mA	Std.	0.80	5.90	0.05	2.00	2.82	0.52	6.00	5.49	3.71	4.08	8.21	7.70	ns
	−1	0.68	5.02	0.05	1.70	2.40	0.44	5.11	4.67	3.16	3.47	6.98	6.55	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-87 • **1.8 V LVCMOS High Slew**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	Std.	0.80	4.14	0.05	2.00	2.82	0.52	4.21	4.05	2.76	1.23	6.42	6.26	ns
	−1	0.68	3.52	0.05	1.70	2.40	0.44	3.58	3.45	2.35	1.04	5.46	5.32	ns
4 mA	Std.	0.80	3.36	0.05	2.00	2.82	0.52	3.41	3.01	3.22	2.85	5.62	5.21	ns
	−1	0.68	2.86	0.05	1.70	2.40	0.44	2.90	2.56	2.74	2.42	4.78	4.43	ns
6 mA	Std.	0.80	2.88	0.05	2.00	2.82	0.52	2.93	2.49	3.54	3.43	5.13	4.70	ns
	−1	0.68	2.45	0.05	1.70	2.40	0.44	2.49	2.12	3.01	2.92	4.36	3.99	ns
8 mA	Std.	0.80	2.79	0.05	2.00	2.82	0.52	2.83	2.40	3.60	3.59	5.04	4.60	ns
	−1	0.68	2.37	0.05	1.70	2.40	0.44	2.41	2.04	3.06	3.05	4.29	3.91	ns
12 mA	Std.	0.80	2.78	0.05	2.00	2.82	0.52	2.82	2.28	3.71	4.21	5.02	4.48	ns
	−1	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81	ns
16 mA	Std.	0.80	2.78	0.05	2.00	2.82	0.52	2.82	2.28	3.71	4.21	5.02	4.48	ns
	−1	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-177 • **Output Data Register Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t$_{OCLKQ}$	Clock-to-Q of the Output Data Register	0.71	0.83	ns
t$_{OSUD}$	Data Setup Time for the Output Data Register	0.38	0.44	ns
t$_{OHD}$	Data Hold Time for the Output Data Register	0.00	0.00	ns
t$_{OSUE}$	Enable Setup Time for the Output Data Register	0.53	0.62	ns
t$_{OHE}$	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t$_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	0.97	1.14	ns
t$_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	0.97	1.14	ns
t$_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t$_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t$_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t$_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t$_{OWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t$_{OWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t$_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
t$_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-187 • **Output DDR Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t$_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.74	0.87	ns
t$_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.40	0.47	ns
t$_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.40	0.47	ns
t$_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
t$_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
t$_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.00	ns
t$_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
t$_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
t$_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
t$_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
t$_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
F$_{DDROMAX}$	Maximum Frequency for the Output DDR	250	250	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-188 • **Output DDR Propagation Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t$_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.84	0.99	ns
t$_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.46	0.54	ns
t$_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.46	0.54	ns
t$_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
t$_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
t$_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.13	ns
t$_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
t$_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
t$_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
t$_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
t$_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
F$_{DDROMAX}$	Maximum Frequency for the Output DDR	309	263	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

Table 2-192 • **Register Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	−1	Std.	Units
t$_{CLKQ}$	Clock-to-Q of the Core Register	0.76	0.90	ns
t$_{SUD}$	Data Setup Time for the Core Register	0.59	0.70	ns
t$_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
t$_{SUE}$	Enable Setup Time for the Core Register	0.63	0.74	ns
t$_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
t$_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.55	0.65	ns
t$_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.55	0.65	ns
t$_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t$_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.31	0.36	ns
t$_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t$_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.31	0.36	ns
t$_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t$_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t$_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t$_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-194 • **Register Delays**
Military-Case Conditions: T$_J$ = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	−1	Std.	Units
t$_{CLKQ}$	Clock-to-Q of the Core Register	0.66	0.78	ns
t$_{SUD}$	Data Setup Time for the Core Register	0.52	0.61	ns
t$_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
t$_{SUE}$	Enable Setup Time for the Core Register	0.55	0.64	ns
t$_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
t$_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.48	0.56	ns
t$_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.48	0.56	ns
t$_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t$_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.27	0.31	ns
t$_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t$_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.27	0.31	ns
t$_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t$_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t$_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.41	0.48	ns
t$_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-207 • **RAM512X18**
Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t$_{AS}$	Address setup time	0.26	0.31	ns
t$_{AH}$	Address hold time	0.00	0.00	ns
t$_{ENS}$	REN, WEN setup time	0.10	0.11	ns
t$_{ENH}$	REN, WEN hold time	0.06	0.07	ns
t$_{DS}$	Input data (WD) setup time	0.19	0.23	ns
t$_{DH}$	Input data (WD) hold time	0.00	0.00	ns
t$_{CKQ1}$	Clock High to new data valid on RD (output retained, WMODE = 0)	2.29	2.69	ns
t$_{CKQ2}$	Clock High to new data valid on RD (pipelined)	0.95	1.12	ns
t$_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t$_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t$_{RSTBQ}$	RESET Low to data out Low on RD (flow through)	0.98	1.15	ns
	RESET Low to data out Low on RD (pipelined)	0.98	1.15	ns
t$_{REMRSTB}$	RESET removal	0.30	0.36	ns
t$_{RECRSTB}$	RESET recovery	1.59	1.87	ns
t$_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t$_{CYC}$	Clock cycle time	5.39	6.20	ns
F$_{MAX}$	Maximum frequency	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-213 • **FIFO Worst Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3P250 (512×8)**

Parameter	Description	–1	Std.	Units
t$_{ENS}$	REN, WEN Setup Time	4.52	5.31	ns
t$_{ENH}$	REN, WEN Hold Time	0.00	0.00	ns
t$_{BKS}$	BLK Setup Time	1.66	1.95	ns
t$_{BKH}$	BLK Hold Time	0.00	0.00	ns
t$_{DS}$	Input Data (WD) Setup Time	0.22	0.26	ns
t$_{DH}$	Input Data (WD) Hold Time	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on RD (flow-through)	2.61	3.06	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on RD (pipelined)	1.14	1.34	ns
t$_{RCKEF}$	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t$_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t$_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t$_{RSTFG}$	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t$_{RSTAF}$	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t$_{RSTBQ}$	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t$_{REMRSTB}$	RESET Removal	0.34	0.40	ns
t$_{RECRSTB}$	RESET Recovery	1.81	2.12	ns
t$_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t$_{CYC}$	Clock Cycle Time	3.89	4.57	ns
F$_{MAX}$	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-216 • **FIFO Worst Military-Case Conditions: T$_J$ = 125°C, VCC = 1.425 V for A3P250 (4k×1)**

Parameter	Description	–1	Std.	Units
t$_{ENS}$	REN, WEN Setup Time	5.85	6.87	ns
t$_{ENH}$	REN, WEN Hold Time	0.00	0.00	ns
t$_{BKS}$	BLK Setup Time	1.66	1.95	ns
t$_{BKH}$	BLK Hold Time	0.00	0.00	ns
t$_{DS}$	Input Data (WD) Setup Time	0.22	0.26	ns
t$_{DH}$	Input Data (WD) Hold Time	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on RD (flow-through)	2.84	3.33	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on RD (pipelined)	1.08	1.27	ns
t$_{RCKEF}$	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t$_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t$_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t$_{RSTFG}$	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t$_{RSTAF}$	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t$_{RSTBQ}$	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
t$_{REMRSTB}$	RESET Removal	0.34	0.40	ns
t$_{RECRSTB}$	RESET Recovery	1.81	2.12	ns
t$_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t$_{CYC}$	Clock Cycle Time	3.89	4.57	ns
F$_{MAX}$	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.
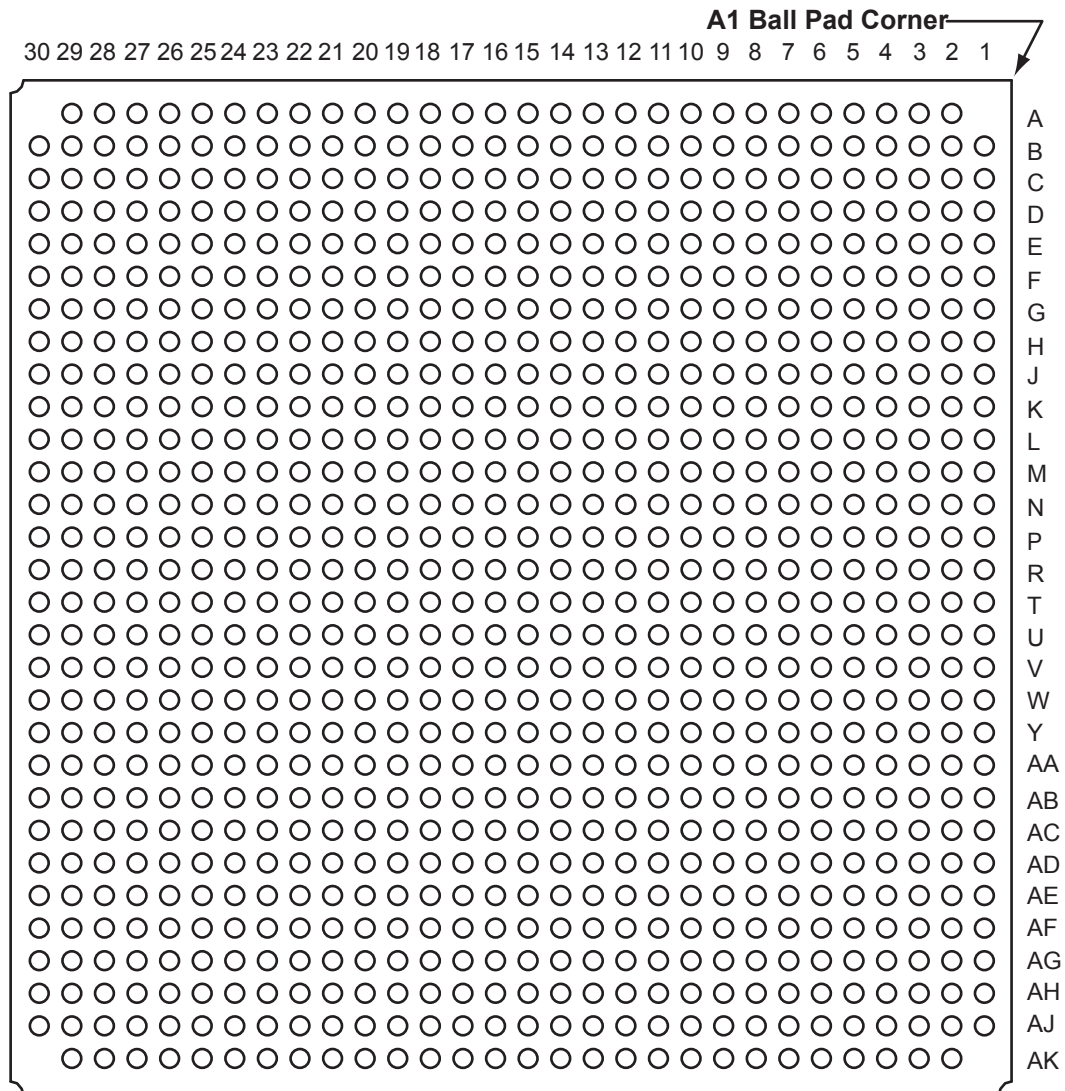
FG484	
Pin Number	A3P1000 Function
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC

FG484	
Pin Number	A3P1000 Function
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2

FG484	
Pin Number	A3P1000 Function
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3

FG896

A1 Ball Pad Corner

Note: This is the bottom view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/products/fpga-soc/solutions.

FG896	
Pin Number	**A3PE3000L Function**
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND

FG896	
Pin Number	A3PE3000L Function
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

Revision	Changes	Page
Revision 5 (September 2014)	Updated FG896 package in the "I/Os Per Package [1]" table (SAR34171).	I-II
	Removed reference to JTAG interface operated at 3.3 V from "Advanced Architecture" section (SAR 34686).	1-4
	Fixed table note (1) in Table 2-1 (SAR 47815).	2-1
	Deleted ambient temp row and modified notes in Table 2-2 (SAR 59413).	2-2
	Removed "5 V-tolerant input buffer and push-pull output buffer" from "2.5 V LVCMOS" section" (SAR 24916).	2-49
	Removed table notes referencing +/-5% and 350mV differential voltage from Table 2-160 (SAR 34810).	2-86
	DDR frequency added to Table 2-182, Table 2-183, Table 2-184, Table 2-186, Table 2-187, Table 2-188 (SAR 56034).	2-105–2-109
	Table note (3) added to Table 2-201 and Table 2-202 to clarify delay increments (SAR 34821).	2-123
	Terminology clarified in Table 2-203, Table 2-204, Table 2-205, Table 2-206, Table 2-207, Table 2-208, Table 2-209, Table 2-210, Table 2-211, Table 2-212, Table 2-213, Table 2-214, Table 2-215, Table 2-216, Figure 2-44, Figure 2-45, Figure 2-46, Figure 2-47, Figure 2-48, and Figure 2-50 (SAR 38237).	2-129 - 2-145
	Revised statement in "VMVx I/O Supply Voltage (quiet)" section per (SAR 38324).	3-1
	Libero IDE revised to SoC throughout (SAR 40287).	N/A
Revision 4 (April 2014)	Added FG256 under A3P1000 in Table 1 • Military ProASIC3/EL Low-Power Devices, in "I/Os Per Package [1]", "Temperature Grade Offerings", "FG256" section, and Table 2-5 • Package Thermal Resistivities (SAR 56384). Added Note for Speed Grade in "Military ProASIC3/EL Ordering Information" section. Also added missing details for FG484 for A3P1000 to Table 2-5 • Package Thermal Resistivities (SAR 56384).	I, III, 2-6 and 4-9
	Added details related to Speed Grade 2 to the "Military ProASIC3/EL Ordering Information" section and the "Speed Grade and Temperature Grade Matrix" section (SAR 56384).	III
	Changed Actel references to Microsemi.	NA
Revision 3 (Sept 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
Revision 2 (June 2012)	The FG484 package was added for A3P1000 in Table 1 • Military ProASIC3/EL Low-Power Devices, the I/Os Per Package [1] table, and the "Temperature Grade Offerings" table (SAR 39010).	I, II, III
	The "FG484" pin table for A3P1000 has been added (SAR 39010).	4-19