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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p1000-pqg208m

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Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based military ProASIC3/EL devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The military ProASIC3/EL family device architecture mitigates the need for ASIC migration at higher volumes. This makes the military ProASIC3/EL family a cost-effective ASIC replacement.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of military ProASIC3/EL flash-based FPGAs. Once it is programmed, the flash cell configuration element of military ProASIC3/EL FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The military ProASIC3/EL family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary military ProASIC3/EL architecture provides granularity comparable to standard-cell ASICs. The military ProASIC3/EL device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the military ProASIC3/EL core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Military	Units
T_J	Junction temperature		–55 to 125 [2]	°C
VCC	1.5 V DC core supply voltage[3]		1.425 to 1.575	V
	1.2 V – 1.5 V wide range DC core supply voltage [4]		1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	V
VPUMP[5]	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation[6]	0 to 3.6	V
VCCPLL[5]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage[4]	1.14 to 1.575	V
VCCI and VMV[5]	1.2 V DC supply voltage[4]		1.14 to 1.26	V
	1.2 V wide range DC supply voltage[4]		1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.0 V DC supply voltage[7]		2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set from 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *For A3P250 and A3P1000*
4. *For A3PE600L and A3PE3000L devices only, operating at VCCI ≥ VCC.*
5. *See the "Pin Descriptions and Packaging" section on page 3-1 for instructions and recommendations on tie-off and supply grouping.*
6. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-22. VCCI should be at the same voltage within a given I/O bank.*
7. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*
8. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*

Table 2-21 • Different Components Contributing to Dynamic Power Consumption in Military ProASIC3 and ProASIC3/EL Devices at 1.5 V VCC

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)			
		A3PE3000L	A3PE600L	A3P1000	A3P250
PAC1	Clock contribution of a Global Rib	13.03	6.24	14.50	11.00
PAC2	Clock contribution of a Global Spine	6.69	3.47	2.48	1.58
PAC3	Clock contribution of a VersaTile row	1.46	1.46	0.81	0.81
PAC4	Clock contribution of a VersaTile used as a sequential module	0.13	0.13	0.12	0.12
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-14 on page 2-9 through Table 2-16 on page 2-10.			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12.			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Dynamic contribution for PLL	2.60			

Table 2-22 • Different Components Contributing to the Static Power Consumption in Military ProASIC3/EL Devices

Parameter	Definition	Device-Specific Dynamic Power (µW)			
		A3PE3000L	A3PE600L	A3P1000	A3P250
PDC0	Array static power in Sleep mode	0 mW	0 mW	N/A	N/A
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8.			
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8.			
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7.			
PDC4	Static PLL contribution at 1.2 V operating core voltage (for A3PE600L and A3PE3000L only)	1.42 mW		N/A	
	Static PLL contribution 1.5 V operating core voltage	2.55 mW			
PDC5	Bank quiescent power (V_{CCI}-dependent)	See Table 2-9 on page 2-7, Table 2-10 on page 2-7, Table 2-12 on page 2-8.			
PDC6	I/O input pin static power (standard-dependent)	See Table 2-14 on page 2-9. through Table 2-16 on page 2-10.			
PDC7	I/O output pin static power (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12.			

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in the Libero SoC.

Table 2-28 • Summary of Maximum and Minimum DC Input Levels Applicable to Military Conditions

	Military[1]	
	I_{IL}[2]	I_{IH}[3]
DC I/O Standard	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	15	15
3.3 V LVCMOS Wide Range	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS[4]	15	15
1.2 V LVCMOS Wide Range[4]	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1. *Military temperature range: –55°C to 125°C.*
2. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Applicable to Military A3PE600L and A3PE3000L devices operating at VCCI ≥ VCC.*

Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Military-Case Conditions: TJ = 125°C, Worst Case VCC = 1.425 V, Worst Case VCCI Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)[2]	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	5	–	0.54	2.94	0.04	1.42	0.39	2.94	2.22	4.03	4.66	6.12	5.40
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.8 V LVCMOS	8 mA	8 mA	High	5	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71
1.5 V LVCMOS	4 mA	4 mA	High	5	–	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32
3.3 V PCI	Per PCI spec.	–	High	10	25 [4]	0.54	2.16	0.04	0.80	0.39	2.20	1.60	2.61	3.01	4.29	3.69
3.3 V PCI-X	Per PCI-X spec.	–	High	10	25 [4]	0.54	2.16	0.04	0.78	0.39	2.20	1.60	2.61	3.01	4.29	3.69

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software. Software default load is higher.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-14 on page 2-71 for connectivity. This resistor is not required during normal operation.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Detailed I/O DC Characteristics

Table 2-35 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-46 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-82 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	35	44	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	45	51	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	91	74	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	91	74	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-83 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	45	51	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	91	74	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	91	74	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

1.5 V DC Core Voltage

Table 2-88 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	–1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	–1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	–1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	–1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	–1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	–1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	–1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.61	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	–1	0.52	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	034	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-128 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	268	181	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

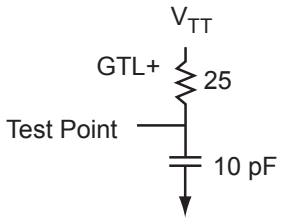

Figure 2-17 • AC Loading

Table 2-129 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-130 • 3.3 V GTL+
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.04	0.05	2.34	0.52	2.07	2.03	–	–	4.28	4.24	ns
–1	0.68	1.74	0.05	1.99	0.44	1.76	1.73	–	–	3.64	3.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-131 • 3.3 V GTL+
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.95	0.04	2.11	0.40	1.92	1.95	–	–	3.38	3.41	ns
–1	0.52	1.66	0.03	1.79	0.34	1.63	1.66	–	–	2.88	2.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-147 • SSTL2 Class I
Military-Case Conditions: T_J = 125°C, V_{CC} = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.98	0.04	1.85	0.40	1.99	1.71	–	–	1.99	1.71	ns
–1	0.52	1.68	0.03	1.58	0.34	1.69	1.46	–	–	1.69	1.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-148 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	169	124	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

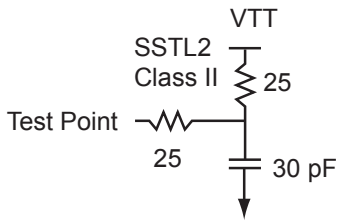

Figure 2-22 • AC Loading

Table 2-149 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-150 • SSTL2 Class II
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.15	0.05	2.09	0.52	2.18	1.75	–	–	2.18	1.75	ns
–1	0.68	1.83	0.05	1.78	0.44	1.86	1.49	–	–	1.86	1.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-155 • SSTL3 Class I
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.15	0.04	1.77	0.40	2.17	1.70	–	–	2.17	1.70	ns
–1	0.52	1.83	0.03	1.51	0.34	1.84	1.45	–	–	1.84	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	103	109	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

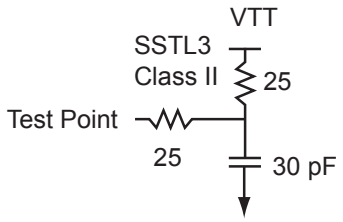

Figure 2-24 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL3 Class II
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.00	0.52	2.08	1.65	–	–	2.08	1.65	ns
–1	0.68	1.75	0.05	1.71	0.44	1.77	1.41	–	–	1.77	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-174 • Input Data Register Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	0.37	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.45	0.53	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.55	0.64	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.55	0.64	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

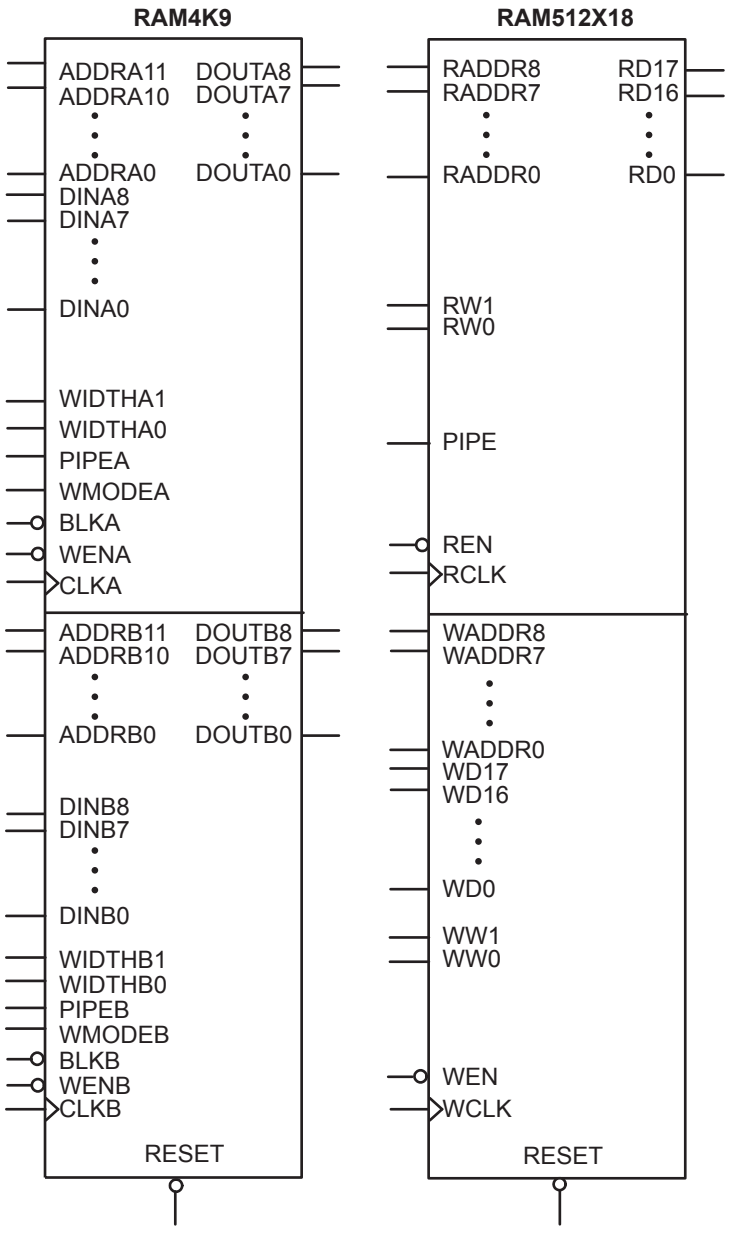

Figure 2-43 • **RAM Models**

Table 2-205 • RAM4K9
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.30	0.35	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.17	0.20	ns
t_{ENH}	REN, WEN hold time	0.12	0.14	ns
t_{BKS}	BLK setup time	0.28	0.33	ns
t_{BKH}	BLK hold time	0.02	0.03	ns
t_{DS}	Input data (DIN) setup time	0.22	0.26	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.84	2.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.15	3.33	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.08	1.27	ns
t_{C2CWWL}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.28	0.33	ns
t_{C2CWWH}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to rising edge	0.26	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.38	0.45	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.42	0.49	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.11	1.31	ns
	RESET Low to data out Low on DOUT (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.26	0.30	ns
t_{CYC}	Clock cycle time	3.89	4.57	ns
F_{MAX}	Maximum frequency	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-207 • RAM512X18
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.31	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.10	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.23	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.29	2.69	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.95	1.12	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	0.98	1.15	ns
	RESET Low to data out Low on RD (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t_{CYC}	Clock cycle time	5.39	6.20	ns
F_{MAX}	Maximum frequency	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

PQ208	
Pin Number	**A3P1000 Function**
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1

PQ208	
Pin Number	**A3P1000 Function**
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

PQ208	
Pin Number	**A3P1000 Function**
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG256	
Pin Number	**A3P1000 Function**
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3PE3000L Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3

FG484	
Pin Number	A3PE3000L Function
AA14	IO170NDB4V2
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	IO06PPB0V0
B4	IO08NDB0V0

FG484	
Pin Number	A3PE3000L Function
B5	IO08PDB0V0
B6	IO14NDB0V1
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	VCC
C9	VCC
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	VCC
C15	VCC
C16	IO70NDB1V3
C17	IO70PDB1V3

FG896	
Pin Number	**A3PE3000L Function**
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6
T11	VCC
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	VCC
T21	VCCIB3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	VCCPLC
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3