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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000l-1fg896m

I/Os Per Package [1]

ProASIC3/EL Low Power Devices	A3P250		A3PE600L		A3P1000		A3PE3000L	
ARM Cortex-M1 Devices					M1A3P1000		M1A3PE3000L	
Package	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
VQ100	68	13	–	–	–	–	–	–
PQ208	–	–	–	–	154	35	–	–
FG144	–	–	–	–	97	25	–	–
FG256	–	–	–	–	177	44	–	–
FG484	–	–	270	135	300	74	341	168
FG896	–	–	–	–	–	–	620	310

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *"G" indicates RoHS-compliant packages. Refer to "Military ProASIC3/EL Ordering Information" on page III for the location of the "G" in the part number.*
4. *For A3PE3000L devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5

Military ProASIC3/EL Device Status

2 – Military ProASIC3/EL DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage for A3PE600/3000L DC output buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VMV	DC input buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+150	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Power per I/O Pin

Table 2-14 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range	3.3	–	16.34
3.3 V LVCMOS – Schmitt trigger Wide Range	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger	1.2	–	0.53
1.2 V LVCMOS Wide Range	1.2	–	0.60
1.2 V LVCMOS Schmitt trigger Wide Range	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	0.79
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*

Power Consumption of Various Internal Resources

Table 2-20 • **Different Components Contributing to Dynamic Power Consumption in Military ProASIC3/EL Devices Operating at 1.2 V VCC**

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)	
		A3PE3000L	A3PE600L
PAC1	Clock contribution of a Global Rib	8.34	3.99
PAC2	Clock contribution of a Global Spine	4.28	2.22
PAC3	Clock contribution of a VersaTile row	0.94	0.94
PAC4	Clock contribution of a VersaTile used as a sequential module	0.08	0.08
PAC5	First contribution of a VersaTile used as a sequential module	0.05	
PAC6	Second contribution of a VersaTile used as a sequential module	0.19	
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11	
PAC8	Average contribution of a routing net	0.45	
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-14 on page 2-9 through Table 2-16 on page 2-10.	
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12.	
PAC11	Average contribution of a RAM block during a read operation	25.00	
PAC12	Average contribution of a RAM block during a write operation	30.00	
PAC13	Dynamic contribution for PLL	1.74	

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*
5. *Software default selection highlighted in gray.*

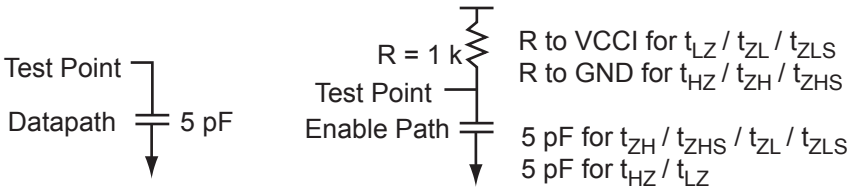


Figure 2-7 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Table 2-60 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	25	27	15	15
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	51	54	15	15
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	103	109	15	15
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	132	127	15	15

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 125°C junction temperature.*
5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.*
6. *Software default selection highlighted in gray.*

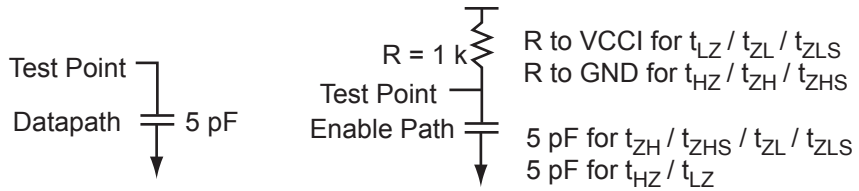


Figure 2-8 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

1.5 V DC Core Voltage

Table 2-100 • 1.5 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.39	0.04	1.88	2.77	0.40	9.54	7.77	3.22	2.47	11.00	9.24	ns
	–1	0.52	7.99	0.03	1.60	2.35	0.34	8.11	6.61	2.74	2.10	9.36	7.86	ns
4 mA	Std.	0.61	8.01	0.04	1.88	2.77	0.40	8.13	6.77	3.58	3.14	9.59	8.24	ns
	–1	0.52	6.81	0.03	1.60	2.35	0.34	6.91	5.76	3.05	2.67	8.16	7.01	ns
6 mA	Std.	0.61	7.51	0.04	1.88	2.77	0.40	7.62	6.59	3.66	3.32	9.09	8.05	ns
	–1	0.52	6.39	0.03	1.60	2.35	0.34	6.48	5.60	3.12	2.83	7.73	6.85	ns
8 mA	Std.	0.61	7.41	0.04	1.88	2.77	0.40	7.52	6.59	3.41	3.99	8.99	8.06	ns
	–1	0.52	6.30	0.03	1.60	2.35	0.34	6.40	5.61	2.90	3.40	7.64	6.85	ns
12 mA	Std.	0.61	7.41	0.04	1.88	2.77	0.40	7.52	6.59	3.41	3.99	8.99	8.06	ns
	–1	0.52	6.30	0.03	1.60	2.35	0.34	6.40	5.61	2.90	3.40	7.64	6.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-101 • 1.5 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	3.78	0.04	1.88	2.77	0.40	3.82	3.43	3.21‘	2.58	5.29	4.89	ns
	–1	0.52	3.21	0.03	1.60	2.35	0.34	3.25	2.92	2.73	2.20	4.50	4.16	ns
4 mA	Std.	0.61	3.20	0.04	1.88	2.77	0.40	3.23	2.79	3.57	3.25	4.70	4.25	ns
	–1	0.52	2.72	0.03	1.60	2.35	0.34	2.75	2.37	3.04	2.77	4.00	3.62	ns
6 mA	Std.	0.61	3.09	0.04	1.88	2.77	0.40	3.12	2.67	3.65	3.44	4.59	4.13	ns
	–1	0.52	2.63	0.03	1.60	2.35	0.34	2.65	2.27	3.11	2.93	3.90	3.52	ns
8 mA	Std.	0.61	3.05	0.04	1.88	2.77	0.40	3.09	2.52	3.77	4.14	4.55	3.98	ns
	–1	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39	ns
12 mA	Std.	0.61	3.05	0.04	1.88	2.77	0.40	3.09	2.52	3.77	4.14	4.55	3.98	ns
	–1	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

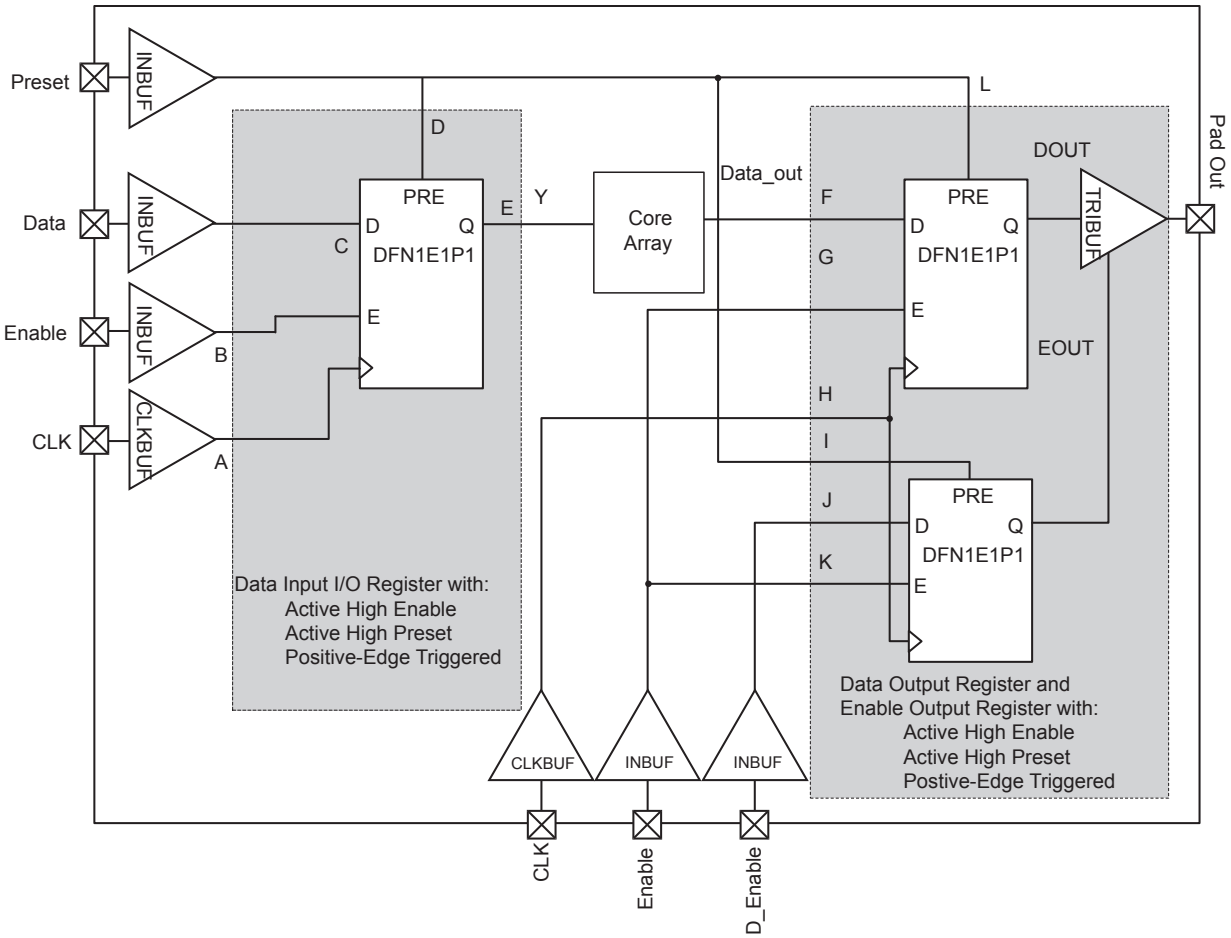


Figure 2-28 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Output Register

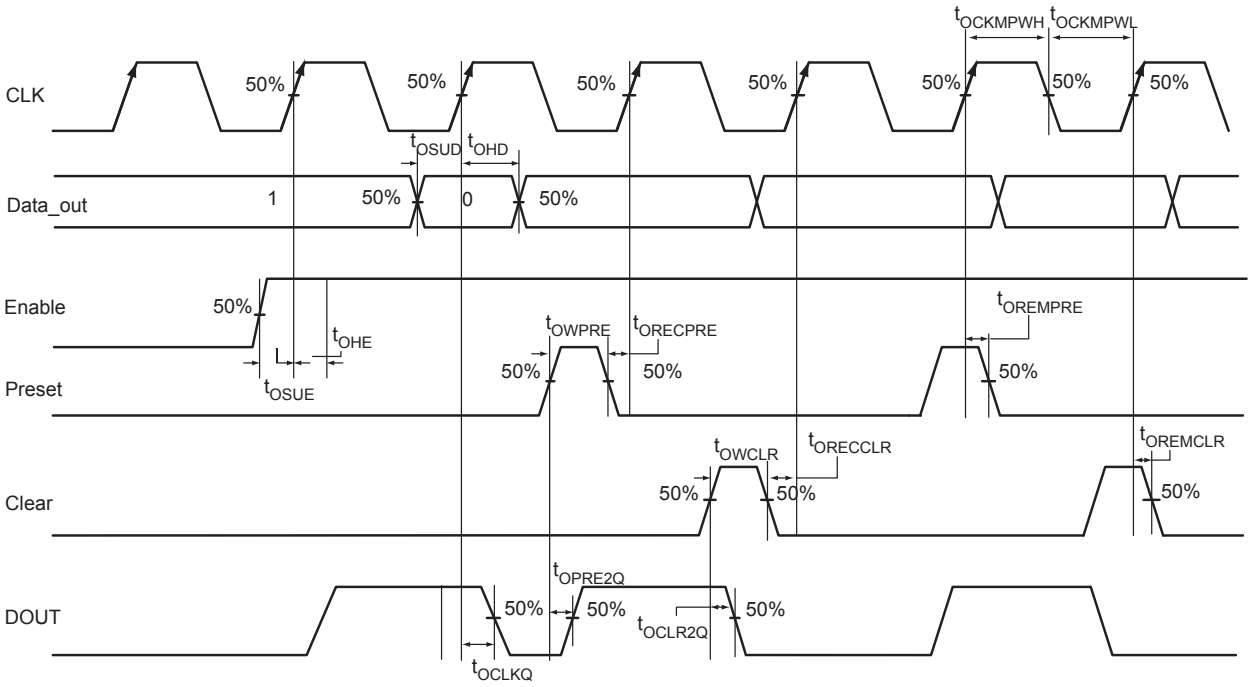


Figure 2-31 • **Output Register Timing Diagram**

Table 2-183 • Input DDR Propagation Delays
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for any A3PE600L/A3PE3000L

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.29	0.34	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.41	0.48	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.30	0.35	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.26	0.31	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.49	0.58	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.60	0.71	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	0.28	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250	250	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-184 • Input DDR Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.33	0.39	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.47	0.55	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.30	0.35	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.30	0.35	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.56	0.65	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.69	0.81	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

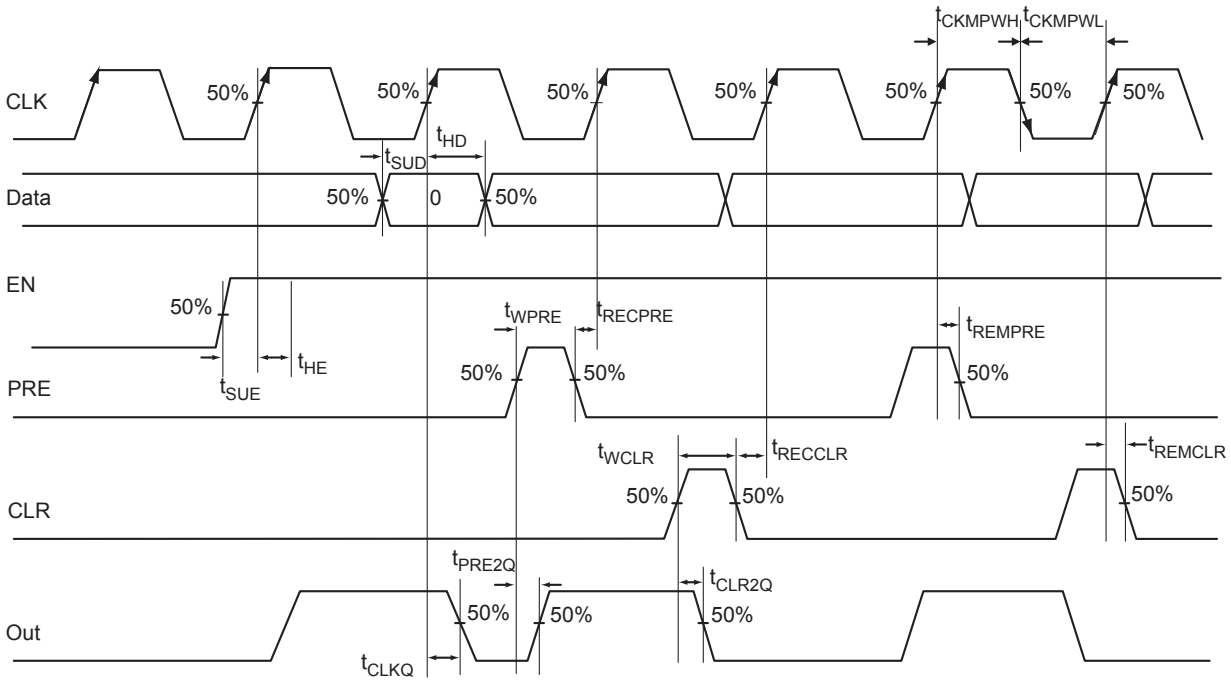


Figure 2-40 • **Timing Model and Waveforms**

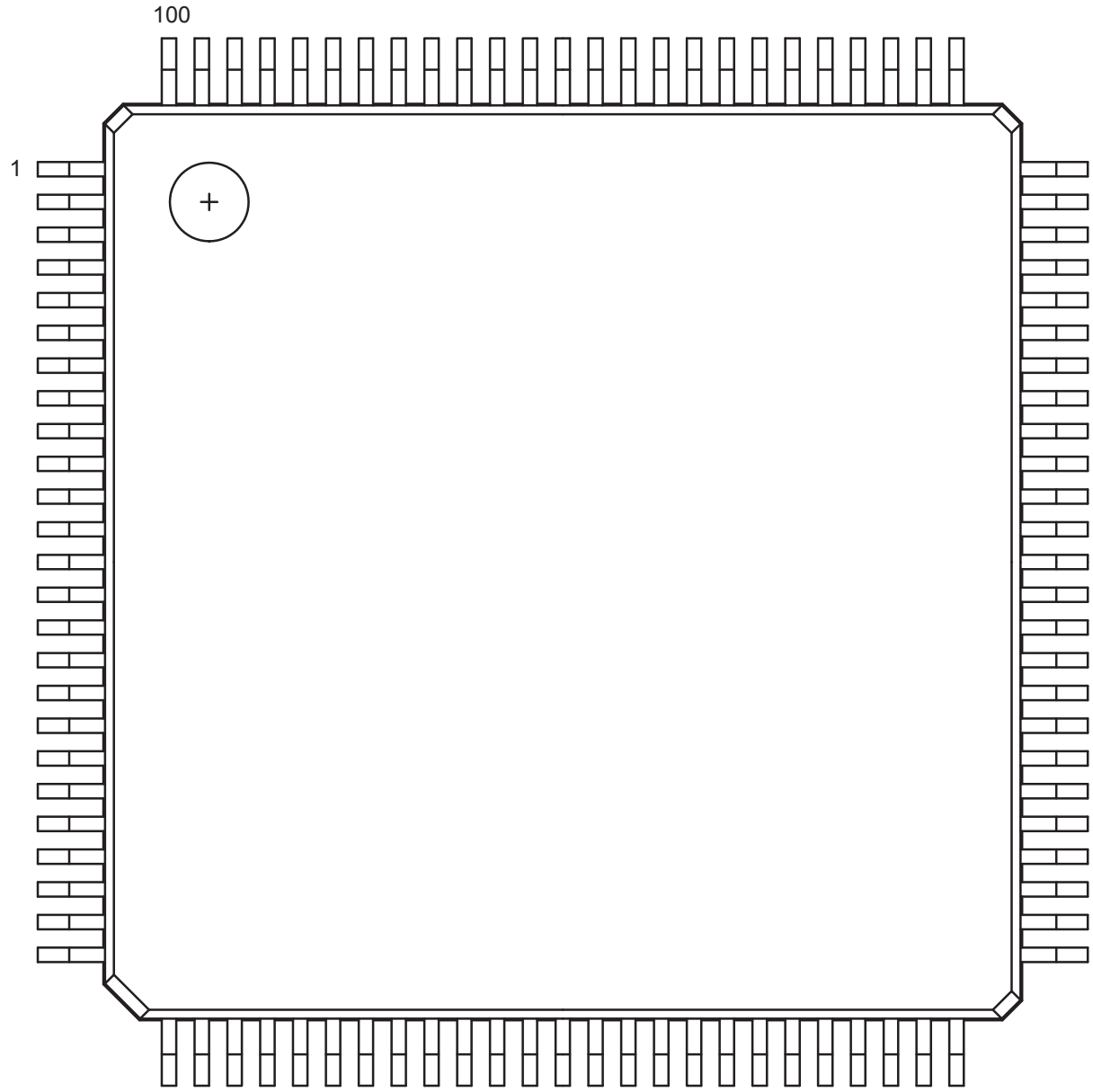
***Table 2-216* • FIFO Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3P250 (4k×1)**

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	5.85	6.87	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.84	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.08	1.27	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

4 – Package Pin Assignments

VQ100



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/products/fpga-soc/solutions.

PQ208

Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/products/fpga-soc/solutions.

FG144	
Pin Number	**A3P1000 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

FG144	
Pin Number	**A3P1000 Function**
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

FG144	
Pin Number	**A3P1000 Function**
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	**VCC**
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

FG896	
Pin Number	**A3PE3000L Function**
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	V**CCI**B0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2