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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000l-fgg896m

Military ProASIC3/EL Ordering Information

A3P1000 – 1 FG G 144 Y M

- **Part Number**
  - **Military ProASIC3/EL Devices**
    - A3P250 = 250,000 System Gates
    - A3PE600L = 600,000 System Gates
    - A3P1000 = 1,000,000 System Gates
    - A3PE3000L = 3,000,000 System Gates
  - **Military ProASIC3/EL Devices with ARM Cortex-M1**
    - M1A3P1000 = 1,000,000 System Gates
    - M1A3PE3000L = 3,000,000 System Gates
- **Speed Grade**
  - Blank = Standard
  - 1 = 15% Faster than Standard
  - 2 = 25% Faster than Standard
  - Note: Speed Grade –2 is available only for A3P1000 device in FG256 and FG484 packages
- **Package Type**
  - VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
  - PQ = Plastic Quad Flat Pack (0.5 mm pitch)
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS-Compliant (Green) Packaging
- **Package Lead Count**
- **Security Feature**
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- **Application (Temperature Range)**
  - M = Military (–55°C to 125°C Junction Temperature)

LICENSED DPA COUNTERMEASURES

Temperature Grade Offerings

Package	A3P250	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices			**M1A3P1000**	**M1A3PE3000L**
VQ100	M	–	–	–
PQ208	–	–	M	–
FG144	–	–	M	–
FG256	–	–	M	–
FG484	–	M	M	M
FG896	–	–	–	M

Note: M = Military temperature range: –55°C to 125°C junction temperature

Power per I/O Pin

Table 2-14 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range	3.3	–	16.34
3.3 V LVCMOS – Schmitt trigger Wide Range	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger	1.2	–	0.53
1.2 V LVCMOS Wide Range	1.2	–	0.60
1.2 V LVCMOS Schmitt trigger Wide Range	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	0.79
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*

Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
3.3 V LVCMOS Wide Range	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS	5	1.2	–	17.94
1.2 V LVCMOS Wide Range	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.18
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.48
SSTL3 (I)	30	3.3	26.02	114.67
SSTL3 (II)	30	3.3	42.21	131.69
Differential				
LVDS	–	2.5	7.70	89.58
LVPECL	–	3.3	19.42	167.86

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-23 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-24 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

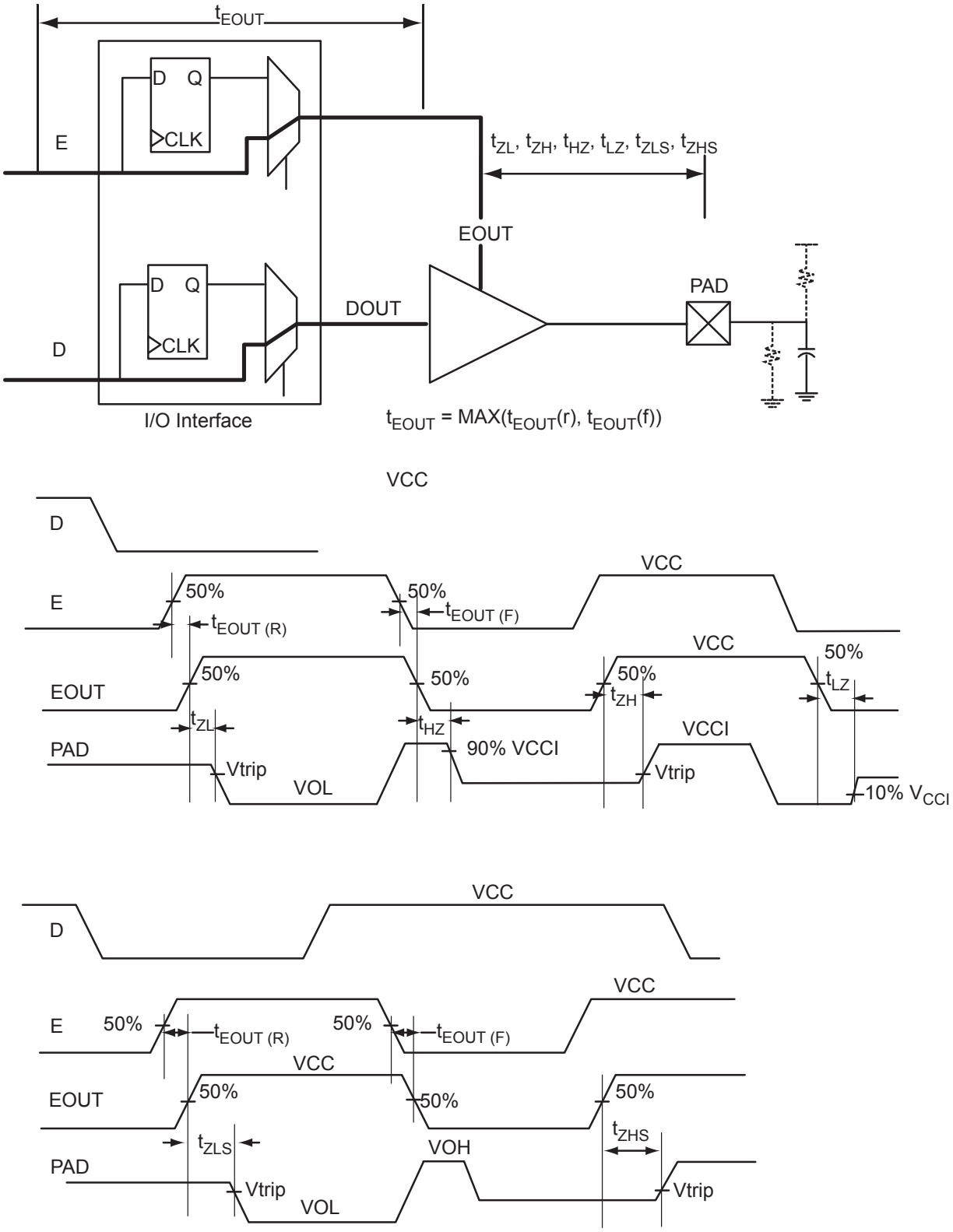

Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-40 • I/O Short Currents IOSH/IOSL
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	Drive Strength	I_{OSL} (mA)[1]	I_{OSH} (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same specification as regular LVCMOS 3.3 V	
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 µA	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X specification	Per PCI Curves	
3.3 V GTL	20 mA[2]	268	181
2.5 V GTL	20 mA[2]	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA[2]	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

Notes:

1. *T_J = 100°C*
2. *Output drive strength is below JEDEC specification.*

1.5 V DC Core Voltage

Table 2-64 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.61	8.94	0.04	1.90	2.87	0.40	8.92	7.06	3.69	3.20	10.39	8.53	ns
		–1	0.52	7.61	0.03	1.61	2.44	0.34	7.59	6.01	3.14	2.72	8.84	7.25	ns
100 µA	8 mA	Std.	0.61	7.24	0.04	1.90	2.87	0.40	7.22	5.99	4.23	4.15	8.68	7.45	ns
		–1	0.52	6.16	003	1.61	2.44	0.34	6.14	5.10	3.60	3.53	7.39	6.34	ns
100 µA	12 mA	Std.	0.61	6.03	0.04	1.90	2.87	0.40	6.01	5.19	4.58	4.74	7.47	6.65	ns
		–1	0.52	5.13	0.03	1.61	2.44	0.34	5.11	4.41	3.89	4.03	6.36	5.66	ns
100 µA	16 mA	Std.	0.61	5.68	0.04	1.90	2.87	0.40	5.66	5.01	4.65	4.91	7.13	6.47	ns
		–1	0.52	4.83	0.03	1.61	2.44	0.34	4.82	4.26	3.95	4.18	6.06	5.51	ns
100 µA	24 mA	Std.	0.61	5.50	0.04	1.90	2.87	0.40	5.48	5.03	4.74	5.53	6.95	6.49	ns
		–1	0.52	4.68	0.03	1.61	2.44	0.34	4.66	4.28	4.04	4.70	5.91	5.52	ns

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges ONLY.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-65 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.61	4.86	0.04	1.90	2.87	0.40	4.84	3.65	3.69	3.43	6.31	5.12	ns
		–1	0.52	4.14	0.03	1.61	2.44	0.34	4.12	3.11	3.14	2.91	5.37	4.35	ns
100 µA	8 mA	Std.	0.61	3.93	0.04	1.90	2.87	0.40	3.91	2.87	4.23	4.38	5.37	4.33	ns
		–1	0.52	3.34	0.03	1.61	2.44	0.34	3.33	2.44	3.60	3.72	4.57	3.68	ns
100 µA	12 mA	Std.	0.61	3.40	0.04	1.90	2.87	0.40	3.38	2.49	4.58	4.99	4.85	3.95	ns
		–1	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36	ns
100 µA	16 mA	Std.	0.61	3.31	0.04	1.90	2.87	0.40	3.29	2.42	4.66	5.16	4.76	3.89	ns
		–1	0.52	2.82	0.03	1.61	2.44	0.34	2.80	2.06	3.96	4.39	4.05	3.31	ns
100 µA	24 mA	Std.	0.61	3.35	0.04	1.90	2.87	0.40	3.33	2.32	4.76	5.78	4.80	3.79	ns
		–1	0.52	2.85	0.03	1.61	2.44	0.34	2.83	1.98	4.05	4.92	4.08	3.22	ns

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.5 V DC Core Voltage

Table 2-88 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	–1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	–1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	–1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	–1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	–1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	–1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	–1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.61	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	–1	0.52	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	034	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-114 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the database; Microsemi loadings for enable path characterization are described in Figure 2-14.

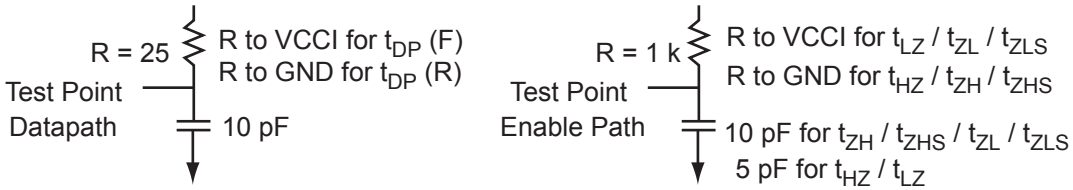

Figure 2-14 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-115.

Table 2-115 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$		10

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-132 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	169	124	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 125°C junction temperature.*

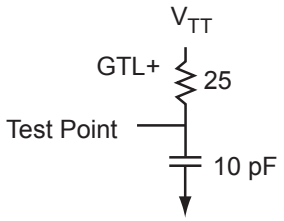

Figure 2-18 • AC Loading

Table 2-133 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-134 • 2.5 V GTL+
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.19	0.05	2.27	0.52	2.22	2.08	–	–	4.43	4.28	ns
–1	0.68	1.86	0.05	1.93	0.44	1.89	1.77	–	–	3.77	3.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-135 • 2.5 V GTL+
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.0 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.05	0.04	2.04	0.40	2.07	1.99	–	–	3.53	3.46	ns
–1	0.52	1.75	0.03	1.73	0.34	1.76	1.69	–	–	3.00	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-160 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0	–	2.925	V
IIH [2,3]	Input High Leakage Current	–	–	10	µA
IIL [2,4]	Input Low Leakage Current	–	–	10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350	–	mV

Notes:

1. *IOL/IOH is defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 125°C junction temperature.*
3. *IIH is the input leakage current per IO pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

Table 2-161 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-25 for a complete table of trip points.*

Table 2-177 • Output Data Register Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.71	0.83	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.38	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.53	0.62	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.97	1.14	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.97	1.14	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Timing Waveforms

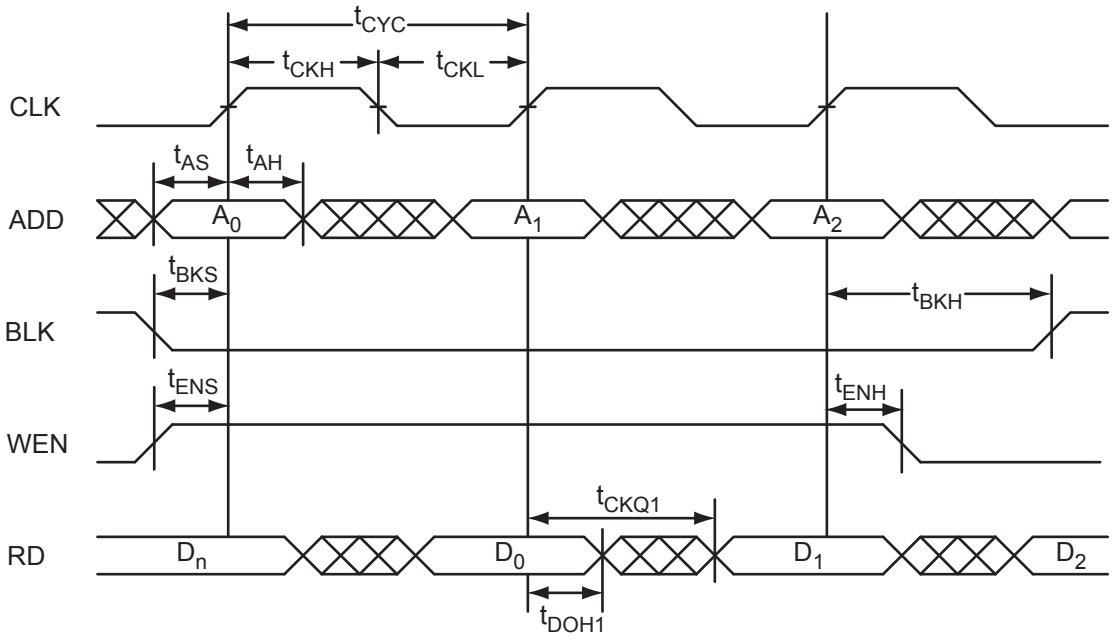

Figure 2-44 • **RAM Read for Pass-Through Output**

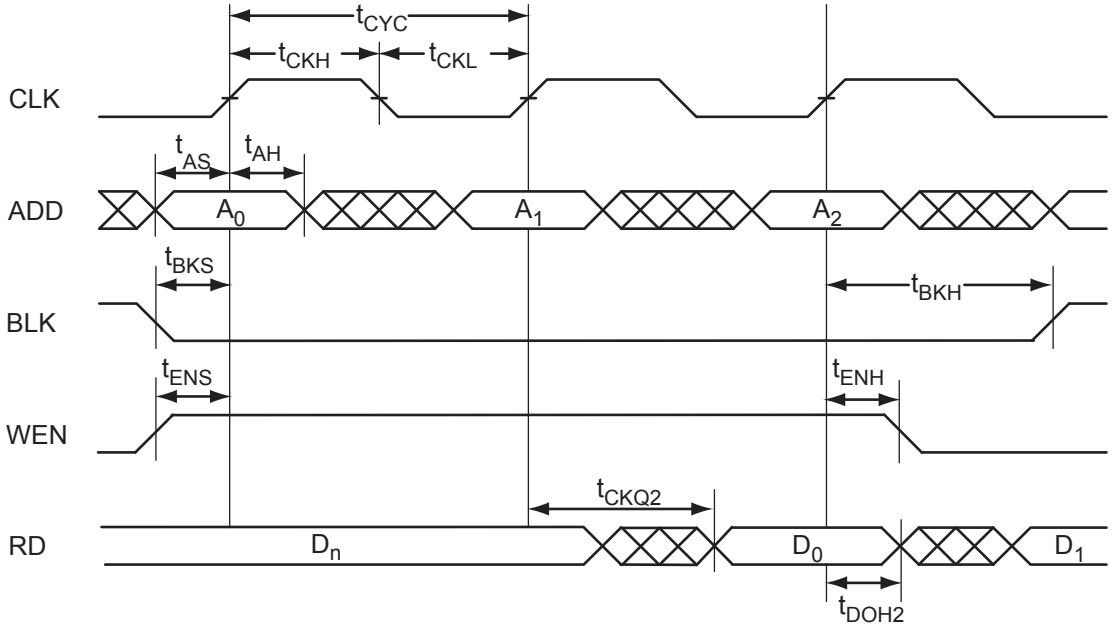

Figure 2-45 • **RAM Read for Pipelined Output**

Timing Characteristics

Table 2-203 • RAM4K9
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.35	0.41	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.20	0.23	ns
t_{ENH}	REN, WEN hold time	0.13	0.16	ns
t_{BKS}	BLK setup time	0.32	0.38	ns
t_{BKH}	BLK hold time	0.03	0.03	ns
t_{DS}	Input data (DIN) setup time	0.25	0.30	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	3.26	3.84	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.47	2.91	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.24	1.46	ns
t_{C2CWWL}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.25	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.27	0.32	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.37	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.28	1.50	ns
	RESET Low to data out Low on DOUT (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.66	0.76	ns
t_{CYC}	Clock cycle time	6.08	6.99	ns
F_{MAX}	Maximum frequency	164	143	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

PQ208	
Pin Number	A3P1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC

PQ208	
Pin Number	A3P1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG256	
Pin Number	A3P1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	A3P1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	A3P1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG484	
Pin Number	A3PE600L Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	VCCIB1
A21	GND
A22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0

FG484	
Pin Number	A3PE600L Function
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	VCC
C9	VCC
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB2
D1	NC
D2	NC
D3	NC
D4	GND

FG484	
Pin Number	A3PE600L Function
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO05PDB0V0
D9	IO10PDB0V1
D10	IO12PDB0V2
D11	IO16NDB0V2
D12	IO23NDB1V0
D13	IO23PDB1V0
D14	IO28NDB1V1
D15	IO28PDB1V1
D16	GBB1/IO34PDB1V1
D17	GBA0/IO35NDB1V1
D18	GBA1/IO35PDB1V1
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO133PDB7V1
E5	GAA2/IO134PDB7V1
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO05NDB0V0
E9	IO10NDB0V1
E10	IO12NDB0V2
E11	IO16PDB0V2
E12	IO20NDB1V0
E13	IO24NDB1V0
E14	IO24PDB1V0
E15	GBC1/IO33PDB1V1
E16	GBB0/IO34NDB1V1
E17	GNDQ

FG484	
Pin Number	A3P1000 Function
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC

FG484	
Pin Number	A3P1000 Function
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2

FG484	
Pin Number	A3P1000 Function
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3

Revision	Changes	Page
Revision 1 (continued)	The "Quiescent Supply Current " section was updated. Table 2-8 • Power Supply State Per Mode is new (SAR 24882, 24112, 32549). New values were added to the following tables (SAR 30619): Table 2-9 • Quiescent Supply Current (IDD) Characteristics, Flash*Freeze Mode* Table 2-11 • Quiescent Supply Current (IDD) Characteristics, Shutdown Mode* Table 2-12 • Quiescent Supply Current (IDD), Static Mode and Active Mode [1] (the name of this table changed from "No Flash*Freeze Mode" to "Static Mode and Active Mode" per SAR 32549) Table 2-13 • Quiescent Supply Current (IDD) Characteristics for A3P250 and A3P1000 The military maximum current for A3P1000 was revised in the following table (SAR 30620): Table 2-13 • Quiescent Supply Current (IDD) Characteristics for A3P250 and A3P1000	2-7
	All timing and power tables were updated to reflect changes in the software resulting from characterization and bug fixes (SAR 32394).	2-9 to 2-146
	In the following tables for A3P250 and A3P1000, the note regarding dynamic power was revised to, "Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default" (SAR 32449). Table 2-18 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Table 2-19 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings	2-12, 2-12
	Values for A3PE600L and A3P250 were added to Table 2-21 • Different Components Contributing to Dynamic Power Consumption in Military ProASIC3 and ProASIC3/EL Devices at 1.5 V VCC. Values in the table, and in Table 2-20 • Different Components Contributing to Dynamic Power Consumption in Military ProASIC3/EL Devices Operating at 1.2 V VCC, were updated were updated to reflect changes in the software resulting from characterization and bug fixes (SAR 30528).	2-13, 2-14
	Table 2-22 • Different Components Contributing to the Static Power Consumption in Military ProASIC3/EL Devices and the "Total Static Power Consumption—P_{STAT}" calculation were updated to add PDC0 (SAR 32549).	2-14, 2-15
	The "Timing Model" was updated (SAR 29793).	2-18
	The title of Table 2-29 • Summary of AC Measuring Points was changed from "Summary of AC Memory Points" (SAR 32446).	2-25
	The following note was added to Table 2-31, and Table 2-32, Summary of I/O Timing Characteristics (SAR 32449): "Output delays provided in this table were extracted with an output load indicated in the Capacitive Load column. For a specific output load, refer to Designer software."	2-26
	Resistances and short circuit currents were updated (SARs 29793, 31717): Table 2-36 • I/O Output Buffer Maximum Resistances [1] Applicable to Pro I/Os for A3PE600L and A3PE3000L Only Table 2-40 • I/O Short Currents IOSH/IOSL Applicable to Pro I/Os for A3PE600L and A3PE3000L Only (SAR 31717) Tables for Pro I/Os in the "Single-Ended I/O Characteristics" section (SAR 31717).	2-30 to 2-33

Revision	Changes	Page
Revision 1 (continued)	The "VQ100" pin table for A3P250 is new (SAR 31975).	4-2
	The "FG144" pin table for A3P1000 was updated to remove the Flash*Freeze (FF) designation from pin L3. This package does not support Flash*Freeze functionality. Pin W6 of the "FG484" for A3PE600L was designated as the Flash*Freeze control pin for that package (SAR 24084).	4-7, 4-14