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Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega168pb-aur

15.11.1. Sleep Mode Control Register

The Sleep Mode Control Register contains control bits for power management.

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: SMCR
Offset: 0x53
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x33

Bit	7	6	5	4	3	2	1	0
					SM2	SM1	SM0	SE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SM2: Sleep Mode Select 2
The SM[2:0] bits select between the five available sleep modes.

Table 15-2. Sleep Mode Select

SM2,SM1,SM0	Sleep Mode
000	Idle
001	ADC Noise Reduction
010	Power-down
011	Power-save
100	Reserved
101	Reserved
110	Standby(1)
111	Extended Standby(1)

Note:
1. Standby mode is only recommended for use with external crystals or resonators.

Bit 2 – SM1: Sleep Mode Select 1
Refer to SM2.

Bit 1 – SM0: Sleep Mode Select 0
Refer to SM2.

Bit 0 – SE: Sleep Enable
The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmer's purpose, it is recommended to write the Sleep Enable (SE) bit to one just before the execution of the SLEEP instruction and to clear it immediately after waking up.

Vector No.	Program Address	Source	Interrupt Definition
20	0x013	USART, UDRE	USART, Data Register Empty
21	0x014	USART, TX	USART, Tx Complete
22	0x015	ADC	ADC Conversion Complete
23	0x016	EE READY	EEPROM Ready
24	0x017	ANALOG COMP	Analog Comparator
25	0x018	TWI	2-wire Serial Interface (I²C)
26	0x019	SPM READY	Store Program Memory Ready
27	0x01A	USART, START	USART Start Edge Interrupt

The most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega48PB is:

Address	Labels		Code Comments
0x000	rjmp	RESET	; Reset Handler
0x001	rjmp	EXT_INT0	; IRQ0 Handler
0x002	rjmp	EXT_INT1	; IRQ1 Handler
0x003	rjmp	PCINT0	; PCINT0 Handler
0x004	rjmp	PCINT1	; PCINT1 Handler
0x005	rjmp	PCINT2	; PCINT2 Handler
0x006	rjmp	WDT	; Watchdog Timer Handler
0x007	rjmp	TIM2_COMPA	; Timer2 Compare A Handler
0x008	rjmp	TIM2_COMPB	; Timer2 Compare B Handler
0x009	rjmp	TIM2_OVF	; Timer2 Overflow Handler
0x00A	rjmp	TIM1_CAPT	; Timer1 Capture Handler
0x00B	rjmp	TIM1_COMPA	; Timer1 Compare A Handler
0x00C	rjmp	TIM1_COMPB	; Timer1 Compare B Handler
0x00D	rjmp	TIM1_OVF	; Timer1 Overflow Handler
0x00E	rjmp	TIM0_COMPA	; Timer0 Compare A Handler
0x00F	rjmp	TIM0_COMPB	; Timer0 Compare B Handler
0x010	rjmp	TIM0_OVF	; Timer0 Overflow Handler
0x011	rjmp	SPI_STC	; SPI Transfer Complete Handler
0x012	rjmp	USART_RXC	; USART, RX Complete Handler
0x013	rjmp	USART_UDRE	; USART, UDR Empty Handler
0x014	rjmp	USART_TXC	; USART, TX Complete Handler

Address	Labels		Code Comments
0x000	rjmp	RESET	; Reset Handler
0x001	rjmp	EXT_INT0	; IRQ0 Handler
0x002	rjmp	EXT_INT1	; IRQ1 Handler
0x003	rjmp	PCINT0	; PCINT0 Handler
0x004	rjmp	PCINT1	; PCINT1 Handler
0x005	rjmp	PCINT2	; PCINT2 Handler
0x006	rjmp	WDT	; Watchdog Timer Handler
0x007	rjmp	TIM2_COMPA	; Timer2 Compare A Handler
0X008	rjmp	TIM2_COMPB	; Timer2 Compare B Handler
0x009	rjmp	TIM2_OVF	; Timer2 Overflow Handler
0x00A	rjmp	TIM1_CAPT	; Timer1 Capture Handler
0x00B	rjmp	TIM1_COMPA	; Timer1 Compare A Handler
0x00C	rjmp	TIM1_COMPB	; Timer1 Compare B Handler
0x00D	rjmp	TIM1_OVF	; Timer1 Overflow Handler
0x00E	rjmp	TIM0_COMPA	; Timer0 Compare A Handler
0x00F	rjmp	TIM0_COMPB	; Timer0 Compare B Handler
0x010	rjmp	TIM0_OVF	; Timer0 Overflow Handler
0x011	rjmp	SPI_STC	; SPI Transfer Complete Handler
0x012	rjmp	USART_RXC	; USART, RX Complete Handler
0x013	rjmp	USART_UDRE	; USART, UDR Empty Handler
0x014	rjmp	USART_TXC	; USART, TX Complete Handler
0x015	rjmp	ADC	; ADC Conversion Complete Handler

- PCINT4: Pin Change Interrupt source 4. The PB4 pin can serve as an external interrupt source.

- MOSI0/TXD1/OC2A/PCINT3 – Port B, Bit 3
  - MOSI0: SPI0 Master Data output, Slave Data input for SPI0 channel. When the SPI0 is enabled as a Slave, this pin is configured as an input regardless of the setting of DDB3. When the SPI0 is enabled as a Master, the data direction of this pin is controlled by DDB3. When the pin is forced by the SPI0 to be an input, the pull-up can still be controlled by the PORTB3 bit.
  - TXD1: Transmit Data (Data output pin for the USART1). When the USART1 Transmitter is enabled, this pin is configured as an output regardless of the value of DDB3.
  - OC2A: Output Compare Match output. The PB3 pin can serve as an external output for the Timer/Counter2 Compare Match A. The PB3 pin has to be configured as an output (DDB3 set '1') to serve this function. The OC2A pin is also the output pin for the PWM mode timer function.
  - PCINT3: Pin Change Interrupt source 3. The PB3 pin can serve as an external interrupt source.

- SS0/OC1B/PCINT2 – Port B, Bit 2
  - SS0: Slave0 Select input. When the SPI0 is enabled as a Slave, this pin is configured as an input regardless of the setting of DDB2. As a Slave, the SPI0 is activated when this pin is driven low. When the SPI0 is enabled as a Master, the data direction of this pin is controlled by DDB2. When the pin is forced by the SPI0 to be an input, the pull-up can still be controlled by the PORTB2 bit.
  - OC1B: Output Compare Match output. The PB2 pin can serve as an external output for the Timer/Counter1 Compare Match B. The PB2 pin has to be configured as an output (DDB2 set (one)) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.
  - PCINT2: Pin Change Interrupt source 2. The PB2 pin can serve as an external interrupt source.

- OC1A/PCINT1 – Port B, Bit 1
  - OC1A: Output Compare Match output. The PB1 pin can serve as an external output for the Timer/Counter1 Compare Match A. The PB1 pin has to be configured as an output (DDB1 set (one)) to serve this function. The OC1A pin is also the output pin for the PWM mode timer function.
  - PCINT1: Pin Change Interrupt source 1. The PB1 pin can serve as an external interrupt source.

- ICP1/CLKO/PCINT0 – Port B, Bit 0
  - ICP1: Input Capture Pin. The PB0 pin can act as an Input Capture Pin for Timer/Counter1.
  - CLKO: Divided System Clock. The divided system clock can be output on the PB0 pin. The divided system clock will be output if the CKOUT Fuse is programmed, regardless of the PORTB0 and DDB0 settings. It will also be output during reset.
  - PCINT0: Pin Change Interrupt source 0. The PB0 pin can serve as an external interrupt source.

Table 19-3 Port B Pins Alternate Functions and Table 19-5 Overriding Signals for Alternate Functions in PB3...PB0 relate the alternate functions of Port B to the overriding signals shown in Figure 19-5 Alternate Port Functions(1). SPI MSTR INPUT and SPI SLAVE OUTPUT constitute the MISO signal, while MOSI is divided into SPI MSTR OUTPUT and SPI SLAVE INPUT.

19.4. Register Description

Table 20-10. Clock Select Bit Description

CA02	CA01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/1 (No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	clkI/O/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

If external pin modes are used for the Timer/Counter0, transitions on the T0 pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

Assembly Code Example(1)

```
TIM16_ReadTCNT1:
   ; Save global interrupt flag
   in    r18,SREG
   ; Disable interrupts
   cli
   ; Read TCNT1 into r17:r16
   in    r16,TCNT1L
   in    r17,TCNT1H
   ; Restore global interrupt flag
   out   SREG,r18
   ret
```

The assembly code example returns the TCNT1 value in the r17:r16 register pair.

C Code Example(1)

```
unsigned int TIM16_ReadTCNT1( void )
{
   unsigned char sreg;
   unsigned int i;
   /* Save global interrupt flag */
   sreg = SREG;
   /* Disable interrupts */
   _CLI();
   /* Read TCNT1 into i */
   i = TCNT1;
   /* Restore global interrupt flag */
   SREG = sreg;
   return i;
}
```

Note:

1. The example code assumes that the part specific header file is included. For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

Atomic Write

The following code examples show how to do an atomic write of the TCNT1 Register contents. Writing any of the OCR1A/B or ICR1 Registers can be done by using the same principle.

Assembly Code Example(1)

```
TIM16_WriteTCNT1:
   ; Save global interrupt flag
   in     r18,SREG
   ; Disable interrupts
   cli
   ; Set TCNT1 to r17:r16
   out    TCNT1H,r17
   out    TCNT1L,r16
   ; Restore global interrupt flag
   out    SREG,r18
   ret
```

The assembly code example requires that the r17:r16 register pair contains the value to be written to TCNT1.

C Code Example(1)

```
void TIM16_WriteTCNT1( unsigned int i )
{
   unsigned char sreg;
   unsigned int i;
```

23.11.4. TC2 Output Compare Register A

Name: OCR2A
Offset: 0xB3
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	OCR2A[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR2A[7:0]: Output Compare 2 A
The Output Compare Register A contains an 8-bit value that is continuously compared with the counter value (TCNT2). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC2A pin.

23.11.6. TC2 Interrupt Mask Register

Name: TIMSK2
Offset: 0x70
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						OCIE2B	OCIE2A	TOIE2
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – OCIE2B: Timer/Counter2, Output Compare B Match Interrupt Enable
When the OCIE2B bit is written to '1' and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match B interrupt is enabled. The corresponding interrupt is executed if a compare match in Timer/Counter2 occurs, i.e., when the OCF2B bit is set in TIFR2.

Bit 1 – OCIE2A: Timer/Counter2, Output Compare A Match Interrupt Enable
When the OCIE2A bit is written to '1' and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match A interrupt is enabled. The corresponding interrupt is executed if a compare match in Timer/Counter2 occurs, i.e., when the OCF2A bit is set in TIFR2.

Bit 0 – TOIE2: Timer/Counter2, Overflow Interrupt Enable
When the TOIE2 bit is written to '1' and the I-bit in the Status Register is set (one), the Timer/Counter2 Overflow interrupt is enabled. The corresponding interrupt is executed if an overflow in Timer/Counter2 occurs, i.e., when the TOV2 bit is set in TIFR2.

More advanced initialization routines can be written to include frame format as parameters, disable interrupts, and so on. However, many applications use a fixed setting of the baud and control registers, and for these types of applications the initialization code can be placed directly in the main routine, or be combined with initialization code for other I/O modules.

Related Links

About Code Examples on page 22

25.7. Data Transmission – The USART Transmitter

The USART Transmitter is enabled by setting the Transmit Enable (TXEN) bit in the UCSRnB Register. When the Transmitter is enabled, the normal port operation of the TxDn pin is overridden by the USART and given the function as the Transmitter's serial output. The baud rate, mode of operation and frame format must be set up once before doing any transmissions. If synchronous operation is used, the clock on the XCKn pin will be overridden and used as transmission clock.

25.7.1. Sending Frames with 5 to 8 Data Bits

A data transmission is initiated by loading the transmit buffer with the data to be transmitted. The CPU can load the transmit buffer by writing to the UDRn I/O location. The buffered data in the transmit buffer will be moved to the Shift Register when the Shift Register is ready to send a new frame. The Shift Register is loaded with new data if it is in idle state (no ongoing transmission) or immediately after the last stop bit of the previous frame is transmitted. When the Shift Register is loaded with new data, it will transfer one complete frame at the rate given by the Baud Register, U2Xn bit or by XCKn depending on mode of operation.

The following code examples show a simple USART transmit function based on polling of the Data Register Empty (UDRE) Flag. When using frames with less than eight bits, the most significant bits written to the UDR0 are ignored. The USART 0 has to be initialized before the function can be used. For the assembly code, the data to be sent is assumed to be stored in Register R17.

Assembly Code Example

```
USART_Transmit:
   ; Wait for empty transmit buffer
   in      r17, UCSR0A
   sbrs    r17, UDRE
   rjmp    USART_Transmit
   ; Put data (r16) into buffer, sends the data
   out    UDR0,r16
   ret
```

C Code Example

```
void USART_Transmit( unsigned char data )
{
   /* Wait for empty transmit buffer */
   while ( !( UCSR0A & (1<<UDRE)) )
      ;
   /* Put data into buffer, sends the data */
   UDR0 = data;
}
```

The function simply waits for the transmit buffer to be empty by checking the UDRE Flag, before loading it with new data to be transmitted. If the Data Register Empty interrupt is utilized, the interrupt routine writes the data into the buffer.

The Data OverRun (DOR) Flag indicates data loss due to a receiver buffer full condition. A Data OverRun occurs when the receive buffer is full (two characters), a new character is waiting in the Receive Shift Register, and a new start bit is detected. If the DOR Flag is set, one or more serial frames were lost between the last frame read from UDR, and the next frame read from UDR. For compatibility with future devices, always write this bit to zero when writing to UCSRnA. The DOR Flag is cleared when the frame received was successfully moved from the Shift Register to the receive buffer.

The Parity Error (UPE) Flag indicates that the next frame in the receive buffer had a Parity Error when received. If Parity Check is not enabled the UPE bit will always read '0'. For compatibility with future devices, always set this bit to zero when writing to UCSRnA. For more details see Parity Bit Calculation and 'Parity Checker' below.

25.8.5. Parity Checker

The Parity Checker is active when the high USART Parity Mode bit 1 in the USART Control and Status Register n C (UCSRnC.UPM[1]) is written to '1'. The type of Parity Check to be performed (odd or even) is selected by the UCSRnC.UPM[0] bit. When enabled, the Parity Checker calculates the parity of the data bits in incoming frames and compares the result with the parity bit from the serial frame. The result of the check is stored in the receive buffer together with the received data and stop bits. The USART Parity Error Flag in the USART Control and Status Register n A (UCSRnA.UPE) can then be read by software to check if the frame had a Parity Error.

The UPEn bit is set if the next character that can be read from the receive buffer had a Parity Error when received and the Parity Checking was enabled at that point (UPM[1] = 1). This bit is valid until the receive buffer (UDRn) is read.

25.8.6. Disabling the Receiver

In contrast to the Transmitter, disabling of the Receiver will be immediate. Data from ongoing receptions will therefore be lost. When disabled (i.e., UCSRnB.RXEN is written to zero) the Receiver will no longer override the normal function of the RxDn port pin. The Receiver buffer FIFO will be flushed when the Receiver is disabled. Remaining data in the buffer will be lost.

25.8.7. Flushing the Receive Buffer

The receiver buffer FIFO will be flushed when the Receiver is disabled, i.e., the buffer will be emptied of its contents. Unread data will be lost. If the buffer has to be flushed during normal operation, due to for instance an error condition, read the UDRn I/O location until the RXCn Flag is cleared.

The following code shows how to flush the receive buffer of USART0.

Assembly Code Example

```
USART_Flush:
   in      r16, UCSR0A
   sbrs    r16, RXC
   ret
   in      r16, UDR0
   rjmp    USART_Flush
```

C Code Example

```
void USART_Flush( void )
{
   unsigned char dummy;
   while ( UCSR0A & (1<<RXC) ) dummy = UDR0;
}
```

Related Links

About Code Examples on page 22

Baud Rate [bps]	f_{osc} = 3.6864MHz				f_{osc} = 4.0000MHz				f_{osc} = 7.3728MHz			
	U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1	
	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error
250k	0	-7.8%	1	-7.8%	0	0.0%	1	0.0%	1	-7.8%	3	-7.8%
0.5M	–	–	0	-7.8%	–	–	0	0.0%	0	-7.8%	1	-7.8%
1M	–	–	–	–	–	–	–	–	–	–	0	-7.8%
Max.(1)	230.4kbps		460.8kbps		250kbps		0.5Mbps		460.8kbps		921.6kbps	

(1) UBRRn = 0, Error = 0.0%

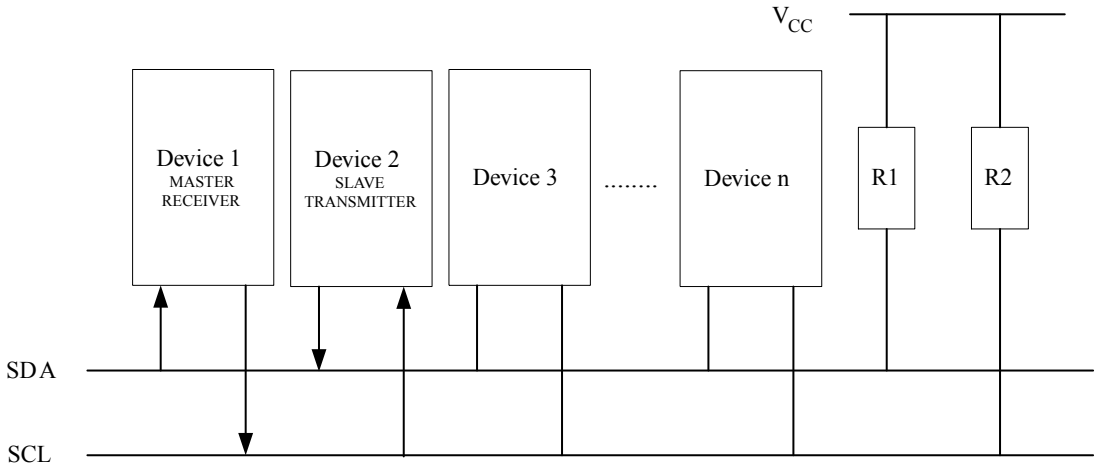
Table 25-8. Examples of UBRRn Settings for Commonly Used Oscillator Frequencies

Baud Rate [bps]	f_{osc} = 8.0000MHz				f_{osc} = 11.0592MHz				f_{osc} = 14.7456MHz			
	U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1	
	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error
2400	207	0.2%	416	-0.1%	287	0.0%	575	0.0%	383	0.0%	767	0.0%
4800	103	0.2%	207	0.2%	143	0.0%	287	0.0%	191	0.0%	383	0.0%
9600	51	0.2%	103	0.2%	71	0.0%	143	0.0%	95	0.0%	191	0.0%
14.4k	34	-0.8%	68	0.6%	47	0.0%	95	0.0%	63	0.0%	127	0.0%
19.2k	25	0.2%	51	0.2%	35	0.0%	71	0.0%	47	0.0%	95	0.0%
28.8k	16	2.1%	34	-0.8%	23	0.0%	47	0.0%	31	0.0%	63	0.0%
38.4k	12	0.2%	25	0.2%	17	0.0%	35	0.0%	23	0.0%	47	0.0%
57.6k	8	-3.5%	16	2.1%	11	0.0%	23	0.0%	15	0.0%	31	0.0%
76.8k	6	-7.0%	12	0.2%	8	0.0%	17	0.0%	11	0.0%	23	0.0%
115.2k	3	8.5%	8	-3.5%	5	0.0%	11	0.0%	7	0.0%	15	0.0%
230.4k	1	8.5%	3	8.5%	2	0.0%	5	0.0%	3	0.0%	7	0.0%
250k	1	0.0%	3	0.0%	2	-7.8%	5	-7.8%	3	-7.8%	6	5.3%
0.5M	0	0.0%	1	0.0%	–	–	2	-7.8%	1	-7.8%	3	-7.8%
1M	–	–	0	0.0%	–	–	–	–	0	-7.8%	1	-7.8%
Max.(1)	0.5Mbps		1Mbps		691.2kbps		1.3824Mbps		921.6kbps		1.8432Mbps	

(1) UBRRn = 0, Error = 0.0%

Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response					Next Action Taken by TWI Hardware
		To/from TWDR	To TWCRn				
			STA	STO	TWINT	TWEA	
0x30	Data byte has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x38	Arbitration lost in SLA +W or data bytes	No TWDR action or	0	0	1	X	2-wire Serial Bus will be released and not addressed Slave mode entered
		No TWDR action	1	0	1	X	A START condition will be transmitted when the bus becomes free

Figure 27-13. Data Transfer in Master Receiver Mode



A START condition is sent by writing to the TWI Control register (TWCRn) a value of the type TWCRn=1x10x10x:

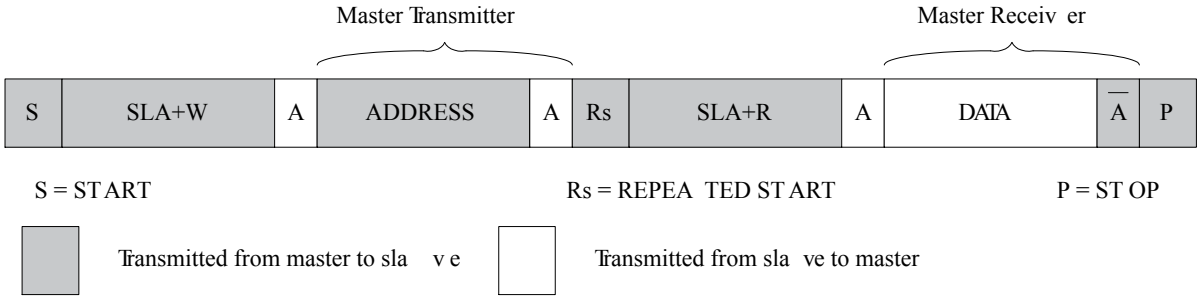
- TWCRn.TWEN must be written to '1' to enable the 2-wire Serial Interface
- TWCRn.TWSTA must be written to '1' to transmit a START condition
- TWCRn.TWINT must be cleared by writing a '1' to it.

The TWI will then test the 2-wire Serial Bus and generate a START condition as soon as the bus becomes free. After a START condition has been transmitted, the TWINT Flag is set by hardware, and the status code in TWSRn will be 0x08 (see Status Code table below). In order to enter MR mode, SLA +R must be transmitted. This is done by writing SLA+R to TWDR. Thereafter, the TWINT flag should be cleared (by writing '1' to it) to continue the transfer. This is accomplished by writing the a value to TWCRn of the type TWCRn=1x00x10x.

When SLA+R have been transmitted and an acknowledgment bit has been received, TWINT is set again and a number of status codes in TWSRn are possible. Possible status codes in Master mode are 0x38, 0x40, or 0x48. The appropriate action to be taken for each of these status codes is detailed in the table below. Received data can be read from the TWDR Register when the TWINT Flag is set high by hardware. This scheme is repeated until the last byte has been received. After the last byte has been received, the MR should inform the ST by sending a NACK after the last received data byte. The transfer is ended by generating a STOP condition or a repeated START condition. A repeated START condition is sent by writing to the TWI Control register (TWCRn) a value of the type TWCRn=1x10x10x again. A STOP condition is generated by writing TWCRn=1xx01x10x:

After a repeated START condition (status code 0x10) the 2-wire Serial Interface can access the same Slave again, or a new Slave without transmitting a STOP condition. Repeated START enables the Master to switch between Slaves, Master Transmitter mode and Master Receiver mode without losing control over the bus.

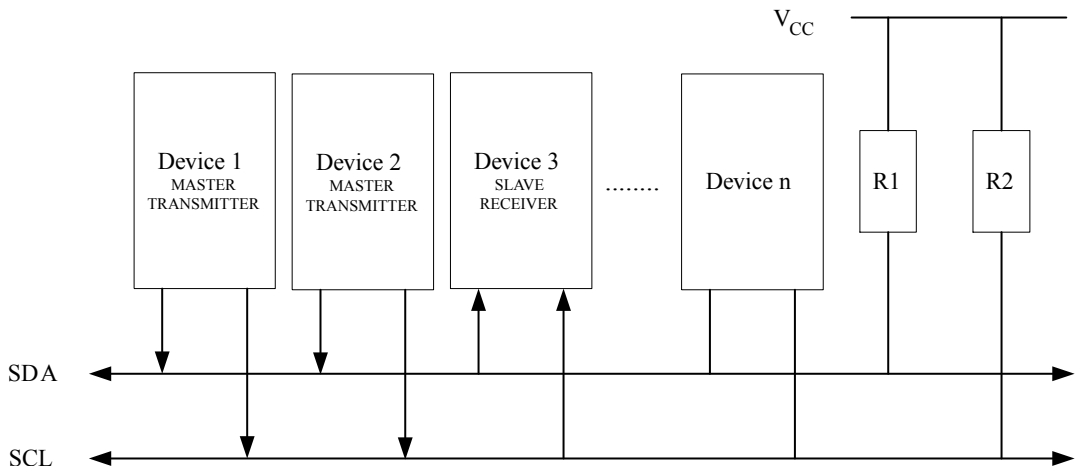
Figure 27-19. Combining Several TWI Modes to Access a Serial EEPROM



27.8. Multi-master Systems and Arbitration

If multiple masters are connected to the same bus, transmissions may be initiated simultaneously by one or more of them. The TWI standard ensures that such situations are handled in such a way that one of the masters will be allowed to proceed with the transfer, and that no data will be lost in the process. An example of an arbitration situation is depicted below, where two masters are trying to transmit data to a Slave Receiver.

Figure 27-20. An Arbitration Example

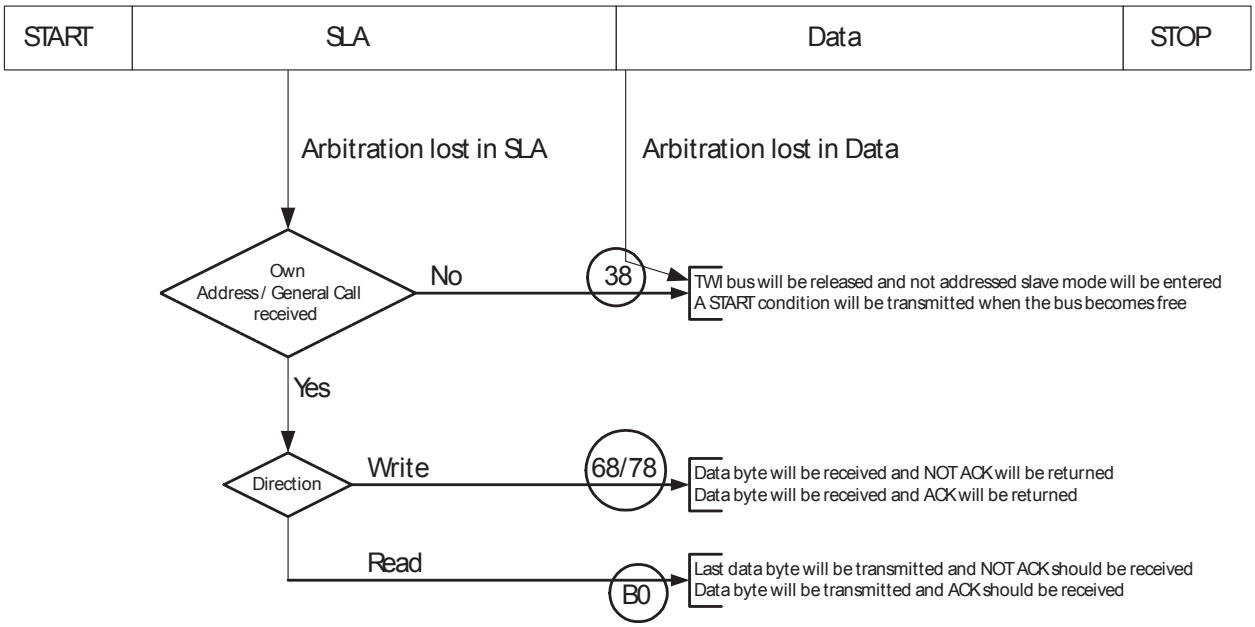


Several different scenarios may arise during arbitration, as described below:

- Two or more masters are performing identical communication with the same Slave. In this case, neither the Slave nor any of the masters will know about the bus contention.
- Two or more masters are accessing the same Slave with different data or direction bit. In this case, arbitration will occur, either in the READ/WRITE bit or in the data bits. The masters trying to output a '1' on SDA while another Master outputs a zero will lose the arbitration. Losing masters will switch to not addressed Slave mode or wait until the bus is free and transmit a new START condition, depending on application software action.
- Two or more masters are accessing different slaves. In this case, arbitration will occur in the SLA bits. Masters trying to output a '1' on SDA while another Master outputs a zero will lose the arbitration. Masters losing arbitration in SLA will switch to Slave mode to check if they are being addressed by the winning Master. If addressed, they will switch to SR or ST mode, depending on the value of the READ/WRITE bit. If they are not being addressed, they will switch to not addressed Slave mode or wait until the bus is free and transmit a new START condition, depending on application software action.

This is summarized in the next figure. Possible status values are given in circles.

Figure 27-21. Possible Status Codes Caused by Arbitration



27.9. Register Description

29.9.3. ADC Data Register Low (ADLAR=0)

When an ADC conversion is complete, the result is found in these two registers.

When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, if the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH.

The ADLAR bit and the MUXn bits in ADMUX affect the way the result is read from the registers. If ADLAR is set, the result is left adjusted. If ADLAR is cleared (default), the result is right adjusted.

Name: ADCL
Offset: 0x78
Reset: 0x00
Property: ADLAR = 0

Bit	7	6	5	4	3	2	1	0
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ADCn: ADC Conversion Result [n = 7:0]
These bits represent the result from the conversion. Refer to ADC Conversion Result for details.

Figure. The debugWIRE Setup shows the schematic of a target MCU, with debugWIRE enabled, and the emulator connector. The system clock is not affected by debugWIRE and will always be the clock source selected by the CKSEL Fuses.

When designing a system where debugWIRE will be used, the following observations must be made for correct operation:

- Pull-up resistors on the dW/(RESET) line must not be smaller than 10kΩ. The pull-up resistor is not required for debugWIRE functionality
- Connecting the RESET pin directly to V_{CC} will not work.
- Capacitors connected to the RESET pin must be disconnected when using debugWire.
- All external reset sources must be disconnected.

30.4. Software Break Points

debugWIRE supports Break Points function in Program Memory by the AVR Break instruction. Setting a break point in Atmel Studio will insert a BREAK instruction in the Program Memory. The Instruction replaced by the BREAK instruction will be stored. When program execution is continued, the stored instruction will be executed before continuing from the Program Memory. A break can be inserted manually by putting the BREAK instruction in the program.

The Flash must be re-programmed each time when a Break Point is changed. This is automatically handled by Atmel Studio through the debugWIRE interface. The use of Break Points will therefore reduce the Flash Data retention. Devices used for debugging purposes should not be shipped to end customers.

30.5. Limitations of debugWIRE

The debugWIRE communication pin (dW) is physically located on the same pin as External Reset (RESET). An External Reset source is therefore not supported when the debugWIRE is enabled.

A programmed DWEN Fuse enables some parts of the clock system to be running in all sleep modes. This will increase the power consumption while in sleep. Thus, the DWEN Fuse should be disabled when debugWire is not used.

30.6. Register Description

The following section describes the registers used with the debugWire.

31. Self-Programming the Flash

31.1. Overview

In ATmega48PB, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can be executed from the entire Flash.

The device provides a Self-Programming mechanism for downloading and uploading program code by the MCU itself. The Self-Programming can use any available data interface and associated protocol to read code and write (program) that code into the Program Memory.

The Program Memory is updated in a page by page fashion. Before programming a page with the data stored in the temporary page buffer, the page must be erased. The temporary page buffer is filled with one word at a time using SPM, and the buffer can be filled either before the Page Erase command or between a Page Erase and a Page Write operation:

Alternative 1, fill the buffer before a Page Erase

- Fill temporary page buffer
- Perform a Page Erase
- Perform a Page Write

Alternative 2, fill the buffer after Page Erase

- Perform a Page Erase
- Fill temporary page buffer
- Perform a Page Write

If only a part of the page needs to be changed, the rest of the page must be stored (for example in the temporary page buffer) before the erase, and then be re-written. When using alternative 1, the Boot Loader provides an effective Read-Modify-Write feature which allows the user software to first read the page, do the necessary changes, and then write back the modified data. If alternative 2 is used, it is not possible to read the old data while loading since the page is already erased. The temporary page buffer can be accessed in a random sequence. It is essential that the page address used in both the Page Erase and Page Write operation is addressing the same page.

31.1.1. Performing Page Erase by Store Program Memory (SPM)

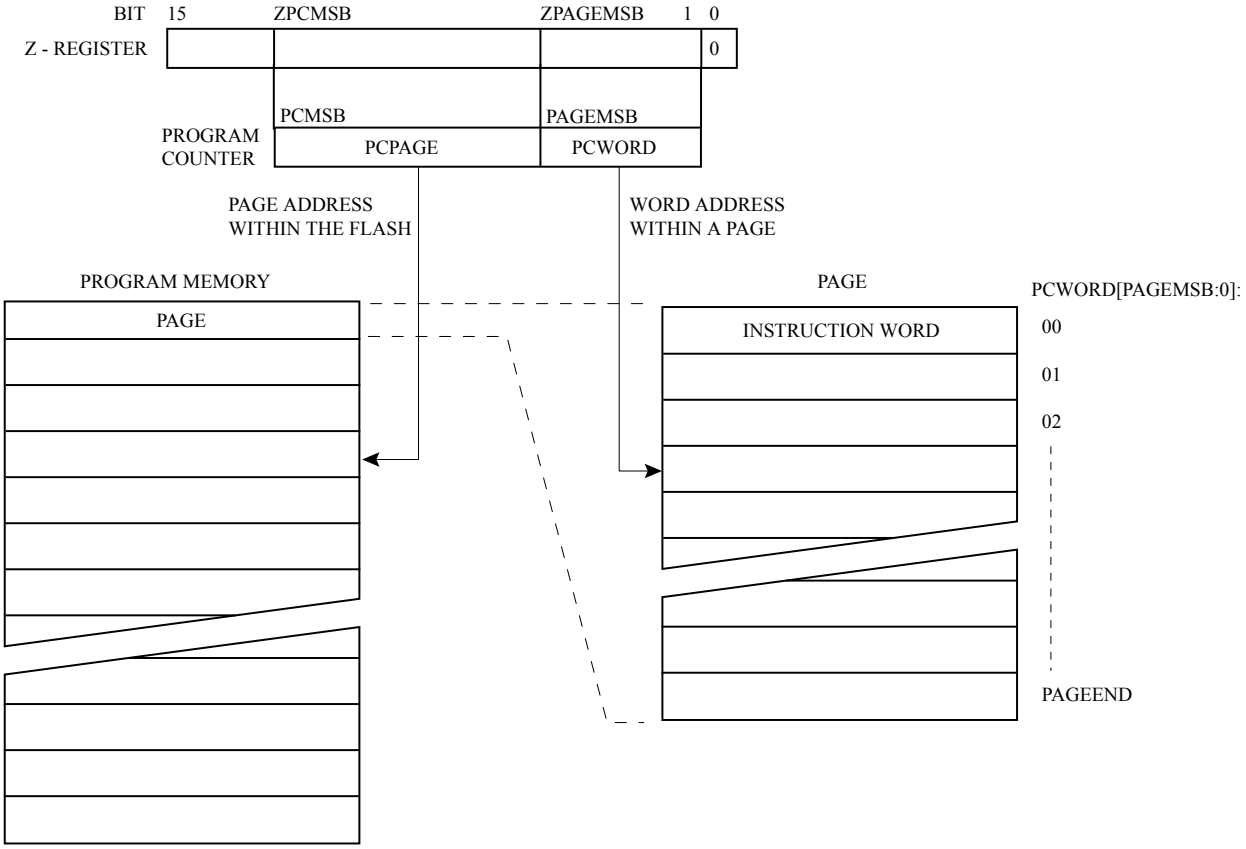
To execute Page Erase, set up the address in the Z-pointer (R30 and R31), write “0x00000011” to Store Program Memory Control and Status Register (SPMCSR) and execute Store Program Memory (SPM) within four clock cycles after writing SPMCSR. The data in R1 and R0 is ignored. The page address must be written to PCPAGE ([Z12:Z6]) in the Z-register. Other bits in the Z-pointer will be ignored during this operation.

- The CPU is halted during the Page Erase operation
  Note: If an interrupt occurs in the time sequence the four cycle access cannot be guaranteed. In order to ensure atomic operation you should disable interrupts before writing to SPMCSR.

31.1.2. Filling the Temporary Buffer (Page Loading)

To write an instruction word, set up the address in the Z-pointer (R30 and R31) and data in R1:R0, write “0x00000001” to SPMCSR and execute SPM within four clock cycles after writing SPMCSR. The content of PCWORD ([Z5:Z1]) in the Z-register is used to address the data in the temporary buffer. The temporary buffer will auto-erase after a Page Write operation or by writing the RWWSRE bit in SPMCSR. It is also

Figure 32-3. Addressing the Flash During SPM



Note: The different variables used in this figure are listed in the Related Links.

Related Links

Page Size on page 378

ATmega88PB Boot Loader Parameters on page 369

32.8. Self-Programming the Flash

The program memory is updated in a page by page fashion. Before programming a page with the data stored in the temporary page buffer, the page must be erased. The temporary page buffer is filled one word at a time using SPM and the buffer can be filled either before the Page Erase command or between a Page Erase and a Page Write operation:

Alternative 1, fill the buffer before a Page Erase

- Fill temporary page buffer
- Perform a Page Erase
- Perform a Page Write

Alternative 2, fill the buffer after Page Erase

- Perform a Page Erase
- Fill temporary page buffer
- Perform a Page Write