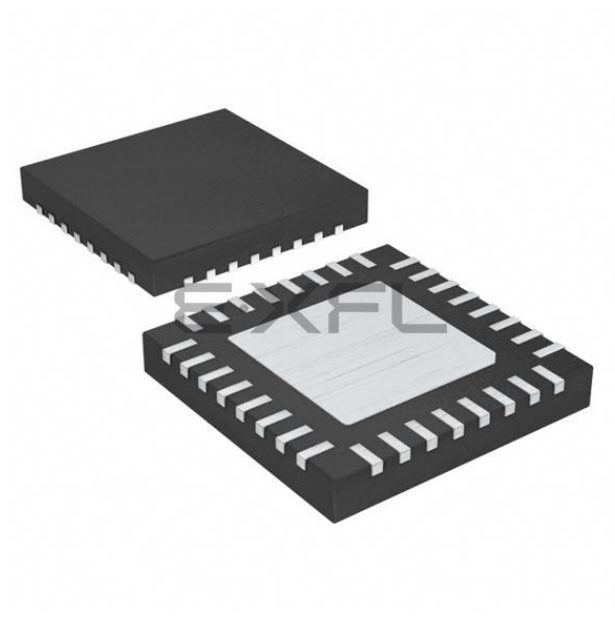

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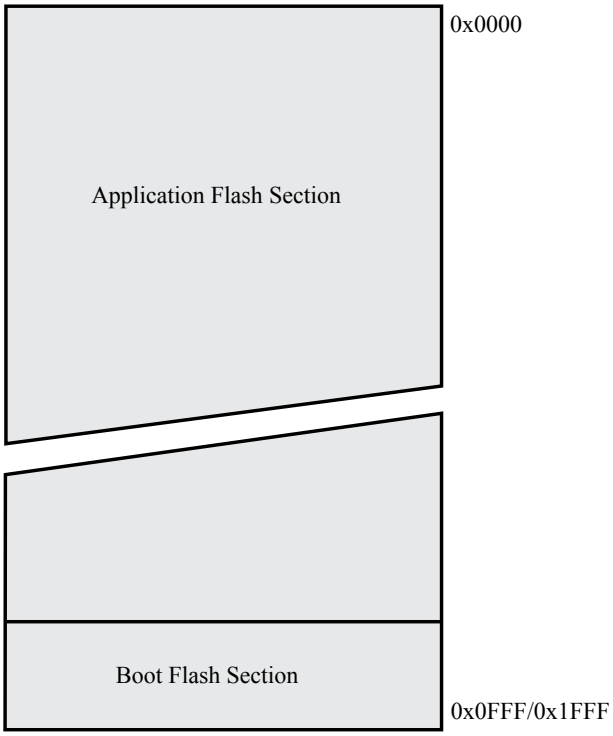
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	27
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega88pb-mnr

Figure 13-2. Program Memory Map ATmega88PB and ATmega168PB



Related Links

Memory Programming on page 374

Instruction Execution Timing on page 30

Boot Loader Support – Read-While-Write Self-Programming on page 356

Self-Programming the Flash on page 362

13.3. SRAM Data Memory

The following figure shows how the device SRAM Memory is organized.

The device is a complex microcontroller with more peripheral units than can be supported within the 64 locations reserved in the Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

The lower 768/1280/1280 data memory locations address both the Register File, the I/O memory, Extended I/O memory, and the internal data SRAM. The first 32 locations address the Register File, the next 64 location the standard I/O memory, then 160 locations of Extended I/O memory, and the next 512/1024/1024 locations address the internal data SRAM.

The five different addressing modes for the data memory cover:

1. Direct
   - The direct addressing reaches the entire data space.
2. Indirect with Displacement
   - The Indirect with Displacement mode reaches 63 address locations from the base address given by the Y- or Z-register.
3. Indirect

13.4. EEPROM Data Memory

The device contains 256/512/512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and the EEPROM Control Register.

See the related links for a detailed description on EEPROM Programming in SPI or Parallel Programming mode.

Related Links

Memory Programming on page 374

13.4.1. EEPROM Read/Write Access

The EEPROM Access Registers are accessible in the I/O space.

The write access time for the EEPROM is given in Table 13-2 EEPROM Programming Time. A self-timing function, however, lets the user software detect when the next byte can be written. If the user code contains instructions that write the EEPROM, some precautions must be taken. In heavily filtered power supplies, V_{CC} is likely to rise or fall slowly on power-up/down. This causes the device for some period of time to run at a voltage lower than specified as minimum for the clock frequency used. Please refer to Preventing EEPROM Corruption for details on how to avoid problems in these situations.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed. When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed.

Related Links

Memory Programming on page 374

13.4.2. Preventing EEPROM Corruption

During periods of low $V_{CC,}$ the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using EEPROM, and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Secondly, the CPU itself can execute instructions incorrectly, if the supply voltage is too low.

EEPROM data corruption can easily be avoided by following this design recommendation:

Keep the AVR $\overline{\text{RESET}}$ active (low) during periods of insufficient power supply voltage. This can be done by enabling the internal Brown-out Detector (BOD). If the detection level of the internal BOD does not match the needed detection level, an external low V_{CC} reset Protection circuit can be used. If a reset occurs while a write operation is in progress, the write operation will be completed provided that the power supply voltage is sufficient.

Related Links

Memory Programming on page 374

13.5. I/O Memory

The I/O space definition of the device is shown in the *Register Summary*.

All device I/Os and peripherals are placed in the I/O space. All I/O locations may be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range 0x00-0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

When using the I/O specific commands IN and OUT, the I/O addresses 0x00-0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The device is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60..0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a '1' to them; this is described in the flag descriptions. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00-0x1F only.

The I/O and Peripherals Control Registers are explained in later sections.

Related Links

Register Summary on page 446
Instruction Set Summary on page 449
Memory Programming on page 374

13.5.1. General Purpose I/O Registers

The device contains three General Purpose I/O Registers, General Purpose I/O Register 0/1/2 (GPIOR 0/1/2). These registers can be used for storing any information, and they are particularly useful for storing global variables and Status Flags. General Purpose I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

Related Links

Register Summary on page 446
Instruction Set Summary on page 449
Memory Programming on page 374

13.6. Register Description

13.6.5. GPIOR2 – General Purpose I/O Register 2

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: GPIOR2
Offset: 0x4B
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2B

Bit	7	6	5	4	3	2	1	0
	GPIOR2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPIOR2[7:0]: General Purpose I/O

15. Power Management and Sleep Modes

Sleep modes enable the application to shut down unused modules in the MCU, thereby saving power. The device provides various sleep modes allowing the user to tailor the power consumption to the application requirements.

When enabled, the Brown-out Detector (BOD) actively monitors the power supply voltage during the sleep periods. To further save power, it is possible to disable the BOD in some sleep modes. See also BOD Disable.

15.1. Sleep Modes

The following Table shows the different sleep modes, their wake-up sources, and BOD disable ability.

Table 15-1. Active Clock Domains and Wake-up Sources in the Different Sleep Modes.

	Active Clock Domains					Oscillators		Wake-up Sources								Software BOD Disable	
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT and PCINT	TWI Address Match	Timer2	SPM/ EEPROM Ready	ADC	WDT	USART[4]	Other I/O		
Idle			Yes	Yes	Yes	Yes	Yes[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
ADC Noise Reduction				Yes	Yes	Yes	Yes[2]	Yes[3]	Yes	Yes[2]	Yes	Yes	Yes	Yes			
Power-down								Yes[3]	Yes				Yes	Yes		Yes	
Power-save					Yes		Yes[2]	Yes[3]	Yes	Yes			Yes	Yes		Yes	
Standby[1]						Yes		Yes[3]	Yes				Yes	Yes		Yes	
Extended Standby					Yes[2]	Yes	Yes[2]	Yes[3]	Yes	Yes			Yes	Yes		Yes	

Note:

1. Only recommended with external crystal or resonator selected as clock source.
2. If Timer/Counter2 is running in asynchronous mode.
3. For INT1 and INT0, only level interrupt.
4. Start frame detection, only.

To enter any of the six sleep modes, the Sleep Enable bit in the Sleep Mode Control Register (SMCR.SE) must be written to '1' and a SLEEP instruction must be executed. Sleep Mode Select bits (SMCR.SM[2:0]) select which sleep mode (Idle, ADC Noise Reduction, Power-down, Power-save, Standby, or Extended Standby) will be activated by the SLEEP instruction.

Note: The block diagram in the section *System Clock and Clock Options* provides an overview over the different clock systems in the device, and their distribution. This figure is helpful in selecting an appropriate sleep mode.

If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up. The MCU is then halted for four cycles in addition to the start-up time, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the Register File and SRAM are unaltered when the device wakes up from sleep. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

Related Links

System Clock and Clock Options on page 48

Address	Labels		Code Comments
0x016	rjmp	EE_RDY	; EEPROM Ready Handler
0x017	rjmp	ANA_COMP	; Analog Comparator Handler
0x018	rjmp	TWI	; 2-wire Serial Interface Handler
0x019	rjmp	SPM_RDY	; Store Program Memory Ready Handler
;			
0x01A	RESET: ldi	r16, high(RAMEND)	; Main program start
0x01B	out	SPH,r16	; Set Stack Pointer to top of RAM
0x01C	ldi	r16, low(RAMEND)	
0x01D	out	SPL,r16	
0x01E	sei		; Enable interrupts
0x01F	<instr>	xxx	

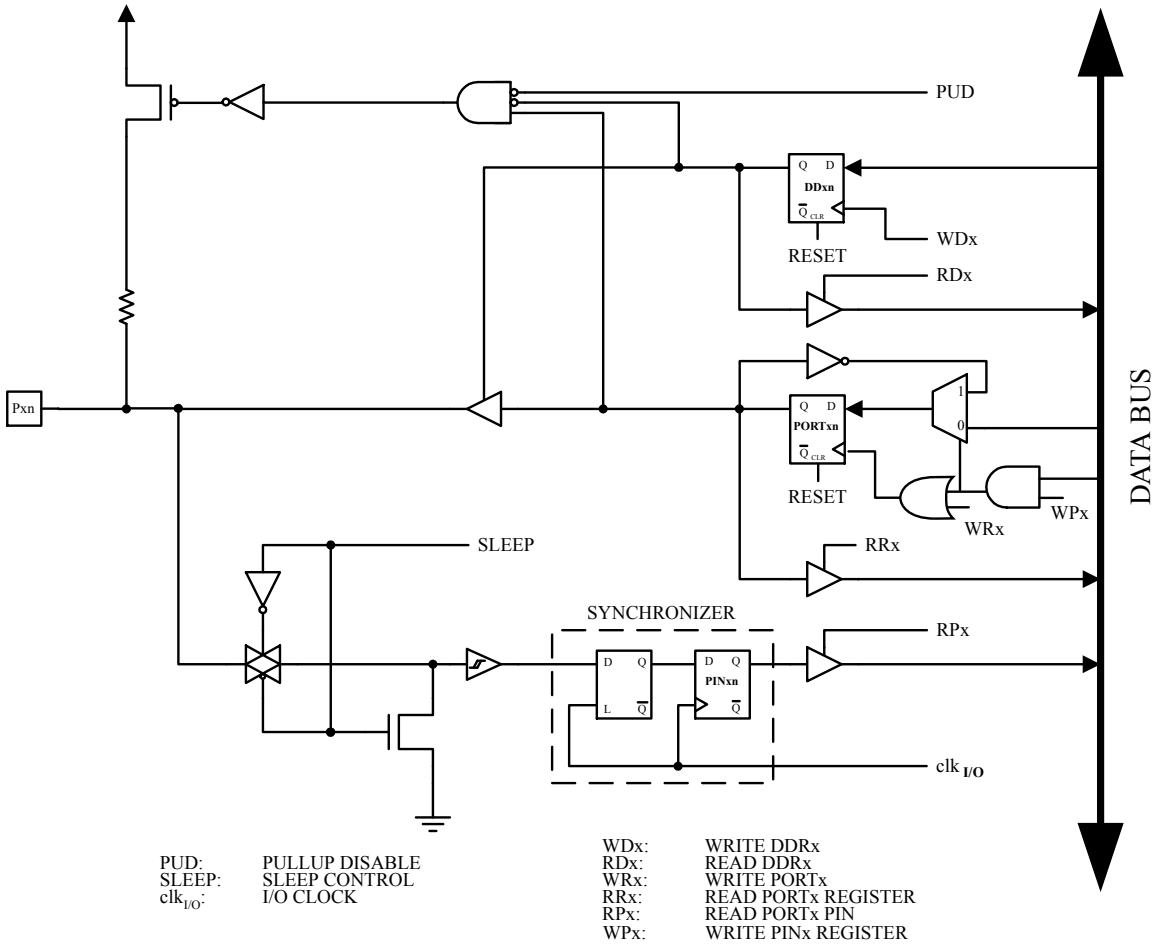
When the BOOTRST Fuse is unprogrammed, the Boot section size set to 2Kbytes and the IVSEL bit in the MCUCR Register (MCUCR.IVSEL) is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega88PB is:

Address	Labels		Code Comments
0x000	RESET: ldi	r16,high(RAMEND)	; Main program start
0x001	out	SPH,r16	; Set Stack Pointer to top of RAM
0x002	ldi	r16,low(RAMEND)	
0x003	out	SPL,r16	
0x004	sei		; Enable interrupts
0x005	<instr>	xxx	
;			
.org	0xC01		
0xC01	rjmp	EXT_INT0	; IRQ0 Handler
0xC02	rjmp	EXT_INT1	; IRQ1 Handler
...	...		...
;			
0xC19	rjmp	SPM_RDY	; Store Program Memory Ready Handler

19.2. Ports as General Digital I/O

The ports are bi-directional I/O ports with optional internal pull-ups. The following figure shows the functional description of one I/O-port pin, here generically called Pxn.

Figure 19-2. General Digital I/O(1)



Note: 1. WRx, WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports.

19.2.1. Configuring the Pin

Each port pin consists of three register bits: DDxn, PORTxn, and PINxn. As shown in the Register Description, the DDxn bits are accessed at the DDRx I/O address, the PORTxn bits at the PORTx I/O address, and the PINxn bits at the PINx I/O address.

The DDxn bit in the DDRx Register selects the direction of this pin. If DDxn is written to '1', Pxn is configured as an output pin. If DDxn is written to '0', Pxn is configured as an input pin.

If PORTxn is written to '1' when the pin is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTxn has to be written to '0' or the pin has to be configured as an output pin. The port pins are tri-stated when reset condition becomes active, even if no clocks are running.

If PORTxn is written to '1' when the pin is configured as an output pin, the port pin is driven high. If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low.

19.4.3. Port B Data Direction Register

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: DDRB
Offset: 0x24
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x04

Bit	7	6	5	4	3	2	1	0
	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – DDRBn: Port B Data Direction [n = 7:0]

19.4.13. Port E Input Pins Address

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: PINE
Offset: 0x2C
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x0C

Bit	7	6	5	4	3	2	1	0
					PINE3	PINE2	PINE1	PINE0
Access					R/W	R/W	R/W	R/W
Reset					x	x	x	x

Bits 3:0 – PINEn: Port E Input Pins Address [n = 3:0]
Writing to the pin register provides toggle functionality for I/O.

CS12	CS11	CS10	Description
1	0	0	clkI/O/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

21.12.12. Timer/Counter 1 Interrupt Mask Register

Name: TIMSK1
Offset: 0x6F
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			ICIE1			OCIE1B	OCIE1A	TOIE1
Access			R/W			R/W	R/W	R/W
Reset			0			0	0	0

Bit 5 – ICIE1: Input Capture Interrupt Enable
When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Input Capture interrupt is enabled. The corresponding Interrupt Vector is executed when the ICF Flag, located in TIFR1, is set.

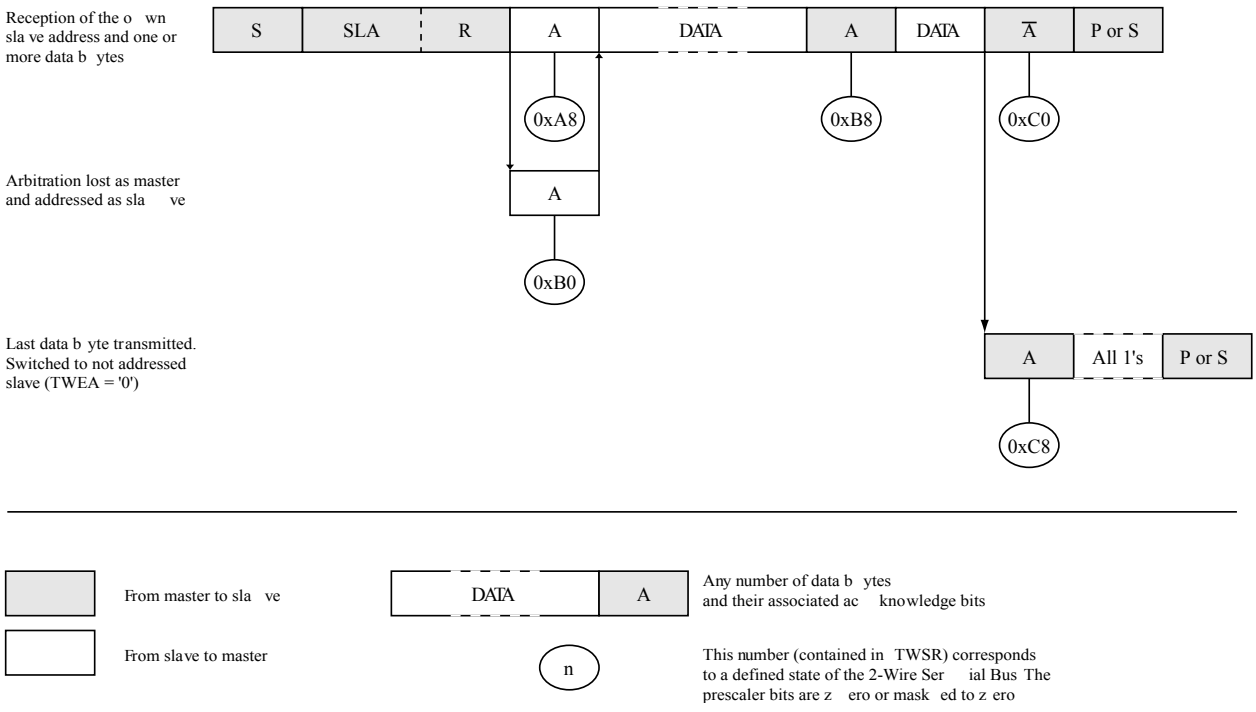
Bit 2 – OCIE1B: Output Compare B Match Interrupt Enable
When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter Output Compare B Match interrupt is enabled. The corresponding Interrupt Vector is executed when the OCFB Flag, located in TIFR1, is set.

Bit 1 – OCIE1A: Output Compare A Match Interrupt Enable
When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter Output Compare A Match interrupt is enabled. The corresponding Interrupt Vector is executed when the OCFA Flag, located in TIFR1, is set.

Bit 0 – TOIE1: Overflow Interrupt Enable
When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter 1 Overflow interrupt is enabled. The corresponding Interrupt Vector is executed when the TOV Flag, located in TIFR1, is set.

Status Code (TWSRb) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application SofTWARne Response					Next Action Taken by TWI Hardware
		To/from TWDRn	To TWCRn				
			STA	STO	TWINT	TWEA	
0xC8	Last data byte in TWDRn has been transmitted (TWEA = “0”); ACK has been received	No TWDRn action	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
			0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = “1”
			1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
			1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if TWGCE = “1”; a START condition will be transmitted when the bus becomes free

Figure 27-18. Formats and States in the Slave Transmitter Mode



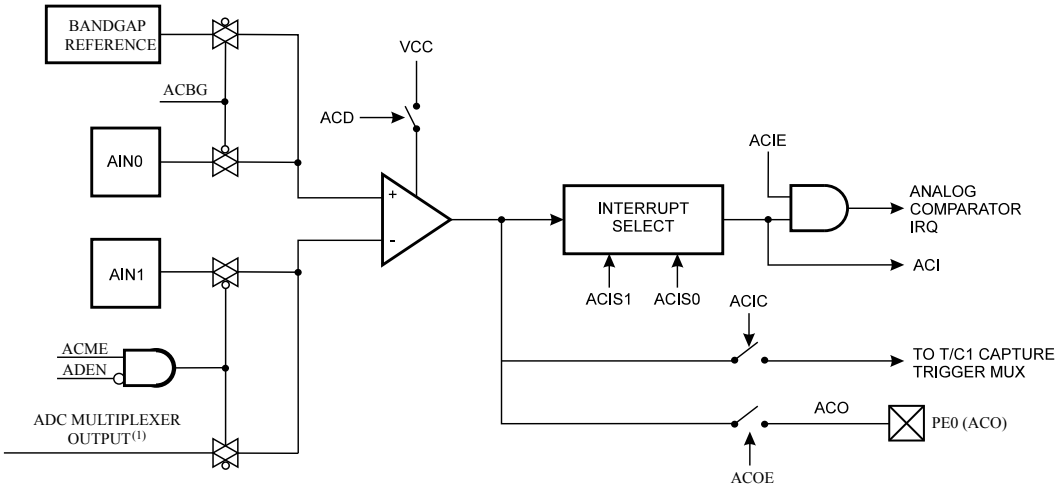
28. AC - Analog Comparator

28.1. Overview

The Analog Comparator compares the input values on the positive pin AIN0 and negative pin AIN1. When the voltage on the positive pin AIN0 is higher than the voltage on the negative pin AIN1, the Analog Comparator output, ACO, is set. The comparator's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown below.

The Power Reduction ADC bit in the Power Reduction Register (PRR.PRADC) must be written to '0' in order to be able to use the ADC input MUX.

Figure 28-1. Analog Comparator Block Diagram



Note: Refer to the *Pin Configuration* and the I/O Ports description for Analog Comparator pin placement

Related Links

I/O-Ports on page 105

Power Management and Sleep Modes on page 60

Pin Configurations on page 14

28.2. Analog Comparator Multiplexed Input

It is possible to select any of the ADC[7..0] pins to replace the negative input to the Analog Comparator. The ADC multiplexer is used to select this input, and consequently, the ADC must be switched off to utilize this feature. If the Analog Comparator Multiplexer Enable bit in the ADC Control and Status Register B (ADCSRB.ACME) is '1' and the ADC is switched off (ADCSRA.ADEN=0), the three least significant Analog Channel Selection bits in the ADC Multiplexer Selection register (ADMUX.MUX[2..0]) select the input pin to replace the negative input to the Analog Comparator, as shown in the table below. When ADCSRB.ACME=0 or ADCSRA.ADEN=1, AIN1 is applied to the negative input of the Analog Comparator.

28.3.2. Analog Comparator Control and Status Register C

The Store Program Memory Control and Status Register contains the control bits needed to control the Boot Loader operations.

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: ACSR0
Offset: 0x4F
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2F

Bit	7	6	5	4	3	2	1	0
								ACOE
Access								R/W
Reset								0

Bit 0 – ACOE: Analog Comparator Output Enable
When this bit is set, the analog comparator output is connected to the ACO pin.

Table 32-12. Explanation of Different Variables used in Figure 32-3 Addressing the Flash During SPM ATmega168PB

Variable		Corresponding Z-value(1)	Description
PCMSB	12		Most significant bit in the Program Counter. (The Program Counter is 13 bits PC[12:0])
PAGEMSB	5		Most significant bit which is used to address the words within one page (64 words in a page requires 6 bits PC [5:0])
ZPCMSB		Z13	Bit in Z-register that is mapped to PCMSB. Because Z0 is not used, the ZPCMSB equals PCMSB + 1.
ZPAGEMSB		Z6	Bit in Z-register that is mapped to PAGEMSB. Because Z0 is not used, the ZPAGEMSB equals PAGEMSB + 1.
PCPAGE	PC[12:6]	Z13:Z7	Program counter page address: Page select, for page erase and page write
PCWORD	PC[5:0]	Z6:Z1	Program counter word address: Word select, for filling temporary buffer (must be zero during page write operation)

Note: 1. Z15:Z14: always ignored

Z0: should be zero for all SPM commands, byte select for the LPM instruction.

Please refer to Addressing the Flash During Self-Programming or details about the use of Z-pointer during Self- Programming.

32.9. Register Description

4. No clk is applied to the pad during power-down mode.

34.2.2. ATmega168PB DC Characteristics

Table 34-4. ATmega168PB DC characteristics - T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition		Min.	Typ.(2)	Max.	Units
ICC	Power Supply Current(1)	Active 1MHz, VCC = 2V	T = 85°C		0.35	0.5	mA
			T = 105°C		0.35	0.6	
		Active 4MHz, VCC = 3V	T = 85°C		0.9	2.5	
			T = 105°C		0.9	2.75	
		Active 8MHz, VCC = 5V	T = 85°C		5.0	9	
			T = 105°C		5.0	10	
		Idle 1MHz, VCC = 2V	T = 85°C		0.06	0.15	
			T = 105°C		0.06	0.2	
		Idle 4MHz, VCC = 3V	T = 85°C		0.37	0.7	
			T = 105°C		0.37	0.8	
		Idle 8MHz, VCC = 5V	T = 85°C		1.4	2.7	
			T = 105°C		1.4	3	
	Power-save mode(3)	32kHz TOSC enabled, V_{CC} = 1.8V	T = 85°C		1.38		µA
			T = 105°C		1.38		
		32kHz TOSC enabled, V_{CC} = 3V	T = 85°C		1.54		
			T = 105°C		1.54		
	Power-down mode(3)(4)	WDT enabled, VCC = 3V	T = 85°C		2.43	8	
			T = 105°C		2.43	10	
		WDT disabled, VCC = 3V	T = 85°C		0.21	2	
			T = 105°C		0.21	5	

Note:

1. Values with *Minimizing Power Consumption* enabled (0xFF).
2. Typical values at 25°C. Maximum values are test limits in production.
3. The current consumption values include input leakage current.
4. No clock is applied to the pad during power-down mode.

Related Links

Minimizing Power Consumption on page 63

34.3. Speed Grades

Maximum frequency is dependent on V_{CC}. As shown in Figure. Maximum Frequency vs. V_{CC}, the Maximum Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V and between 2.7V < V_{CC} < 4.5V.

Figure 35-50. ATmega168PB: Active Supply Current vs. Frequency (1-20MHz)

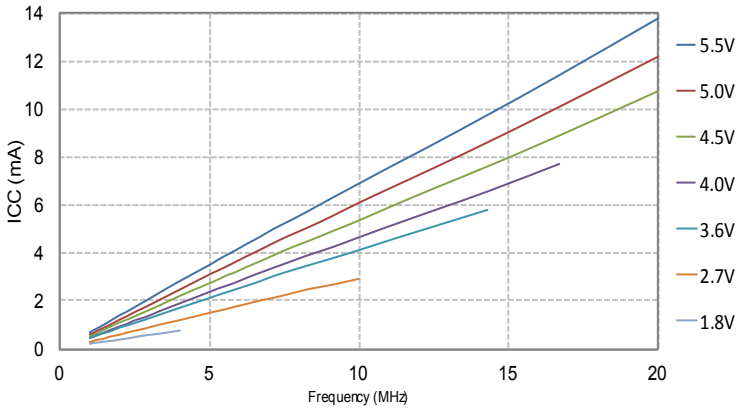


Figure 35-51. ATmega168PB: Active Supply Current vs. V_{CC} (Internal RC Oscillator, 128kHz)

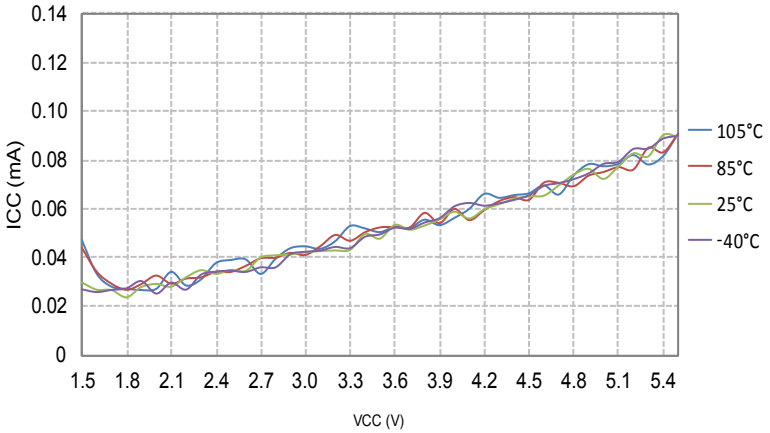


Figure 35-52. ATmega168PB: Active Supply Current vs. V_{CC} (Internal RC Oscillator, 1MHz)

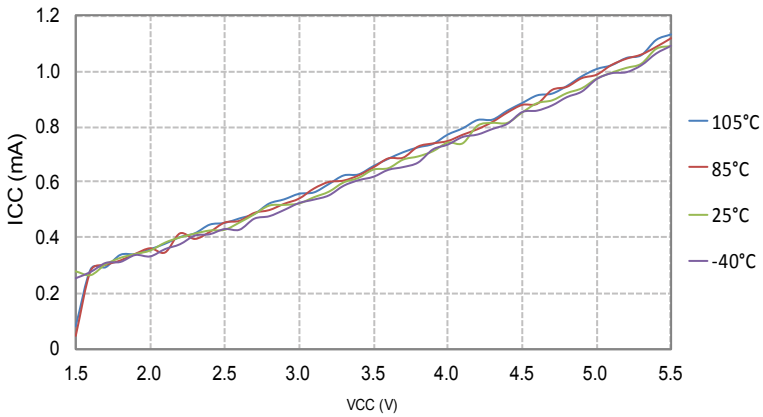
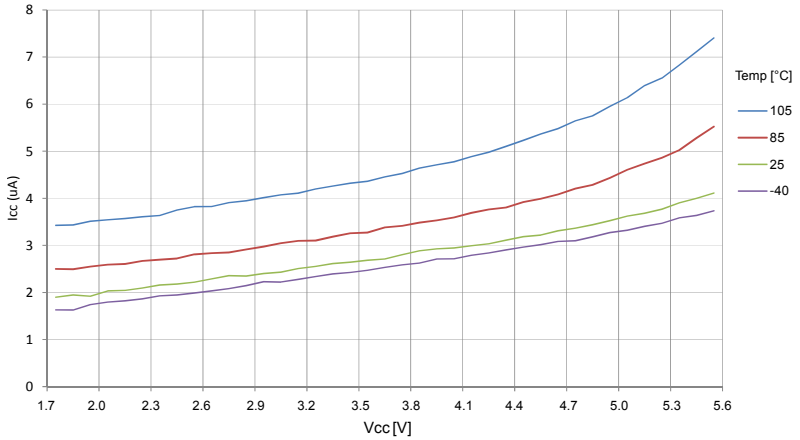


Figure 35-60. ATmega168PB: Power-Down Supply Current vs. V_{CC} (Watchdog Timer Enabled)



35.2.5. Power-save Supply Current

Figure 35-61. ATmega168PB: Power-Save Supply Current vs. V_{CC}

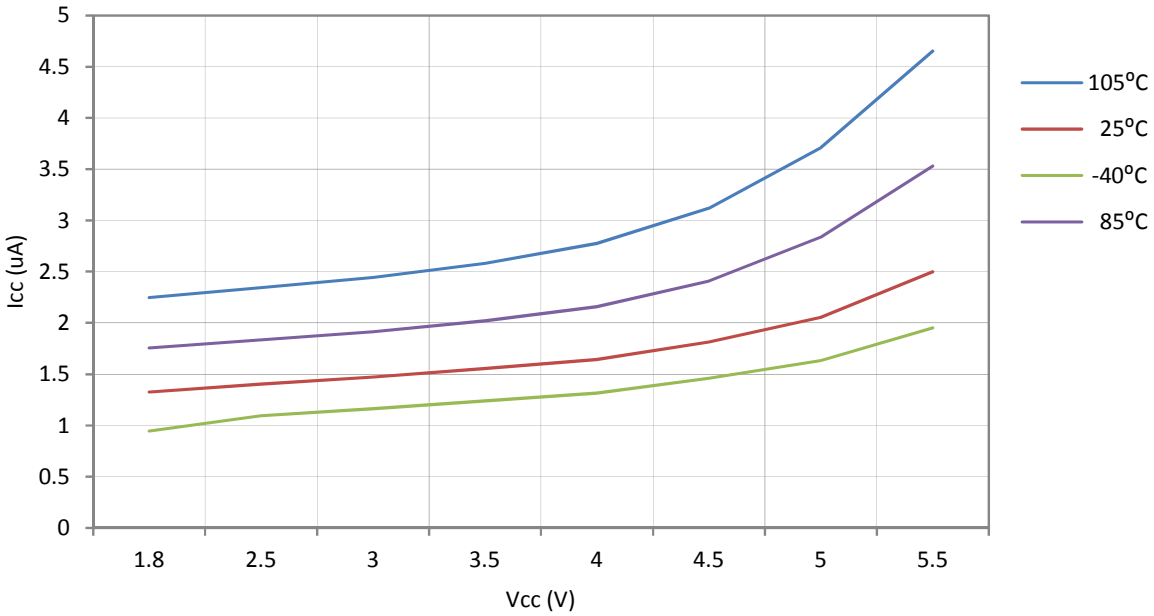


Figure 35-80. ATmega168PB: BOD Thresholds vs. Temperature (BODLEVEL is 2.7V)

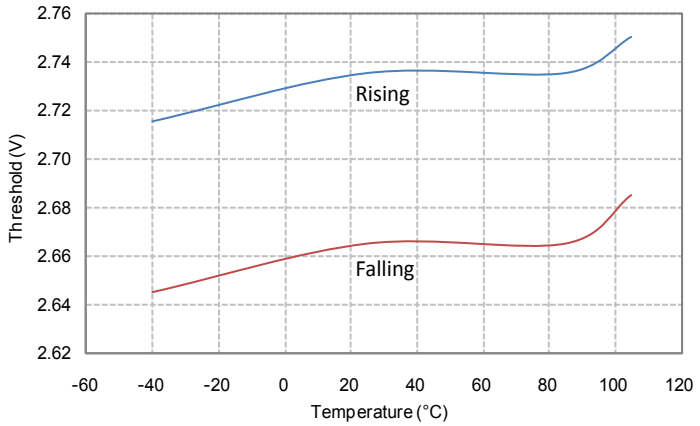


Figure 35-81. ATmega168PB: BOD Thresholds vs. Temperature (BODLEVEL is 4.3V)

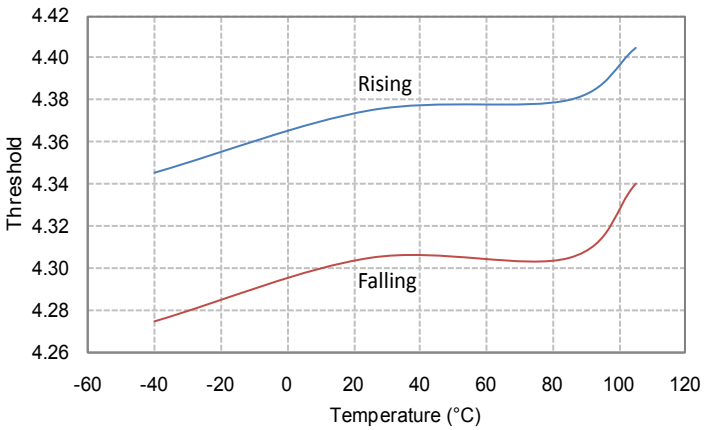


Figure 35-82. ATmega168PB: Calibrated Bandgap Voltage vs. Temperature

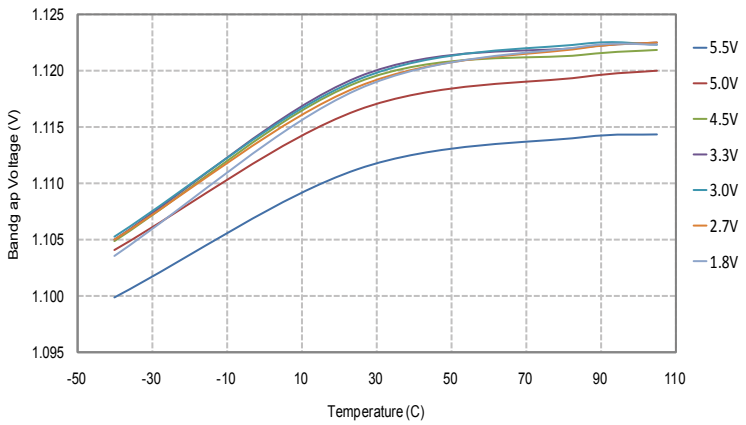


Figure 35-85. ATmega168PB: Watchdog Oscillator Frequency vs. V_{CC}

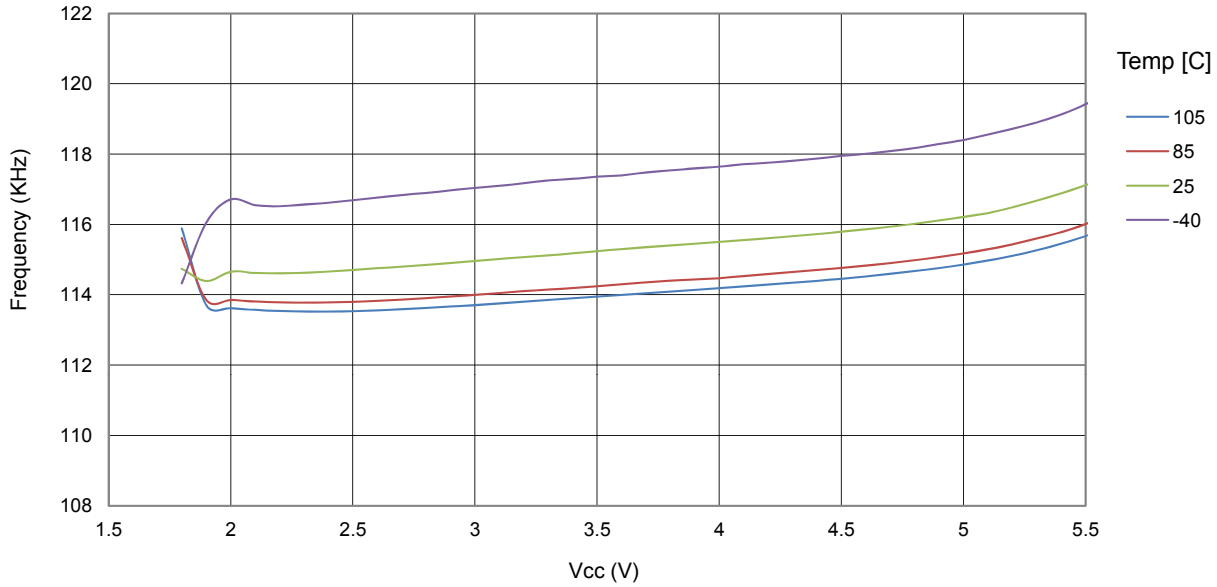


Figure 35-86. ATmega168PB: Calibrated 8MHz RC Oscillator Frequency vs. V_{CC}