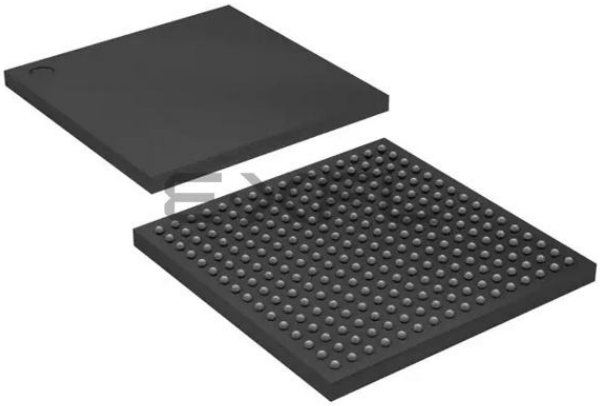

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	903
Number of Logic Elements/Cells	14448
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c15af256a7n

Chapter Revision Dates

The chapters in this book, *Cyclone II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *February 2008*
Part number: *CII51001-3.2*

Chapter 2. Cyclone II Architecture
Revised: *February 2007*
Part number: *CII51002-3.1*

Chapter 3. Configuration & Testing
Revised: *February 2007*
Part number: *CII51003-2.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *February 2007*
Part number: *CII51004-3.1*

Chapter 5. DC Characteristics and Timing Specifications
Revised: *February 2008*
Part number: *CII51005-4.0*

Chapter 6. Reference & Ordering Information
Revised: *February 2007*
Part number: *CII51006-1.4*

Chapter 7. PLLs in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51007-3.1*

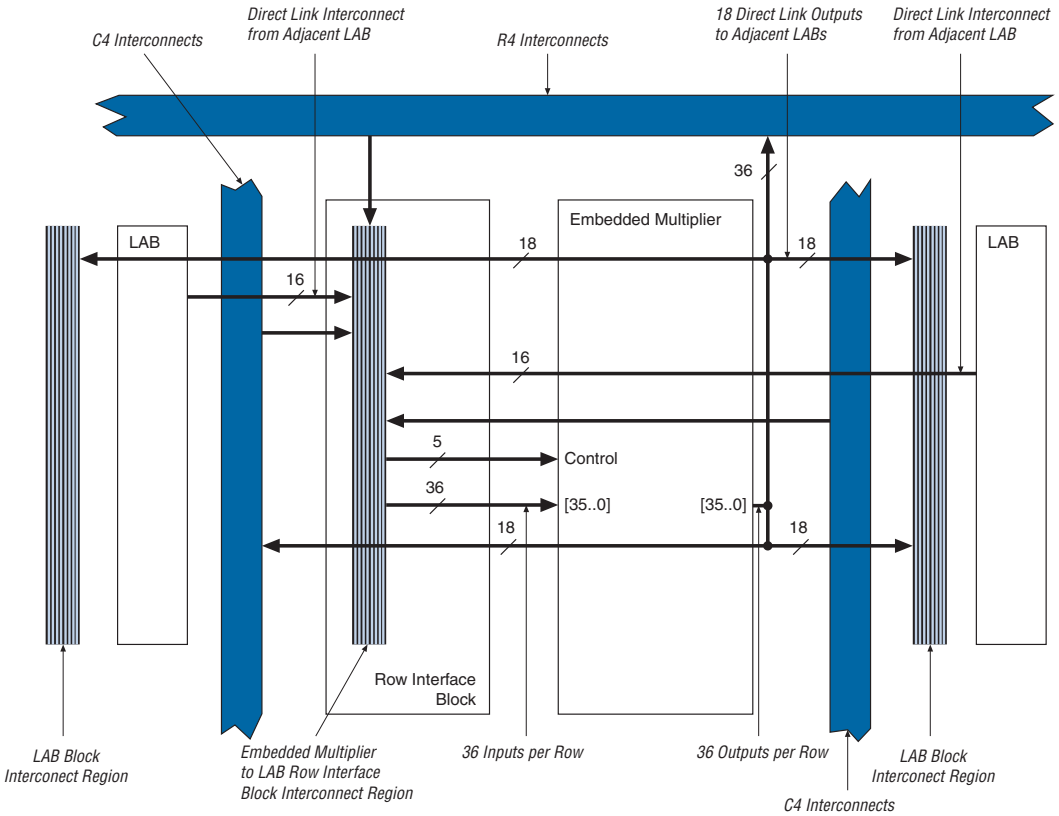
Chapter 8. Cyclone II Memory Blocks
Revised: *February 2008*
Part number: *CII51008-2.4*

Chapter 9. External Memory Interfaces
Revised: *February 2007*
Part number: *CII51009-3.1*

Embedded Multiplier Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the embedded multiplier row interface interconnect. The embedded multipliers can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the embedded multiplier are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. Embedded multiplier outputs can also connect to left and right LABs through 18 direct link interconnects each. Figure 2–19 shows the embedded multiplier to logic array interface.

Figure 2–19. Embedded Multiplier LAB Row Interface



Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

areset

The PLL areset signal is the reset and resynchronization input for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL input and output clocks. You should include the areset signal in designs if any of the following conditions are true:

- Manual clock switchover is enabled in the design
- Phase relationships between input and output clocks need to be maintained after a loss of lock condition
- If the input clock to the PLL is not toggling or is unstable upon powerup, assert the areset signal after the input clock is toggling, staying within the input jitter specification

Altera recommends using the areset and locked signals in your designs to control and observe the status of your PLL.

The areset signal is an active high signal and, when driven high, the PLL counters reset, clearing the PLL output and causing the PLL to lose lock. The VCO is also set back to its nominal frequency. The clock outputs from the PLL are driven to ground as long as areset is active. When areset transitions low, the PLL resynchronizes to its input clock as the PLL relocks. If the target VCO frequency is below this nominal frequency, then the PLL clock output frequency starts at a higher value than desired during the lock process. In this case, Altera recommends monitoring the gated locked signal to ensure the PLL is fully in lock before enabling the clock outputs from the PLL. The Cyclone II device can drive this PLL input signal from LEs or any general-purpose I/O pin. The areset signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to GND.

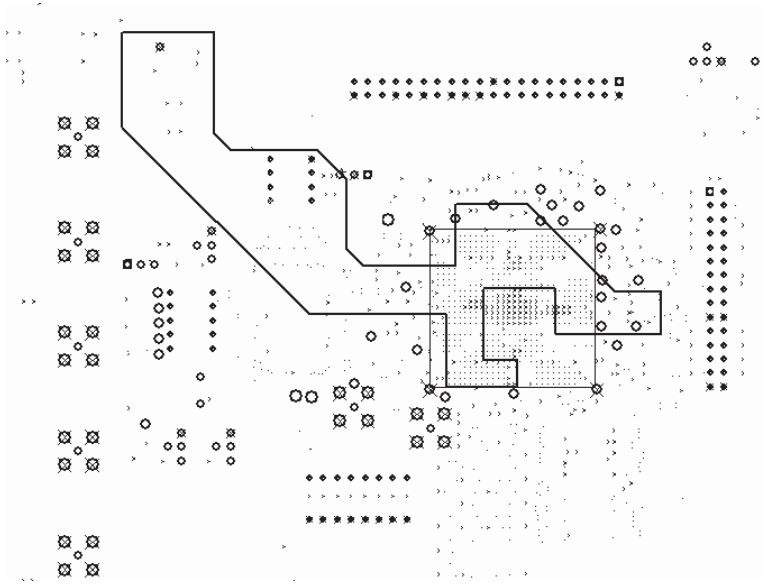
pfdena

The pfdena signal is an active high signal that controls the PFD output in the PLL with a programmable gate. If you disable the PFD by transitioning pfdena low, the VCO operates at its last set control voltage and frequency value with some long-term drift to a lower frequency. Even though the PLL clock outputs continue to toggle regardless of the input clock, the PLL could lose lock. The system continues running when the PLL goes out of lock or if the input clock is disabled. By maintaining the current frequency, the system has time to store its current settings before shutting down. If the pfdena signal transitions high, the PLL relocks and resynchronizes to the input clock. The pfdena input signal can be driven by any general-purpose I/O pin or from LEs. This signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

Table 7–8. Global Clock Network Connections (Part 2 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PLL4_c0													✓	✓		✓
PLL4_c1													✓		✓	✓
PLL4_c2														✓	✓	
DPCLK0 *(1)*	✓															
DPCLK1 *(1)*		✓														
DPCLK10 *(1)*, *(2)* CDPCLK0 or CDPCLK7 *(3)*			✓													
DPCLK2 *(1)*, *(2)* CDPCLK1 or CDPCLK2 *(3)*				✓												
DPCLK7 *(1)*					✓											
DPCLK6 *(1)*						✓										
DPCLK8 *(1)*, *(2)* CDPCLK5 or CDPCLK6 *(3)*							✓									
DPCLK4 *(1)*, *(2)* CDPCLK4 or CDPCLK3 *(3)*								✓								
DPCLK8 *(1)*									✓							
DPCLK11 *(1)*										✓						
DPCLK9 *(1)*											✓					
DPCLK10 *(1)*												✓				
DPCLK5 *(1)*													✓			
DPCLK2 *(1)*														✓		
DPCLK4 *(1)*															✓	

Figure 7–16. V_{CCINT} Plane Partitioned for VCCA Island



Thick VCCA Trace

Because of board constraints, you may not be able to partition a VCCA island. Instead, run a thick trace from the power supply to each VCCA pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each VCCA pin with a decoupling circuit shown in Figure 7–17. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10 µF tantalum parallel capacitor where the power enters the board. Decouple each VCCA pin with a 0.1 µF and 0.001 µF parallel combination of ceramic capacitors located as close as possible to the Cyclone II device. You can connect the GNDA pins directly to the same ground plane as the device's digital ground.

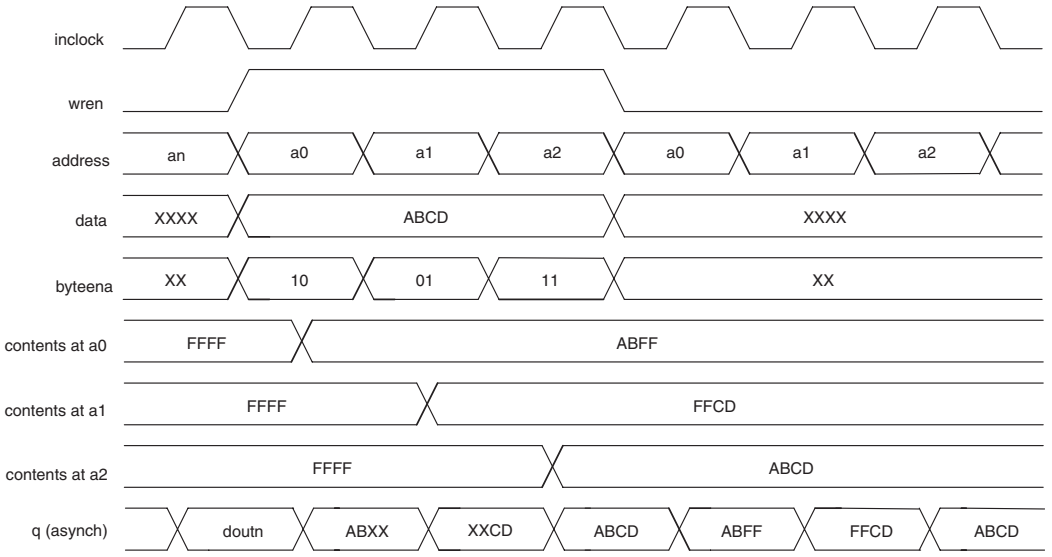
Table 8–1. Summary of M4K Memory Features (Part 2 of 2)	
Feature	**M4K Blocks**
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓
Embedded shift register mode *(2)*	✓
ROM mode	✓
FIFO buffer *(2)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support	✓
Memory Initialization File (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register clears	Output registers only
Same-port read-during-write	New data available at positive clock edge
Mixed-port read-during-write	Old data available at positive clock edge

Notes to Table 8–1:
(1) Maximum performance information is preliminary until device characterization.
(2) FIFO buffers and embedded shift registers require external logic elements (LEs) for implementing control logic.

Table 8–2 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device family member.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 1 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C5	26	119,808
EP2C8	36	165,888
EP2C15	52	239,616
EP2C20	52	239,616
EP2C35	105	483,840

Figure 8–2. Cyclone II Byte Enable Functional Waveform



Packed Mode Support

Cyclone II M4K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

- Each of the two independent block sizes is less than or equal to half of the M4K block size. The maximum data width for each independent block is 18 bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

See "Single-Port Mode" on page 8–9 and "Single-Clock Mode" on page 8–24 for more information.

Address Clock Enable

Cyclone II M4K memory blocks support address clock enables, which holds the previous address value until needed. When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable.

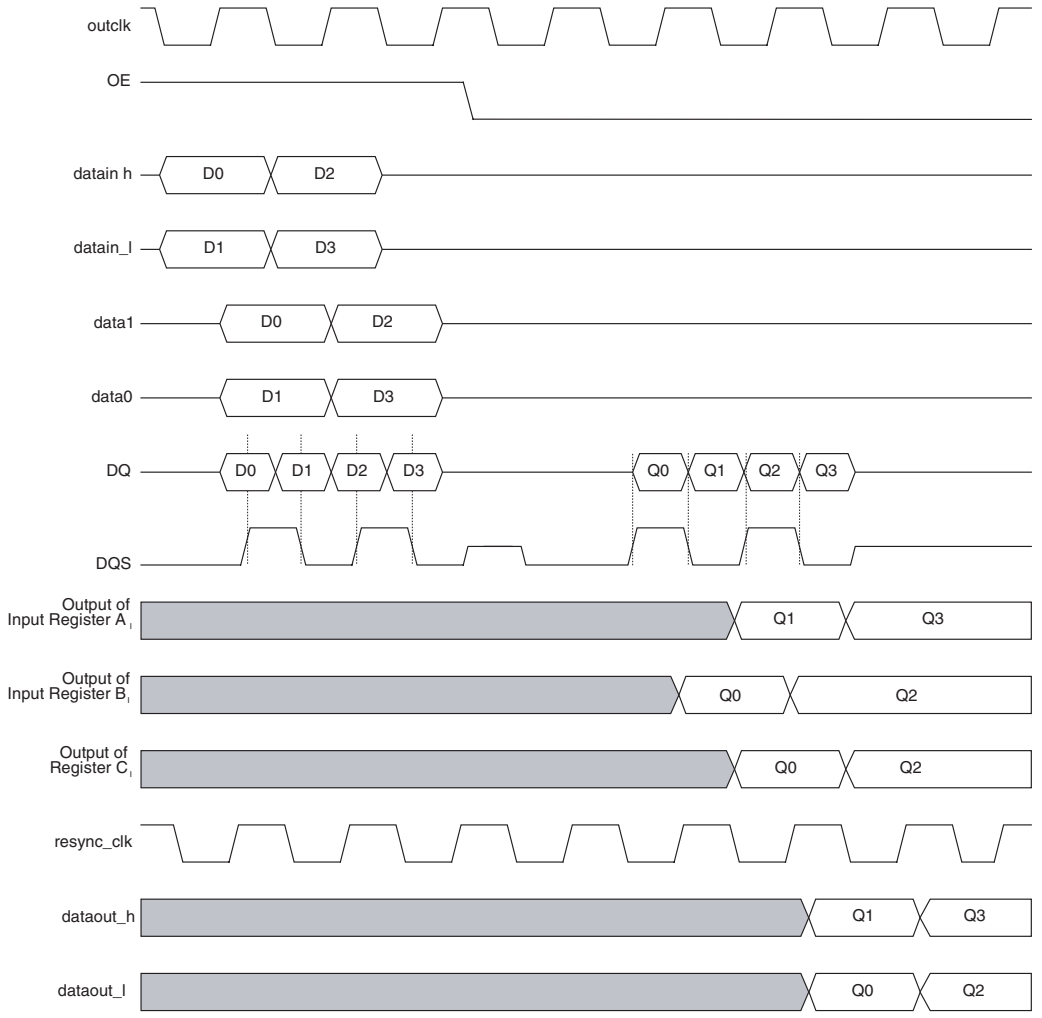
Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	• Added document revision history. • Updated "Packed Mode Support" section. • Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	• In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. • Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Figure 9–17. DDR Bidirectional Waveforms



Conclusion

Cyclone II devices support SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The clock delay control circuitry allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

12. Embedded Multipliers in Cyclone II Devices

CII51012-1.2

Introduction

Use Cyclone® II FPGAs alone or as digital signal processing (DSP) co-processors to improve price-to-performance ratios for DSP applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II device features and design support:

- Up to 150 18 x 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interface to external memory
- DSP Intellectual Property (IP) cores
- DSP Builder interface to the Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

This chapter focuses on the Cyclone II embedded multiplier blocks.

Cyclone II devices have embedded multiplier blocks optimized for multiplier-intensive low-cost DSP applications. These embedded multipliers combined with the flexibility of programmable logic devices (PLDs), provide you with the ability to efficiently implement various cost sensitive DSP functions easily. Consumer-based application systems such as digital television (DTV) and home entertainment systems typically require a cost effective solution for implementing multipliers to perform signal processing functions like finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Along with the embedded multipliers, the M4K memory blocks in Cyclone II devices also support various soft multiplier implementations. These, in combination with the embedded multipliers increase the available number of multipliers in Cyclone II devices and provide the user with a wide variety of implementation options and flexibility when designing their systems.

See the Cyclone II Device Family Data Sheet section in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II devices.

Document Revision History

Table 12–4 shows the revision history for this document.

Table 12–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.2	• Added document revision history. • Updated "Software Support" section.	• Removed reference to third-party synthesis tool: LeonardoSpectrum and Synplify.
November 2005 v2.1	Updated Introduction.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

During initialization, the initialization clock source is either the Cyclone II 10 MHz (typical) internal oscillator (separate from the AS internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone II device provides itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. You can also make use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

If an error occurs at any point during configuration, the FPGA with the error drives the nSTATUS signal low. If you enable the **Auto-restart configuration after error** option, the entire chain begins reconfiguration after a reset time-out period (a maximum of 40 µs). If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The microprocessor or controller can pulse nCONFIG if it is under system control rather than tied to V_{CC}.

While you can cascade Cyclone II devices, serial configuration devices cannot be cascaded or chained together.

If you use the optional CLKUSR pin and the nCONFIG is pulled low to restart configuration during device initialization, make sure the CLKUSR pin continues to toggle while nSTATUS is low (a maximum of 40 µs).

Configuration Stage

When the nSTATUS pin transitions high, the configuration device's OE pin also transitions high and the configuration device clocks data out serially to the FPGA using its internal oscillator. The Cyclone II device receives configuration data on its DATA0 pin and the clock is received on the DCLK pin. Data is latched into the FPGA on the rising edge of DCLK.

After the FPGA has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by a pull-up resistor. Since the Cyclone II device's CONF_DONE pin is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the nCS pin. You can turn this option on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you do not use this internal pull-up resistor, you need to connect an external 10-kΩ pull-up resistor to the nCS and CONF_DONE line. A low-to-high transition on CONF_DONE indicates configuration is complete, and the device can begin initialization.

Initialization Stage

In Cyclone II devices, the default initialization clock source is the Cyclone II internal oscillator (typically 10 MHz). Cyclone II devices can also use the optional CLKUSR pin. If your design uses the internal oscillator, the Cyclone II device supplies itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to use another device or source to send additional clock cycles to the CLKUSR pin during the initialization stage. Additionally, you can use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the device, you can use the CLKUSR pin. Using the CLKUSR pin allows you to control when the Cyclone II device enters user mode. You can delay the Cyclone II devices from entering user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to properly initialize and support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor pulls it high when

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

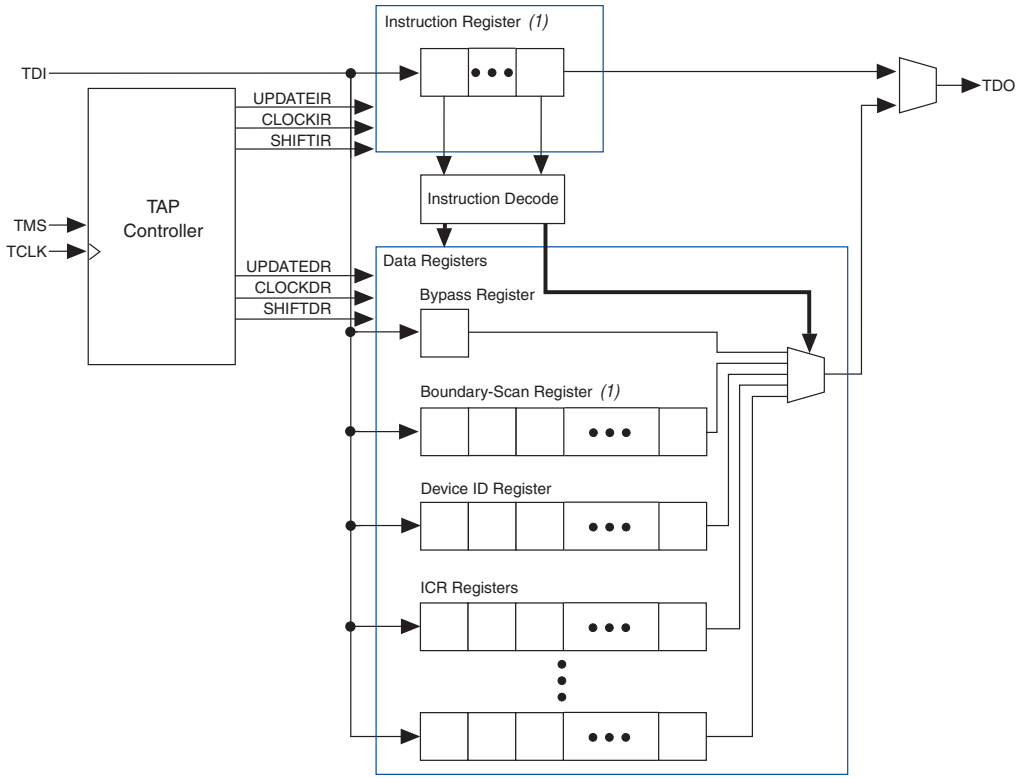
For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a 1-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 14–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 14–2. IEEE Std. 1149.1 Circuitry



Note to Figure 14–2:

(1) For register lengths, see the device data sheet in the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information on the TAP controller, see "IEEE Std. 1149.1 BST Operation Control" on page 14–6. The TMS and TCK pins

If you are testing the device after configuring it, the programmable weak pull-up resister or the bus hold feature overrides the CLAMP value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The HIGHZ instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.

I/O Voltage Support in JTAG Chain

A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone II devices, the TDO pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone II devices can support 2.5- or 3.3-V input levels.

For more information on MultiVolt I/O support, see the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook*.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 14–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.