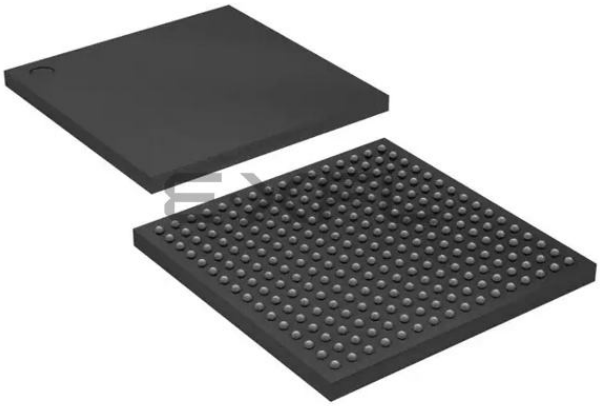

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Details	
Product Status	Active
Number of LABs/CLBs	903
Number of Logic Elements/Cells	14448
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c15af256i8n

Contents

Global Clock Network

The 16 or 8 global clock networks drive throughout the entire device. Dedicated clock pins (CLK[]), PLL outputs, the logic array, and dual-purpose clock (DPCLK[]) pins can also drive the global clock network.

The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, memory blocks, and embedded multipliers. The global clock lines can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin, or DQS signals for DDR SDRAM or QDRII SRAM interfaces. Internal logic can also drive the global clock network for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fan-out.

Clock Control Block

There is a clock control block for each global clock network available in Cyclone II devices. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device. The larger Cyclone II devices (EP2C15 devices and larger) have 16 clock control blocks, four on each side of the device. The smaller Cyclone II devices (EP2C5 and EP2C8 devices) have eight clock control blocks, four on the left and right sides of the device.

The control block has these functions:

- Dynamic global clock network clock source selection
- Dynamic enable/disable of the global clock network

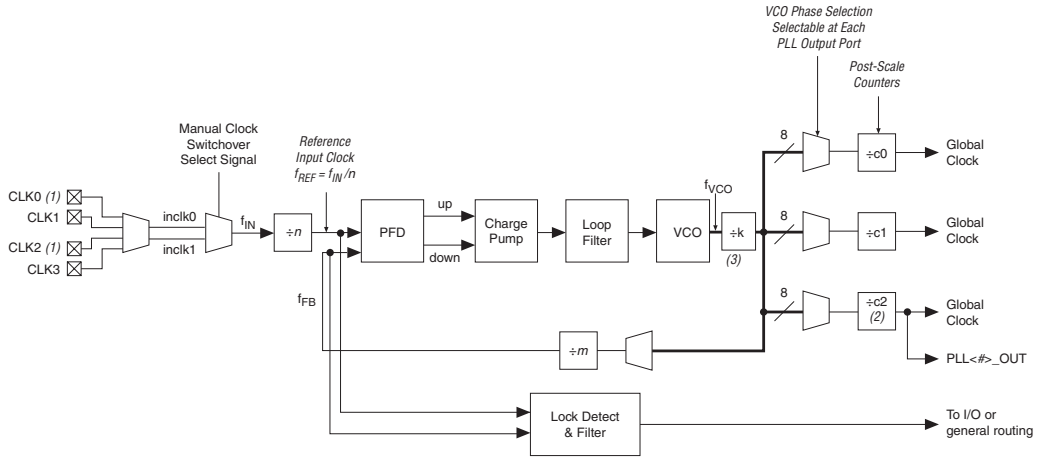
In Cyclone II devices, the dedicated CLK[] pins, PLL counter outputs, DPCLK[] pins, and internal logic can all feed the clock control block. The output from the clock control block in turn feeds the corresponding global clock network.

The following sources can be inputs to a given clock control block:

- Four clock pins on the same side as the clock control block
- Three PLL clock outputs from a PLL
- Four DPCLK pins (including CDPCLK pins) on the same side as the clock control block
- Four internally-generated signals

Figure 2–16 shows a block diagram of the Cyclone II PLL.

Figure 2–16. Cyclone II PLL *Note (1)*



Notes to Figure 2–16:

(1) This input can be single-ended or differential. If you are using a differential I/O standard, then two CLK pins are used. LVDS input is supported via the secondary function of the dedicated CLK pins. For example, the CLK0 pin's secondary function is LVDSCLK1p and the CLK1 pin's secondary function is LVDSCLK1n. If a differential I/O standard is assigned to the PLL clock input pin, the corresponding CLK(n) pin is also completely used. The Figure 2–16 shows the possible clock input connections (CLK0/CLK1) to PLL1.

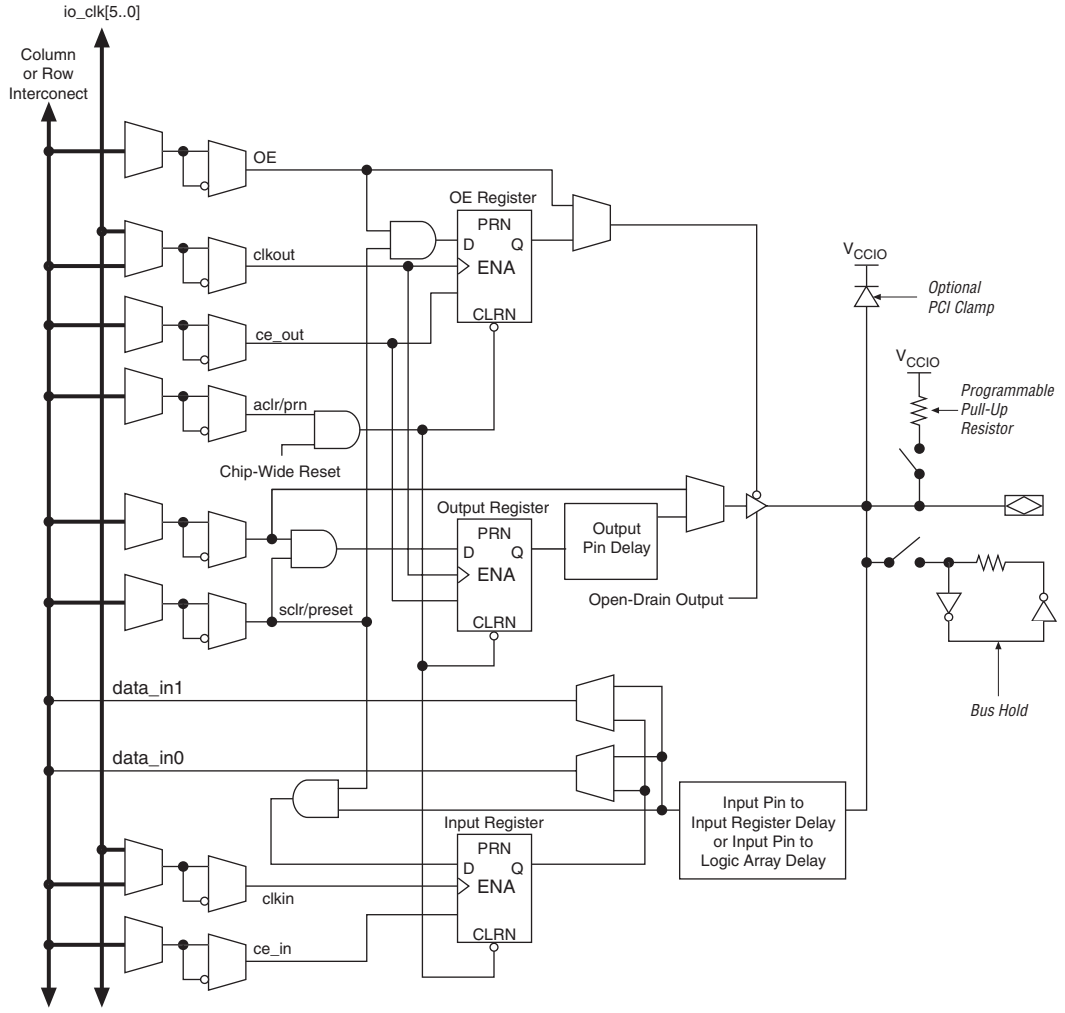
(2) This counter output is shared between a dedicated external clock output I/O and the global clock network.

For more information on Cyclone II PLLs, see the PLLs in the *Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Embedded Memory

The Cyclone II embedded memory consists of columns of M4K memory blocks. The M4K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. The output registers can be bypassed, but input registers cannot.

Figure 2–25. Cyclone II IOE in Bidirectional I/O Configuration



The Cyclone II device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time.

Document Revision History

Table 2–21 shows the revision history for this document.

Table 2–21. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Removed Table 2-1. • Updated Figure 2–25. • Added new *Note (1)* to Table 2–17. • Added handpara note in "I/O Banks" section. • Updated *Note (2)* to Table 2–20.	• Removed Drive Strength Control from Figure 2–25. • Elaboration of DDR2 and QDRII interfaces supported by I/O bank included.
November 2005 v2.1	• Updated Table 2–7. • Updated Figures 2–11 and 2–12. • Updated Programmable Drive Strength table. • Updated Table 2–16. • Updated Table 2–18. • Updated Table 2–19.	
July 2005 v2.0	• Updated technical content throughout. • Updated Table 2–16.	
February 2005 v1.2	Updated figure 2-12.	
November 2004 v1.1	Updated Table 2–19.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.179	–0.189	0.089	0.047	0.045	0.055	ns

Notes to Table 5–23:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–24. EP2C8/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.256	1.314	2.270	2.416	2.596	2.606	ns
t_{COUT}	1.258	1.316	2.286	2.429	2.604	2.614	ns
t_{PLLCIN}	–0.276	–0.294	–0.08	–0.134	–0.152	–0.142	ns
$t_{PLLCOUT}$	–0.274	–0.292	–0.064	–0.121	–0.144	–0.134	ns

Notes to Table 5–24:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C15A Clock Timing Parameters

Tables 5–25 and 5–26 show the clock timing parameters for EP2C15A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_18_ CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_HSTL_ CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—
DIFFERENTIAL_SSTL _18_CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
SSTL_18_ CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—
SSTL_18_ CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_HSTL_ CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
DIFFERENTIAL_SSTL_2 _CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60
DIFFERENTIAL_SSTL_2 _CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
DIFFERENTIAL_SSTL_ 18_CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—

Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	80–20%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—		100	—		100	—	—	100	µs

Note to Table 5–48:

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

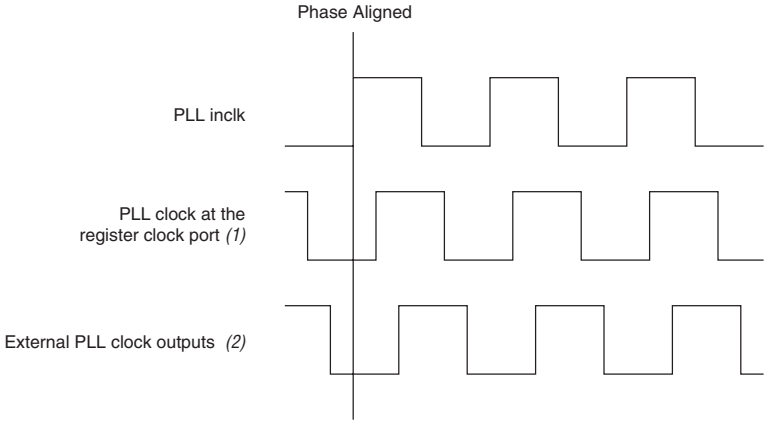
PLL Timing Specifications

Table 5–54 describes the Cyclone II PLL specifications when operating in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (–40° to 100° C), the automotive junction temperature range (–40° to 125° C), and the extended temperature range (–40° to 125° C). Follow the PLL specifications for –8 speed grade devices when operating in the industrial, automotive, or extended temperature range.

Table 5–54. PLL Specifications *Note (1)* ***(Part 1 of 2)***

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–6 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–7 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{INPFD}	PFD input frequency (–6 speed grade)	10	—	402.5	MHz
	PFD input frequency (–7 speed grade)	10	—	402.5	MHz
	PFD input frequency (–8 speed grade)	10	—	402.5	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$ *(5)*	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output)	PLL output frequency (–6 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–7 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	10	—	500	MHz
	PLL output frequency (–7 speed grade)	10	—	450	MHz
	PLL output frequency (–8 speed grade)	10	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	—	55	%
t_{JITTER} (p-p) *(2)*	Period jitter for external clock output f_{OUT_EXT} > 100 MHz	—	—	300	ps
	f_{OUT_EXT} ≤100 MHz	—	—	30	mUI
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 *(6)*	µs
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±60	ps

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode



Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

areset

The PLL areset signal is the reset and resynchronization input for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL input and output clocks. You should include the areset signal in designs if any of the following conditions are true:

- Manual clock switchover is enabled in the design
- Phase relationships between input and output clocks need to be maintained after a loss of lock condition
- If the input clock to the PLL is not toggling or is unstable upon powerup, assert the areset signal after the input clock is toggling, staying within the input jitter specification

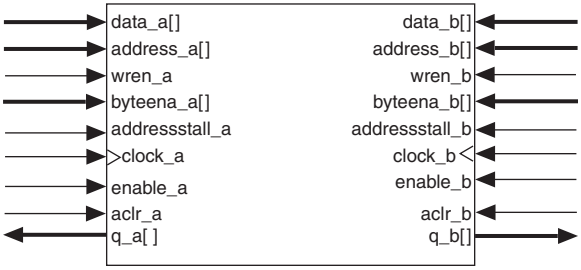
Altera recommends using the areset and locked signals in your designs to control and observe the status of your PLL.

The areset signal is an active high signal and, when driven high, the PLL counters reset, clearing the PLL output and causing the PLL to lose lock. The VCO is also set back to its nominal frequency. The clock outputs from the PLL are driven to ground as long as areset is active. When areset transitions low, the PLL resynchronizes to its input clock as the PLL relocks. If the target VCO frequency is below this nominal frequency, then the PLL clock output frequency starts at a higher value than desired during the lock process. In this case, Altera recommends monitoring the gated locked signal to ensure the PLL is fully in lock before enabling the clock outputs from the PLL. The Cyclone II device can drive this PLL input signal from LEs or any general-purpose I/O pin. The areset signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to GND.

pfdena

The pfdena signal is an active high signal that controls the PFD output in the PLL with a programmable gate. If you disable the PFD by transitioning pfdena low, the VCO operates at its last set control voltage and frequency value with some long-term drift to a lower frequency. Even though the PLL clock outputs continue to toggle regardless of the input clock, the PLL could lose lock. The system continues running when the PLL goes out of lock or if the input clock is disabled. By maintaining the current frequency, the system has time to store its current settings before shutting down. If the pfdena signal transitions high, the PLL relocks and resynchronizes to the input clock. The pfdena input signal can be driven by any general-purpose I/O pin or from LEs. This signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

Figure 8–10. Cyclone II True Dual-Port Mode *Note (1)*



Note to Figure 8–10:
(1) True dual-port memory supports input and output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K blocks in true dual-port mode is 256 × 16-bit (18-bit with parity).

The 128 × 32-bit (36-bit with parity) configuration of the M4K block is unavailable because the number of output drivers is equivalent to the maximum bit width. The maximum width of the true dual-port RAM equals half of the total number of output drivers because true dual-port RAM has outputs on two ports. Table 8–6 lists the possible M4K block mixed-port width configurations.

Table 8–6. Cyclone II Memory Block Mixed-Port Width Configurations (True Dual-Port)

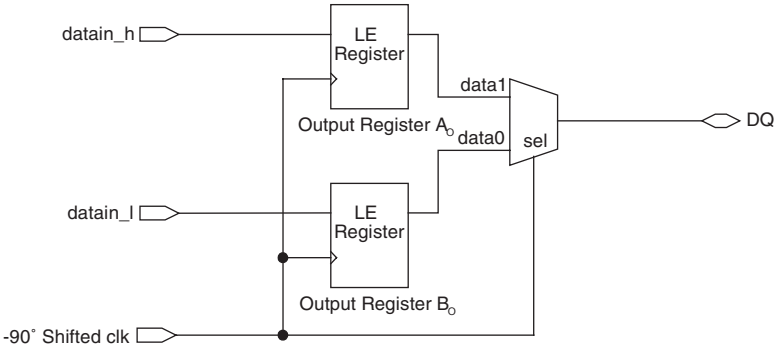
Read Port	Write Port						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

In true dual-port configuration, the RAM outputs are in read-during-write mode. This means that during a write operation, data being written to the A or B port of the RAM flows through to the A or B

DDR Output Registers

Figure 9–14 shows a schematic representation of DDR output implemented in a Cyclone II device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

Figure 9–14. DDR Output Implementation for DDR Memory Interfaces



While the clock signal is logic-high, the output from output register A_O is driven onto the DDR output pin. While the clock signal is logic-low, the output from output register B_O is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin. Altera recommends the use of `altdq` and `altdqs` megafunctions to implement this output logic. This automatically provides the required tight placement and routing constraints on the LE registers and the output multiplexer.

Figure 9–15 shows examples of functional waveforms from a DDR output implementation.

Figure 10–15. 1.5-V Differential HSTL Class I Termination

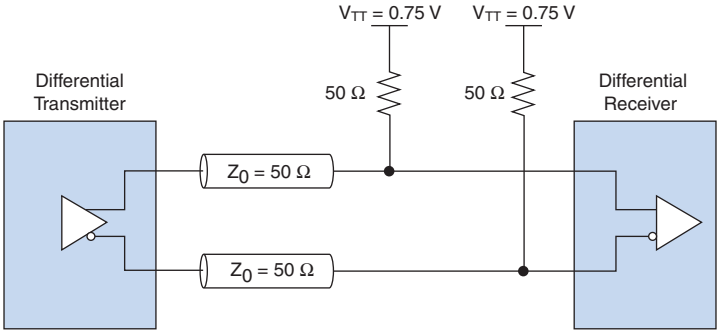
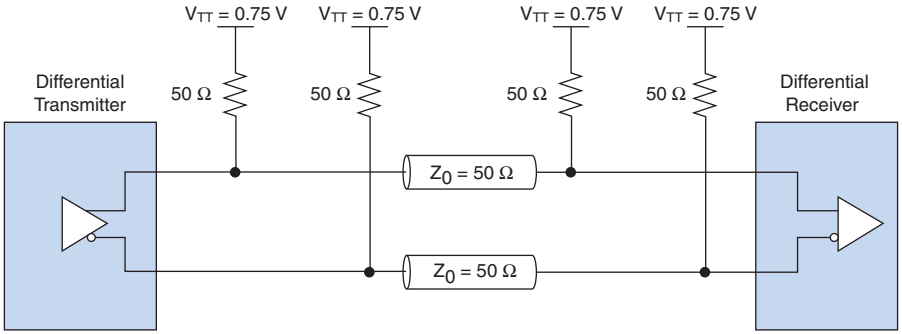


Figure 10–16. 1.5-V Differential HSTL Class II Termination



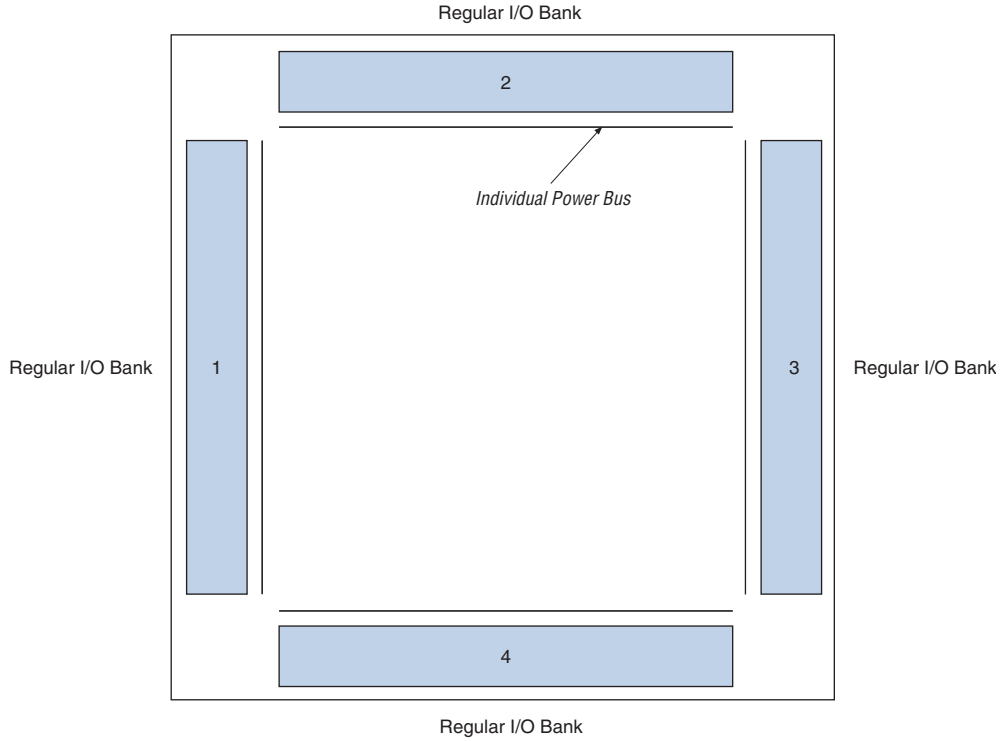
LVDS, RSDS and mini-LVDS

The LVDS standard is formulated under ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. Cyclone II devices are capable of running at a maximum data rate of 805 Mbps for input and 640 Mbps for output and still meet the ANSI/TIA/EIA-644 standard.

Because of the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS),

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*



Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Document Revision History

Table 11–6 shows the revision history for this document.

Table 11–6. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added *Note (1)* to Table 11–1. • Updated Figure 11–5 and added *Note (1)* • Added *Note (1)* to Table 11–2. • Updated Figure 11–6 and added *Note (1)* • Added *Note (1)* to Table 11–3. • Added *Note (1)* to Figure 11–9.	• Added information stating LVDS/RSDS/mini-LVDS I/O standards specifications apply at the external resistors network output.
November 2005 v2.1	• Updated Table 11–2. • Updated Figures 11–7 through 11–9. • Added Resistor Network Solution for RSDS. • Updated note for mini-LVDS Resistor Network table.	
July 2005 v2.0	• Updated "I/O Standards Support" section. • Updated Tables 11–1 through 11–3.	
November 2004 v1.1	• Updated Table 11–1. • Updated Figures 11–4, 11–5, 11–7, and 11–9.	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	

device releases its nSTATUS pin after a reset time-out period (maximum of 40 µs). When the nSTATUS pin is released and pulled high by a pull-up resistor, the configuration device reconfigures the chain. If this option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 µs to restart configuration. The external system can pulse the nCONFIG pin if the pin is under system control rather than tied to V_{CC}.

Additionally, if the configuration device sends all of its data and then detects that the CONF_DONE pin has not transitioned high, it recognizes that the FPGA has not configured successfully. Enhanced configuration devices wait for 64 DCLK cycles after the last configuration bit was sent for the CONF_DONE pin to transition high. EPC2 devices wait for 16 DCLK cycles. After that, the configuration device pulls its OE pin low, which in turn drives the target device's nSTATUS pin low. If you turn on the **Auto-restart configuration after error** option in the Quartus II software, the target device resets and then releases its nSTATUS pin after a reset time-out period (maximum of 40 µs). When nSTATUS transitions high again, the configuration device reconfigures the FPGA.

For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multiple Device PS Configuration Using a Configuration Device

You can use Altera enhanced configuration devices (EPC16, EPC8, and EPC4 devices) or EPC2 and EPC1 configuration devices to configure multiple Cyclone II devices in a PS configuration chain.

Figure 13–14 shows how to configure multiple devices with an enhanced configuration device. This circuit is similar to the configuration device circuit for a single device, except Cyclone II devices are cascaded for multiple device configuration.

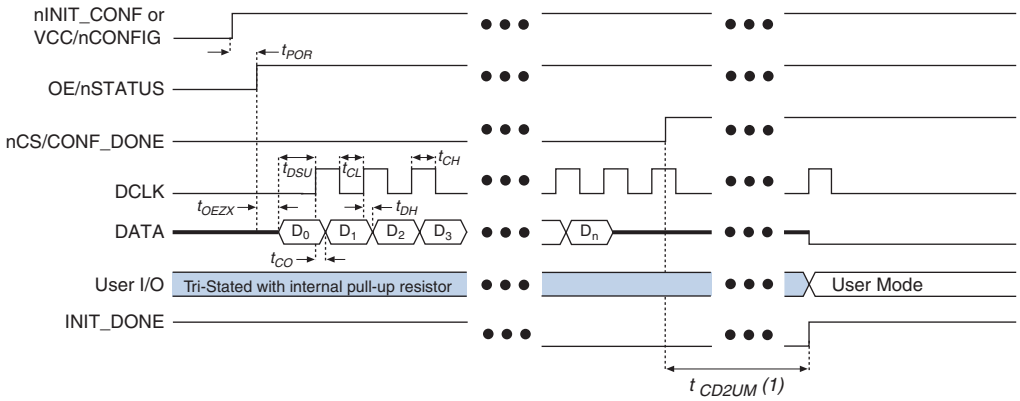
You can use a single configuration chain to configure Cyclone II devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, connect all the Cyclone II device CONF_DONE pins and connect all Cyclone II device nSTATUS pins together.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

During PS configuration, the design must meet the setup and hold timing parameters and maximum DCLK frequency. The enhanced configuration and EPC2 devices are designed to meet these interface timing specifications.

Figure 13–18 shows the timing waveform for the PS configuration scheme using a configuration device.

Figure 13–18. Cyclone II PS Configuration Using a Configuration Device Timing Waveform



Note to Figure 13–18:

(1) Cyclone II devices enter user mode 299 clock cycles after CONF_DONE goes high. The initialization clock can come from the Cyclone II internal oscillator or the CLKUSR pin.

For timing information, refer to the *Enhanced Configuration Devices (EPC4, EPC8, and EPC16) Data Sheet* or the *Configuration Devices for SRAM-based LUT Devices Data Sheet* in the *Configuration Handbook*.

For more information on device configuration options and how to create configuration files, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.