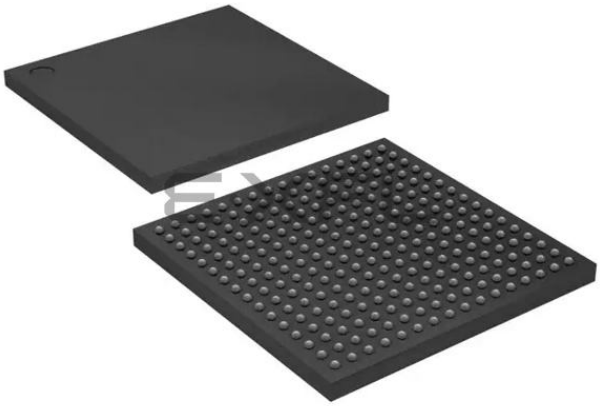

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20af256a7n

Each global clock network has a clock control block to select from a number of input clock sources (PLL clock outputs, CLK[] pins, DPCLK[] pins, and internal logic) to drive onto the global clock network. Table 2–2 lists how many PLLs, CLK[] pins, DPCLK[] pins, and global clock networks are available in each Cyclone II device. CLK[] pins are dedicated clock pins and DPCLK[] pins are dual-purpose clock pins.

Table 2–2. Cyclone II Device Clock Resources

Device	Number of PLLs	Number of CLK Pins	Number of DPCLK Pins	Number of Global Clock Networks
EP2C5	2	8	8	8
EP2C8	2	8	8	8
EP2C15	4	16	20	16
EP2C20	4	16	20	16
EP2C35	4	16	20	16
EP2C50	4	16	20	16
EP2C70	4	16	20	16

Figures 2–11 and 2–12 show the location of the Cyclone II PLLs, CLK[] inputs, DPCLK[] pins, and clock control blocks.

Table 3–1. Cyclone II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. In the **Settings** dialog box in the Assignments menu, click **Device & Pin Options**, then **General,** and then turn on the **Auto Usercode option**.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.174	–0.186	0.11	0.07	0.071	0.081	ns

Notes to Table 5–21:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–22. EP2C5/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.212	1.267	2.210	2.351	2.54	2.540	ns
t_{COUT}	1.214	1.269	2.226	2.364	2.548	2.548	ns
t_{PLLCIN}	–0.259	–0.277	–0.043	–0.095	–0.106	–0.096	ns
$t_{PLLCOUT}$	–0.257	–0.275	–0.027	–0.082	–0.098	–0.088	ns

Notes to Table 5–22:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C8/A Clock Timing Parameters

Tables 5–23 and 5–24 show the clock timing parameters for EP2C8/A devices.

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.339	1.404	2.405	2.565	2.764	2.774	ns
t_{COUT}	1.353	1.419	2.439	2.597	2.793	2.803	ns
t_{PLLCIN}	–0.193	–0.204	0.055	0.015	0.016	0.026	ns

EP2C70 Clock Timing Parameters

Tables 5–33 and 5–34 show the clock timing parameters for EP2C70 devices.

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

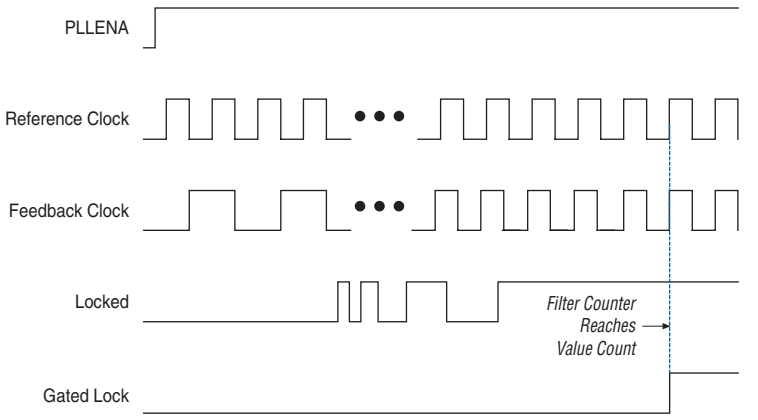
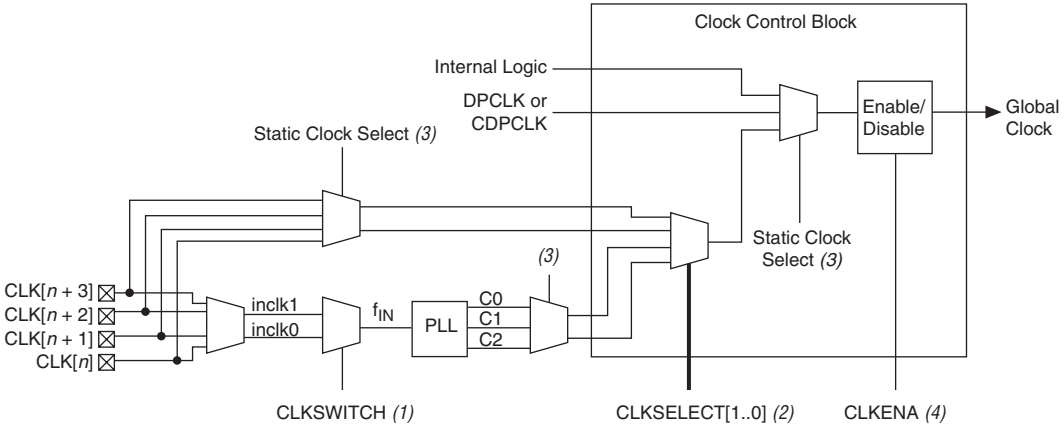


Figure 7–11. Clock Control Block



Notes to Figure 7–11:

(1) The `CLKSWITCH` signal can either be set through the configuration file or dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The `CLKSELECT[1..0]` signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enable or disable the global clock network in user mode.

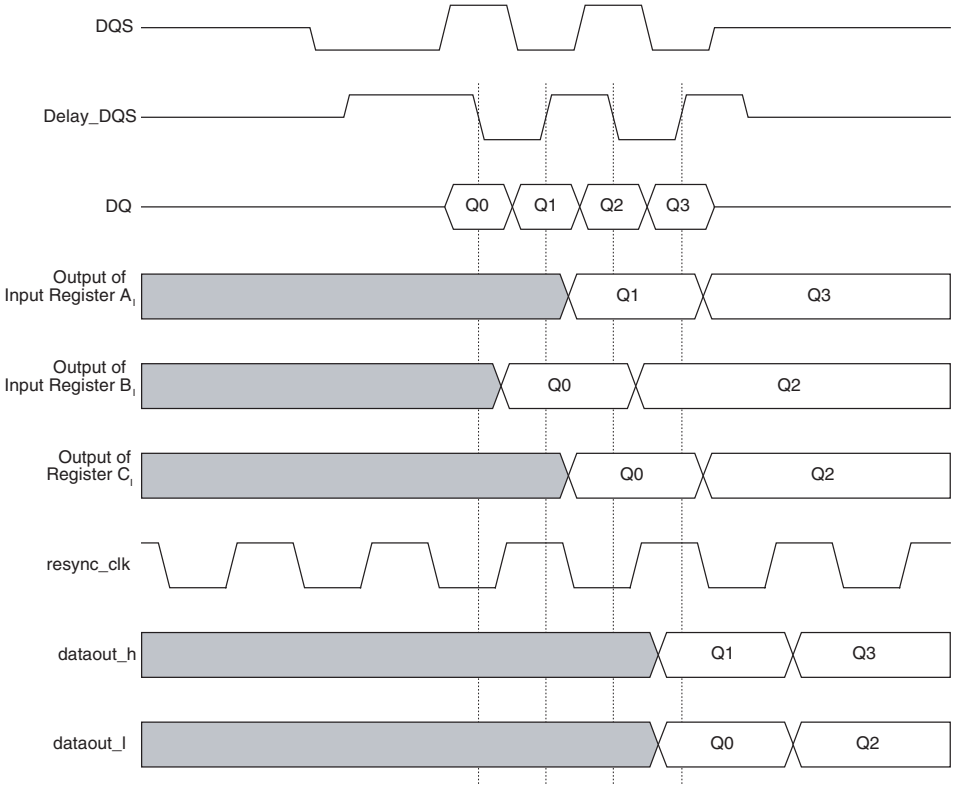
Each PLL generates three clock outputs through the `c[1..0]` and c2 counters. Two of these clocks can drive the global clock network through the clock control block.

Global Clock Network Clock Source Generation

There are a total of 8 clock control blocks on the smaller Cyclone II devices (EP2C5 and EP2C8 devices) and a total of 16 clock control blocks on the larger Cyclone II devices (EP2C15 devices and larger). Figure 7–12 shows the Cyclone II clock inputs and the clock control blocks placement.

Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

3.3-V LVCMOS (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL ($-0.3\ V \leq V_I \leq 3.9\ V$). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels specified by the 3.3-V LVCMOS I/O standard.

3.3-V (PCI Special Interest Group [SIG] PCI Local Bus Specification Revision 3.0)

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 3.0 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires a 3.3-V V_{CCIO}. The 3.3-V PCI standard does not require input reference voltages or board terminations.

The side (left and right) I/O banks on all Cyclone II devices are fully compliant with the 3.3V PCI Local Bus Specification Revision 3.0 and meet 32-bit/66 MHz operating frequency and timing requirements.

Table 10–2 lists the specific Cyclone II devices that support 64- and 32-bit PCI at 66 MHz.

Table 10–2. Cyclone II 66-MHz PCI Support (Part 1 of 2)

Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLineBGA®		✓

I/O Termination

The majority of the Cyclone II I/O standards are single-ended, non-voltage-referenced I/O standards and, as such, the following I/O standards do not specify a recommended termination scheme:

- 3.3-V LVTTL and LVCMOS
- 2.5-V LVTTL and LVCMOS
- 1.8-V LVTTL and LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI and PCI-X

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

For more information on termination for voltage-referenced I/O standards, refer to "Supported I/O Standards" on page 10–1.

Differential I/O Standard Termination

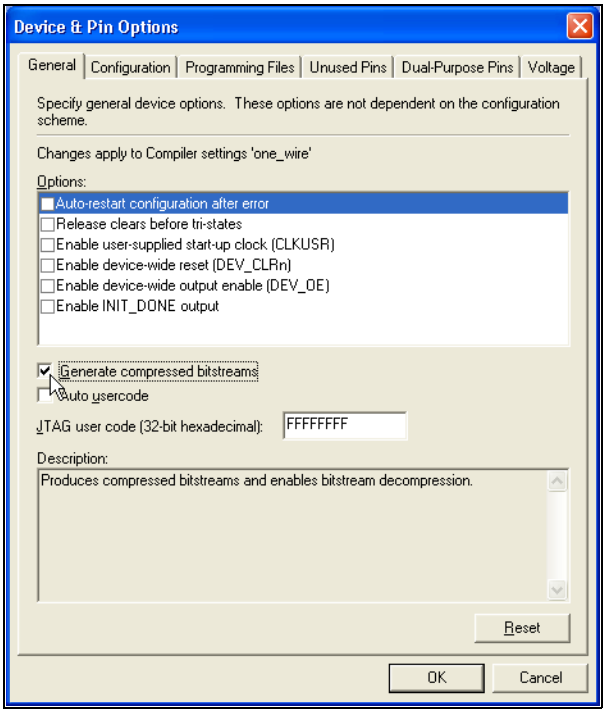
Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Cyclone II devices support differential I/O standards LVDS, RSDS, and mini-LVDS, and differential LVPECL.

For more information on termination for differential I/O standards, refer to "Supported I/O Standards" on page 10–1.

November 2005 v2.1	• Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6.	—
July 2005 v2.0	Updated Table 10–1.	—
November 2004 v1.1	Updated Table 10–7.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings

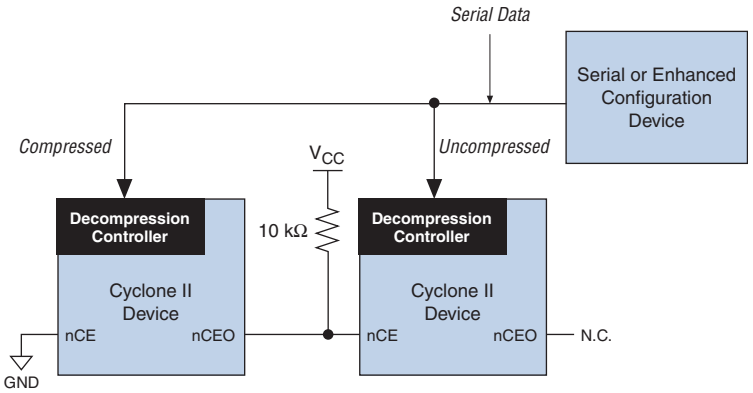


You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

When multiple Cyclone II devices are cascaded, the compression feature can be selectively enabled for each device in the chain. Figure 13–2 depicts a chain of two Cyclone II devices. The first Cyclone II device has compression enabled and therefore receives a compressed bitstream from the configuration device. The second Cyclone II device has the compression feature disabled and receives uncompressed data.

Figure 13–2. Compressed & Uncompressed Configuration Data in a Programming File



You can generate programming files (for example, POF files) for this setup in the Quartus II software.

Active Serial Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone II devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memory that feature a simple, four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

For more information on serial configuration devices, see the *Serial Configuration Devices Data Sheet* in the Configuration Handbook.

You must connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. You should buffer the DCLK and DATA lines for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

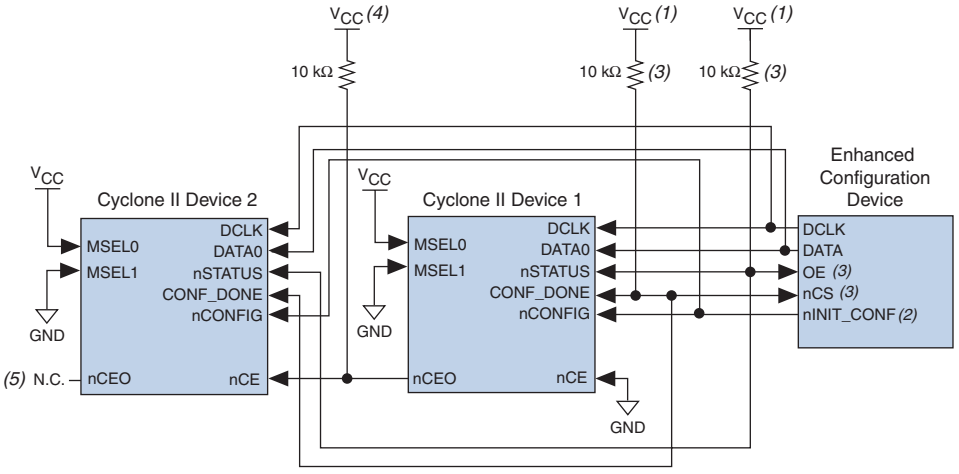
Since all nSTATUS and CONF_DONE pins are connected, if any Cyclone II device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first Cyclone II detects an error, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single Cyclone II device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the Cyclone II devices release their nSTATUS pins after a reset time-out period (maximum of 40 µs). After all nSTATUS pins are released and pulled high, the MAX II device reconfigures the chain without pulsing nCONFIG low. If the **Auto-restart configuration after error** option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

Figure 13–14. Multiple Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 13–14:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You cannot cascade enhanced configuration devices (EPC16, EPC8, and EPC4 devices).

When configuring multiple devices, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multiple device configuration chains, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

When configuring multiple devices with the PS scheme, connect the first Cyclone II device's nCE pin to GND and connect its nCEO pin to the nCE pin of the Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin to the V_{CCIO} level when

nCONFIG low for at least 2 µs to restart configuration. The microprocessor or controller can only transition the nCONFIG pin low if the pin is under system control and not tied to V_{CC}.

The enhanced configuration devices support parallel configuration of up to eight devices. The *n*-bit (*n* = 1, 2, 4, or 8) PS configuration mode allows enhanced configuration devices to concurrently configure a chain of FPGAs. These devices do not have to be the same device family or density; they can be any combination of Altera FPGAs with different designs. An individual enhanced configuration device DATA pin is available for each targeted FPGA. Each DATA line can also feed a chain of FPGAs. Figure 13–15 shows how to concurrently configure multiple devices using an enhanced configuration device.

When designing a Cyclone II board for JTAG configuration, use the guidelines in Table 13–10 for the placement of the dedicated configuration pins.

Table 13–10. Dedicated Configuration Pin Connections During JTAG Configuration

Signal	Description
nCE	On all Cyclone II devices in the chain, nCE should be driven low by connecting it to ground, pulling it low via a resistor, or driving it by some control circuitry. For devices that are also in multiple device AS, or PS configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Cyclone II devices in the chain, nCEO can be used as a user I/O or connected to the nCE of the next device. If nCEO is connected to the nCE of the next device, the nCEO pin must be pulled high to V_{CCIO} by an external 10-kΩ pull-up resistor to help the internal weak pull-up resistor. If the nCEO pin is not connected to the nCE pin of the next device, you can use it as a user I/O pin after configuration.
MSEL	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If only JTAG configuration is used, you should tie these pins to ground.
nCONFIG	Driven high by connecting to V_{CC}, pulling up via a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CC} individually. nSTATUS pulling low in the middle of JTAG configuration indicates that an error has occurred.
CONF_DONE	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CC} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

Figure 13–23 shows JTAG configuration of a Cyclone II device with a microprocessor.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Cyclone II devices is enabled upon device power-up. Because this circuitry may be used for BST or in-circuit reconfiguration, this circuitry must be enabled only at specific times as mentioned in "Using IEEE Std. 1149.1 BST Circuitry" on page 14–16.

If the IEEE Std. 1149.1 circuitry will not be utilized at any time, the circuitry should be permanently disabled. Table 14–3 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Cyclone II devices to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 14–3. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
TMS	V_{CC}
TCK	GND
TDI	V_{CC}
TDO	Leave open

Note to Table 14–3:
(1) There is no software option to disable JTAG in Cyclone II devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the 10-bit checkerboard pattern "1010101010" does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller has not reached the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
  - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.