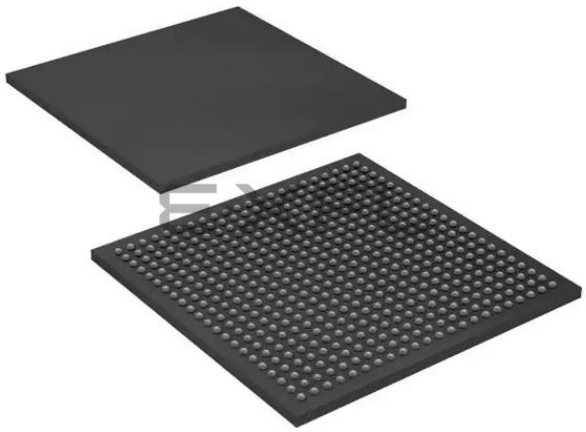

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Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	315
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20af484a7n

Chapter Revision Dates

The chapters in this book, *Cyclone II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *February 2008*
Part number: *CII51001-3.2*

Chapter 2. Cyclone II Architecture
Revised: *February 2007*
Part number: *CII51002-3.1*

Chapter 3. Configuration & Testing
Revised: *February 2007*
Part number: *CII51003-2.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *February 2007*
Part number: *CII51004-3.1*

Chapter 5. DC Characteristics and Timing Specifications
Revised: *February 2008*
Part number: *CII51005-4.0*

Chapter 6. Reference & Ordering Information
Revised: *February 2007*
Part number: *CII51006-1.4*

Chapter 7. PLLs in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51007-3.1*

Chapter 8. Cyclone II Memory Blocks
Revised: *February 2008*
Part number: *CII51008-2.4*

Chapter 9. External Memory Interfaces
Revised: *February 2007*
Part number: *CII51009-3.1*

There are five dynamic control input signals that feed the embedded multiplier: `signa`, `signb`, `clk`, `clkena`, and `aclr`. `signa` and `signb` can be registered to match the data signal input path. The same `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

For more information on Cyclone II embedded multipliers, see the *Embedded Multipliers in Cyclone II Devices* chapter.

I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- V_{REF} pins

Cyclone II device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–20 shows the Cyclone II IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. You can use IOEs as input, output, or bidirectional pins.

Advanced I/O Standard Support

Table 2–17 shows the I/O standards supported by Cyclone II devices and which I/O pins support them.

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS *(1)*	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(2)*	*(2)*	*(2)*
PCI and PCI-X *(1) (3)*	Single ended	3.3 V	3.3 V			✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(4)*	*(5)*	2.5 V				✓	
		2.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential SSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI). Cyclone II devices support the RSDS and mini-LVDS I/O standards at data rates up to 311 Mbps at the transmitter.

A subset of pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. The dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry. Therefore, internal logic performs serialization and deserialization functions.

Cyclone II pin tables list the pins that support the high-speed I/O interface. The number of LVDS channels supported in each device family member is listed in Table 2–18.

Table 2–18. Cyclone II Device LVDS Channels (Part 1 of 2)

Device	Pin Count	Number of LVDS Channels *(1)*
EP2C5	144	31 (35)
	208	56 (60)
	256	61 (65)
EP2C8	144	29 (33)
	208	53 (57)
	256	75 (79)
EP2C15	256	52 (60)
	484	128 (136)
EP2C20	240	45 (53)
	256	52 (60)
	484	128 (136)
EP2C35	484	131 (139)
	672	201 (209)
EP2C50	484	119 (127)
	672	189 (197)

Devices Can Be Driven before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone II devices before or during power-up or power-down without damaging the device. Cyclone II devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the Cyclone II device's output buffers are turned off during system power-up or power-down. The Cyclone II device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to 3.3V. Refer to Figure 4–1 for more information.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The V_{CCIO} and V_{CCINT} must have monotonic rise to their steady state levels. (Refer to Figure 4–3 for more information.) The power supply ramp rates can range from 100 µs to 100 ms for non "A" devices. Both V_{CC} supplies must power down within 100 ms of each other to prevent I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Cyclone II devices meet the following hot-socketing specification.

- The hot-socketing DC specification is $| I_{IOPIN} | < 300$ µA.
- The hot-socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

This specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional capacitance for trace, connector, and loading separately.

I_{IOPIN} is the current at any user I/O pin on the device. The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

If you cannot meet the maximum V_{CC} ramp time requirement, you must use an external component to hold nCONFIG low until the power supplies have reached their minimum recommend operating levels. Otherwise, the device may not properly configure and enter user mode.

Conclusion

Cyclone II devices are hot socketable and support all power-up and power-down sequences with the one requirement that V_{CCIO} and V_{CCINT} be powered up and down within 100 ms of each other to keep the I/O pins from driving out. Cyclone II devices do not require any external devices for hot socketing and power sequencing.

Document Revision History

Table 4–1 shows the revision history for this document.

Table 4–1. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Updated "I/O Pins Remain Tri-Stated during Power-Up" section. • Updated "Power-On Reset Circuitry" section. • Added footnote to Figure 4–3.	• Specified V_{CCIO} and V_{CCINT} supplies must be GND when "not powered". • Added clarification about input-tristate behavior. • Added infomation on V_{CC} monotonic ramp.
July 2005 v2.0	Updated technical content throughout.	
February 2005 v1.1	Removed ESD section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–13 shows the Cyclone II device pin capacitance for different I/O pin types.

Table 5–13. Device Capacitance *Note (1)*

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin.	6	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin.	6	pF
C_{VREF}	Input capacitance for dual-purpose VREF pin when used as VREF or user I/O pin.	21	pF
C_{CLK}	Input capacitance for clock pin.	5	pF

Note to Table 5–13:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflectometry (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

You can calculate the power usage for your design using the PowerPlay Early Power Estimator and the PowerPlay Power Analyzer feature in the Quartus® II software.

The interactive PowerPlay Early Power Estimator is typically used during the early stages of FPGA design, prior to finalizing the project, to get a magnitude estimate of the device power. The Quartus II software PowerPlay Power Analyzer feature is typically used during the later stages of FPGA design. The PowerPlay Power Analyzer also allows you to apply test vectors against your design for more accurate power consumption modeling.

In both cases, only use these calculations as an estimation of power, not as a specification. For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *Power Estimation and Analysis* section in volume 3 of the *Quartus II Handbook*.

You can obtain the Excel-based PowerPlay Early Power Estimator at www.altera.com. Refer to Table 5–3 on page 5–3 for typical I_{CC} standby specifications.

The power-up current required by Cyclone II devices does not exceed the maximum static current. The rate at which the current increases is a function of the system power supply. The exact amount of current consumed varies according to the process, temperature, and power ramp rate. The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.8V_HSTL_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_HSTL_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
LVDS	t_{PI}	651	682	1036	1075	1113	1113	ps
	t_{PCOUT}	434	455	669	699	728	728	ps
PCI	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps
PCI-X	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps

Notes to Table 5–41 :

(1) These numbers are for commercial devices.

(2) These numbers are for automotive devices.

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	438	439	439	338	362	387	338	362	387
	8 mA	306	321	336	267	283	299	267	283	299
	12 mA	139	179	220	193	198	202	193	198	202
	16 mA	145	158	172	139	147	156	139	147	156
	20 mA	65	77	90	74	79	84	74	79	84
	24 mA	19	20	21	14	18	22	14	18	22
LVCMOS	4 mA	298	305	313	197	205	214	197	205	214
	8 mA	190	205	219	112	118	125	112	118	125
	12 mA	43	72	101	27	31	35	27	31	35
	16 mA	87	99	110	—	—	—	—	—	—
	20 mA	36	46	56	—	—	—	—	—	—
	24 mA	24	25	27	—	—	—	—	—	—
2.5V	4 mA	228	233	237	270	306	343	270	306	343
	8 mA	173	177	180	191	199	208	191	199	208
	12 mA	119	121	123	—	—	—	—	—	—
	16 mA	64	65	66	—	—	—	—	—	—
1.8V	2 mA	452	457	461	332	367	403	332	367	403
	4 mA	321	347	373	244	291	337	244	291	337
	6 mA	227	255	283	178	222	266	178	222	266
	8 mA	37	118	199	58	133	207	58	133	207
	10 mA	41	72	103	46	85	123	46	85	123
	12 mA	7	8	10	13	28	44	13	28	44
1.5V	2 mA	738	764	789	540	604	669	540	604	669
	4 mA	499	518	536	300	354	408	300	354	408
	6 mA	261	271	282	60	103	146	60	103	146
	8 mA	22	25	29	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

Table 7–2 provides an overview of the Cyclone II PLL features.

Table 7–2. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *(1)*
Phase shift	Down to 125-ps increments *(2)*, *(3)*
Programmable duty cycle	✓
Number of internal clock outputs	Up to three per PLL *(4)*
Number of external clock outputs	One per PLL *(4)*
Locked port can feed logic array	✓
PLL clock outputs can feed logic array	✓
Manual clock switchover	✓
Gated lock	✓

Notes to Table 7–2:

(1) *m* and post-scale counter values range from 1 to 32. *n* ranges from 1 to 4.

(2) The smallest phase shift is determined by the voltage control oscillator (VCO) period divided by 8.

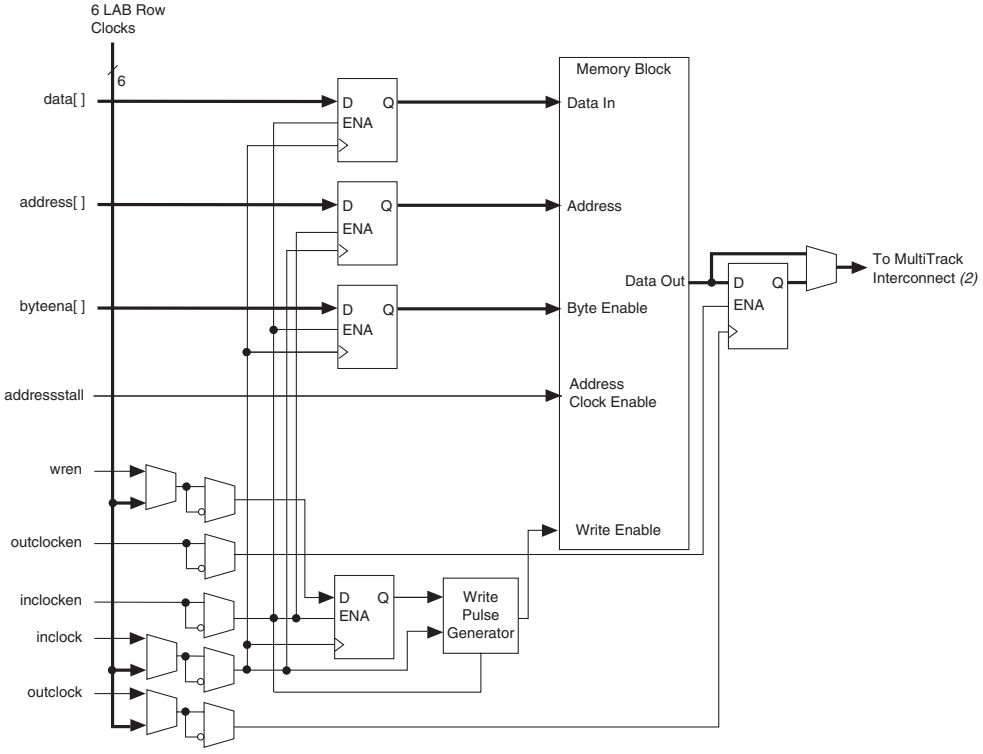
(3) For degree increments, Cyclone II devices can shift output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the VCO frequency.

(4) The Cyclone II PLL has three output counters that drive the global clock network. One of these output counters (c2) can also drive a dedicated external I/O pin (single ended or differential). This counter output can also drive the external clock output (`PLL<#>_OUT`) and internal global clock network at the same time.

Cyclone II PLL Hardware Overview

Cyclone II devices contain up to four PLLs that are arranged in the four corners of the Cyclone II device as shown in Figure 7–1, which shows a top-level diagram of the Cyclone II device and the PLL locations.

Figure 8–16. Cyclone II Input/Output Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–16:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTrack interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

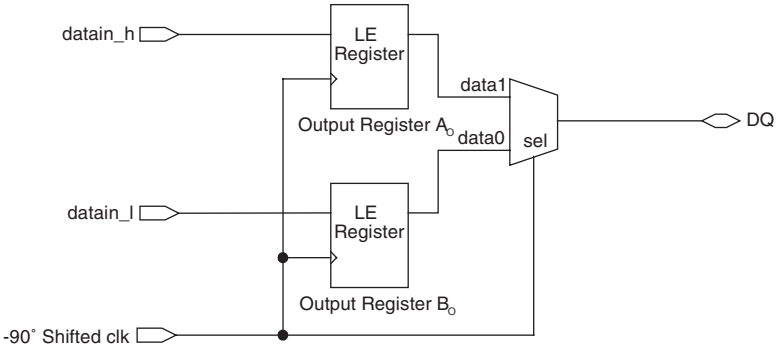
Read/Write Clock Mode

Cyclone II memory blocks can implement read/write clock mode for simple dual-port memory. The write clock controls the blocks' data inputs, write address, and write enable signals. The read clock controls the data output, read address, and read enable signals. The memory blocks support independent clock enables for each clock for the read- and write-side registers. This mode does not support asynchronous clear signals for the registers. Figure 8–17 shows a memory block in read/write clock mode.

DDR Output Registers

Figure 9–14 shows a schematic representation of DDR output implemented in a Cyclone II device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

Figure 9–14. DDR Output Implementation for DDR Memory Interfaces



While the clock signal is logic-high, the output from output register A_O is driven onto the DDR output pin. While the clock signal is logic-low, the output from output register B_O is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin. Altera recommends the use of `altdq` and `altdqs` megafunctions to implement this output logic. This automatically provides the required tight placement and routing constraints on the LE registers and the output multiplexer.

Figure 9–15 shows examples of functional waveforms from a DDR output implementation.

Section IV. I/O Standards

This section provides information on Cyclone® II single-ended, voltage referenced, and differential I/O standards.

This section includes the following chapters:

- Chapter 10, Selectable I/O Standards in Cyclone II Devices
- Chapter 11, High-Speed Differential Interfaces in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 10–1. SSTL-2 Class I Termination

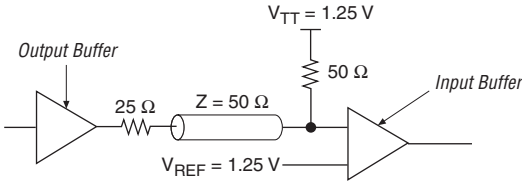
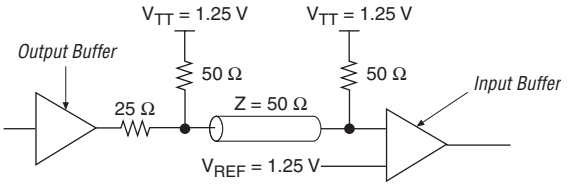


Figure 10–2. SSTL-2 Class II Termination



Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of – 0.3 V ≤V_I ≤V_{CCIO} + 0.3 V. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

After applying the equation above, apply one of the equations in Table 10–11, depending on the package type.

Table 10–11. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤9 (per VCCIO/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤5 (per VCCIO/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (refer to Table 10–4 for more details) and compatible V_{REF} voltage levels.

DDR and QDR Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads have to be on the same power bank as DQS pads. With the DDR and DDR2 memory interfaces, a VCCIO and ground pair can have a maximum of five DQ pads.

For a QDR interface, D is the QDR output and Q is the QDR input. D pads and Q pads have to be on the same power bank as CQ. With the QDR and QDRII memory interfaces, a VCCIO and ground pair can have a maximum of five D and Q pads.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone II QDR and QDRII performance is not guaranteed.

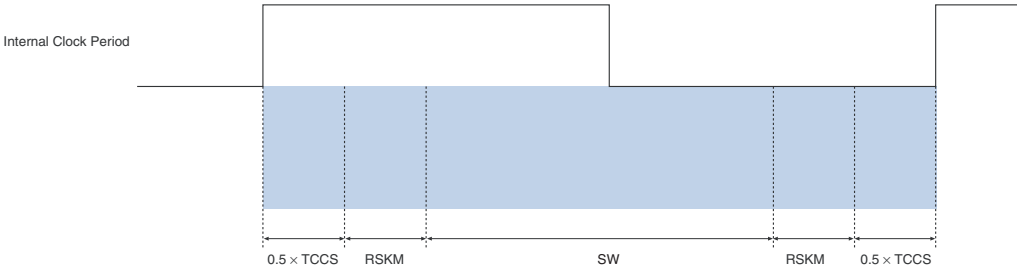
DC Guidelines

There is a current limit of 240 mA per eight consecutive output top and bottom pins per power pair, as shown by the following equation:

$$\sum_{pin}^{pin+7} I_{PIN} < 240mA \text{ per power pair}$$

There is a current limit of 240 mA per 12 consecutive output side (left and right) pins per power pair, as shown by the following equation:

Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

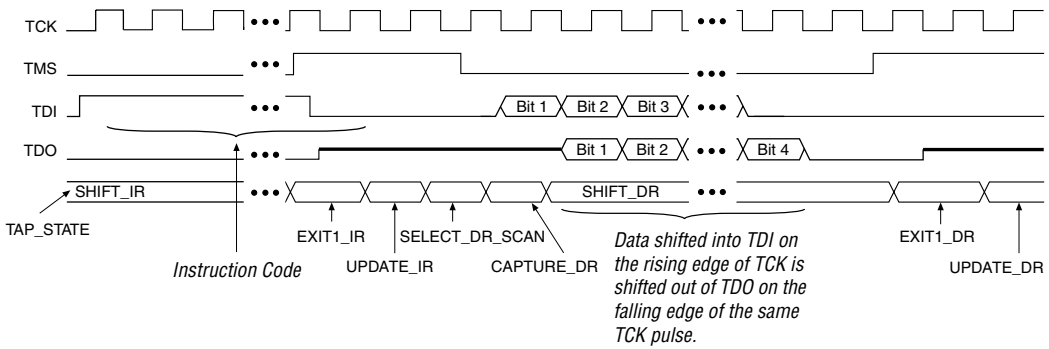
See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

Figure 14–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

The IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the TDI and TDO ports, and the device IDCODE is shifted out. The IDCODE for Cyclone II devices are listed in the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

USERCODE Instruction Mode

The USERCODE instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the TDI and TDO ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit USERCODE register. The UES is then shifted out through the device ID register. The UES value is not user defined until after the device has been configured. Before configuration, the UES value is set to the default value.

CLAMP Instruction Mode

The CLAMP instruction mode is used to allow the boundary-scan register to determine the state of the signals driven from the pins. In CLAMP instruction mode, the bypass register is selected as the serial path between the TDI and TDO ports.